Inertial Sensor (6DoF)

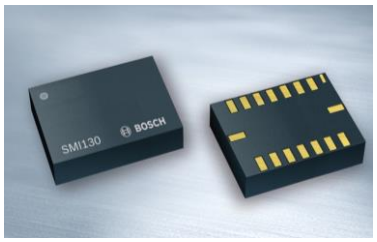
for Non-Safety Automotive Applications

SMI130

Robert Bosch GmbH, Reutlingen, Germany

Part No.: 0273 141 181

Document No.: 1 279 929 758



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1 Introduction

The SMI130 is a combined triaxial accelerometer (ACC) and triaxal gyroscope (GYR) for non-safety related applications, e.g. for in-dash navigation in the passenger compartment. Within one package, the SMI130 offers the detection of acceleration and angular rate for the x-, y- and z-axis. The digital standard serial peripheral interface (SPI) of the SMI130 allows for bi-directional data transmission.

Basic Description

Sensor	Bosch Part Nr.	Type	Range	Resolution
SMI130	0273 141 181	Accelerometer	±2, ±4, ±8, ±16 g	12 bit
		Gyroscope	±125 .. ±2000 °/s	16 bit

Key Features

2 inertial sensors in one device	Advanced triaxial 16 bit gyroscope and a versatile, leading edge triaxial 12 bit accelerometer for reduced PCB space and simplified signal routing
Small package	LGA, 16 pins, footprint 3.0 x 4.5 mm², height 0.95 mm
Common voltage supplies	VDD voltage range: 2.4 ... 3.6 V
Digital interface	SPI, TWI (compatible with I^2C)
Smart operation and integration	Gyroscope and accelerometer can be operated individually
Consumer electronics suite	MSL1, RoHS compliant, halogen- and Pb-free
Operating temperature	-40 ... +85 °C
Programmable functionality	Acceleration and rate ranges selectable Low-pass filter bandwidths selectable
On-chip temperature sensor	Factory trimmed, 8 bit, typical

Bosch points out that the system/product does not implement any ASIL-classified requirements (in the sense of ISO 26262). Therefore it has not been approved by Bosch for applications in which Bosch delivered system/product has an ASIL-related (above QM) role. This implies the following limitations:

- The SMI130 must not be used if it influences safety goals with ratings higher than ASIL QM. Safety goals are defined in the overall system (i.e., on item level).
- Bosch cannot provide any quantitative failure analysis (e.g. FTA or FMEDA) for the SMI130.
- The SMI130 does not provide a CRC to check communication errors within a SPI/I2C frame.
- The SMI130 does not provide error flags to detect malfunctions of the ASIC.

2 Technical Description

2.1 Working Principle of the Sensing Elements (MEMS)

The inertial sensor SMI130 is based upon a combined two-chip stacked concept: Accelerometer and gyroscope both consist of a separated evaluation ASIC and a micro-mechanical sensing element (MEMS). The SMI130 combines both stacked sensors side-by-side within a standard LGA package.

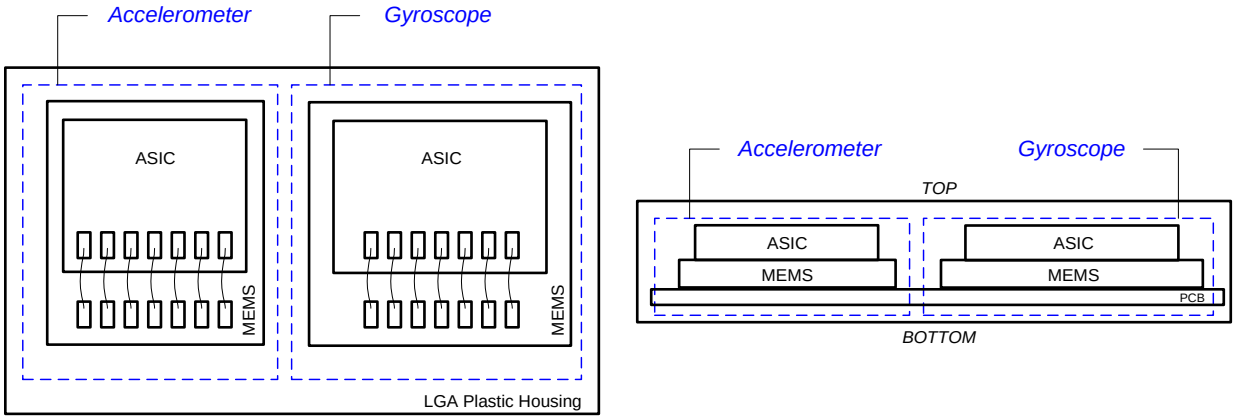


Figure 2-1: Schematics of the SMI130 mechanical design (left: top view; right: side view). The SMI130 consists of two separate sensing elements (accelerometer and gyroscope, dashed boxes), packed in one single LGA package. Each sensing element has its readout ASIC stacked on top of the sensitive MEMS.

2.2 Block Diagram

Figure 2-2 shows the basic building blocks of the SMI130. As stated before the accelerometer and the gyroscope have separate ASICs (light gray boxes).

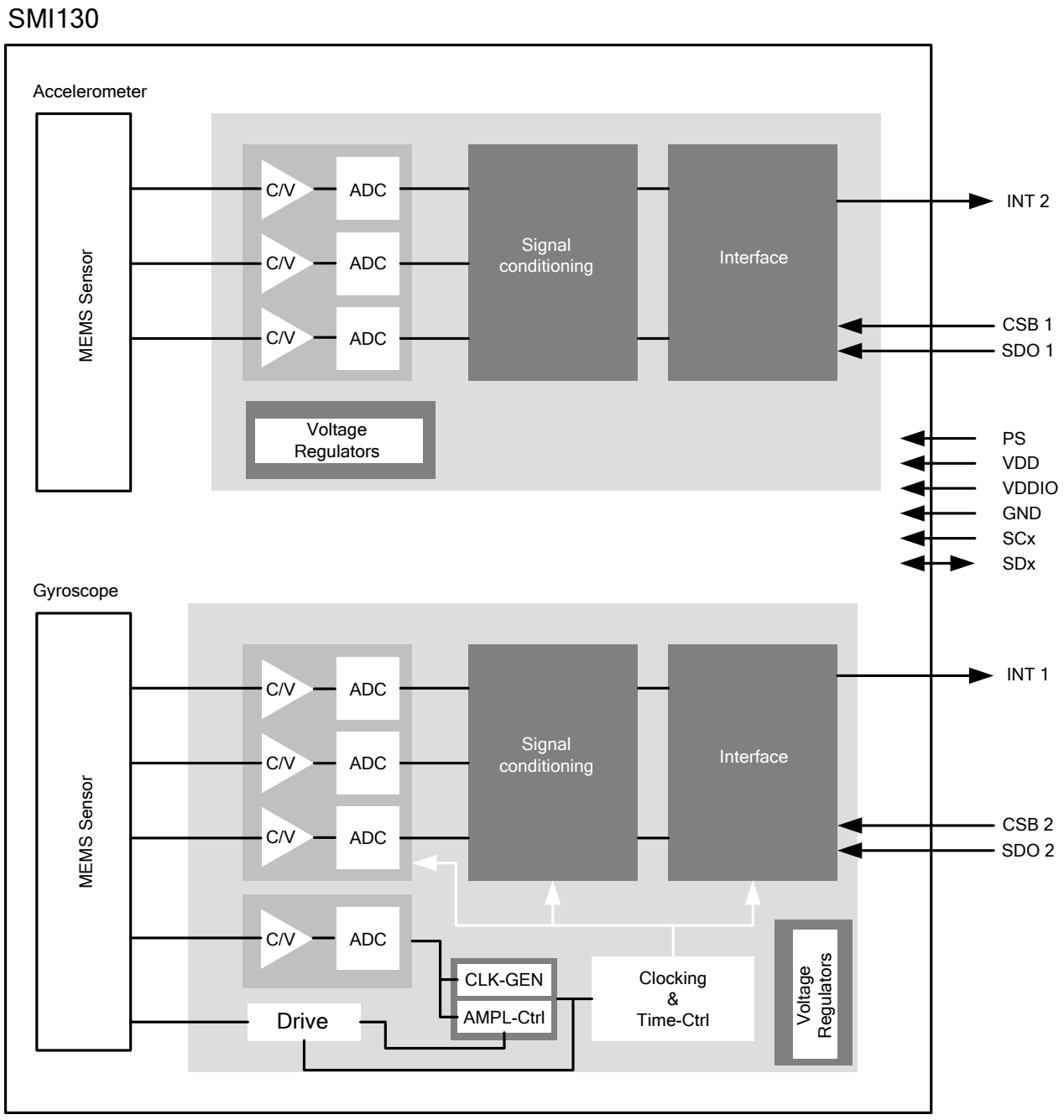


Figure 2-2: Simplified block diagram of the SMI130. Both MEMS elements are evaluated by their own ASIC (light gray). Both sensing elements detect voltage (V) variations, feeding the analog-digital converter (ADC). The digital signals are further processed by and accessible via SPI.

2.3 Signal Path

Accelerometer

The accelerometer offers temperature and acceleration data for all three spatial dimensions. For the latter, the differential capacitance change (C) of the corresponding sensing element is detected. These signals correspond to the voltage (V) entering the hybrid algorithmic analog-digital-converter (ADC), translating the formerly analog signals into digital serial bit streams at a rate of 400 kHz. Then, the detected signal is translated into a data word of max. 16 bits and enters the digital signal processor (DSP).

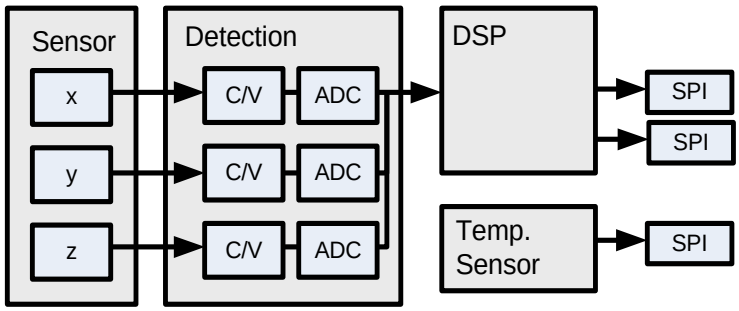


Figure 2-3: Simplified signal path of the accelerometer.

Within the DSP (see Figure 2-4), the data is corrected for the analog-digital conversion, gained and offset corrected. A low-pass filter engine provides an adjustable data bandwidth. Here, the sampling rate is directly connected with the selected bandwidth.

The low-pass engine can be bypassed so that unfiltered data is accessible.

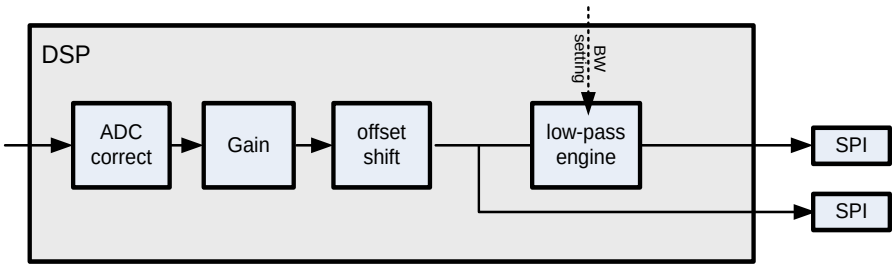


Figure 2-4: Simplified DSP element (accelerometer).

Gyroscope

The signal path of the gyroscope is sketched in Figure 2-5. For proper data acquisition, five blocks are necessary for each rate axis, i.e., the drive, the (MEMS) sensor, the detection, the controller & demodulator and the digital signal processor (DSP). In addition, a temperature signal is provided by the temperature sensor.

The drive is a closed-loop system that actively moves each sensor element at ~25 kHz.

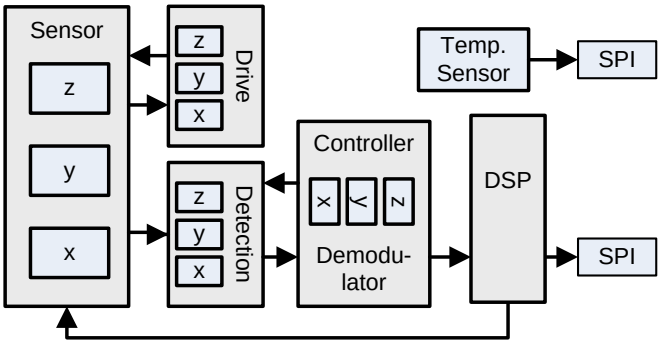


Figure 2-5: Simplified signal path of the gyroscope.

Data acquisition is independent from the drive and the temperature sensor. A more detailed sketch of the signal path of one axis is given in Figure 2-6.

The block ‘Detection’ corresponds to the analog part of the SMI130. The differential capacitance change (C) of each sensing element corresponds to the rate data of the respective sensing axis. The latter corresponds to the voltage (V) entering the 25 kHz filter which is conform to the drive frequency. The 1-bit Σ/Δ-converter (ADC) translates the signal into a digital serial bit stream at a rate of 400 kHz.

This bit stream is fed into both the common mode controller and the demodulator. The first back-couples to ‘C/V’ in order to negate mass deviation of the sensor element. The latter demodulates the 25 kHz data signal which then enters the DSP.

In the DSP, the signal is both fed into the quadrature correction and offset shifted. Afterwards, it is fine gained and low pass filtered before being accessible via e.g. SPI.

The block ‘Quad. Corr.’ back-couples onto distinctive pads on the sensing element to compensate for possible deviations from the oscillation axis.

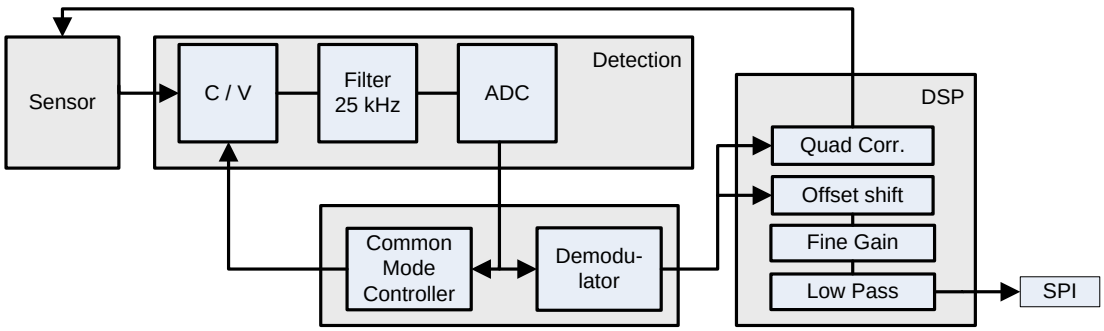


Figure 2-6: Path of the detection signal for one axis (gyroscope).

2.4 Power Management

The SMI130 has two distinct power supply pins:

- VDD is the main power supply for the internal blocks.
- VDDIO is a separate power supply pin mainly used for the supply of the interface.

Switching sequence of power supply VDD and VDDIO

If VDD and VDDIO are not powered on simultaneously (via directly connecting both pins), VDD has to be powered on first and set to a specified level. Thereafter, VDDIO can be powered on.

Not following this sequence might result in voltage levels of both pins which are not limited. This also applies if both are operated within their corresponding operating range.

In the case that the VDDIO supply is off, all interface pins (CSB, SDI, SCK, PS) must be kept close to GNDIO potential.

The SMI130 provides a **power-on reset (POR)** generator. It resets the logic part and the register values after powering on VDD and VDDIO.

1. After POR, all settings are reset to the default values.
2. In the case that VDD < 1.8 V or VDDIO < 1V for longer than 1 ms, a safe POR (see below) is required. Else, the device may end up in an undefined state.

Safe POR options:

#1 Ramp down VDD to a level ≤ 0.35 V monotonically and stay below this level for ≥ 2 µs. There is no constraint on the VDDIO level. Ramp up VDD and VDDIO to operating range.

#2 Ramp down VDDIO to a level ≤ 0.35 V monotonically and stay below for ≥ 2 µs while keeping VDD ≥ 1.8 V. Ramp up VDD and VDDIO to operating range.

SPI protocol requirements:

The PS pin must be directly connected to GNDIO.

2.5 Soft Reset

A soft reset causes all user configuration settings to be overwritten with their default value and the sensor to enter normal mode. A waiting time of 200 ms after a soft reset of the SMI130 accelerometer and gyroscope is recommended.

Accelerometer

A soft reset is initiated by writing the value 0xB6 to register ACC 0x14 (BGW_SOFTRESET).

Gyroscope

A soft reset is initiated by writing the value 0xB6 to register GYR 0x14 (BGW_SOFTRESET).

2.6 Sensor Data

The data representation of the SMI130 follows two´s complement representation.

2.6.1 Accelerometer

For each axis, the 12 bits of acceleration data are split into a MSB upper part (bits <11:4> of acceleration data) and a LSB lower part (bits <3:0> of acceleration data). Registers ACC 0x02 (ACCD_X_LSB) and ACC 0x03 (ACCD_X_MSB) contain the acceleration data for the x-channel, registers ACC 0x04 (ACCD_Y_LSB) and ACC 0x05 (ACCD_Y_MSB) for the y-channel and registers ACC 0x06 (ACCD_Z_LSB) and ACC 0x07 (ACCD_Z_MSB) for the z-channel. The LSB part (all axes) also contains the *new_data* flag. It is recommended to always start reading out the LSB register first.

In order to ensure data integrity, a **shadowing procedure** can be enabled. In this case, the content of the MSB register is locked by reading the corresponding LSB register until the MSB register is read as well. This means that the MSB register always has to be read in order to remove the data lock. Shadowing can be disabled (enabled) by writing 1 (0) to bit 6 (*shadow_dis*) in the register ACC 0x13 (ACCD_HBW). For disabled shadowing, the content of both MSB and LSB registers is updated by new values immediately. Unused bits of the LSB registers may have any value and should be ignored.

New data can be identified by bit 0 (*new_data* flag) of each LSB register. It is set after the data registers have been updated and reset if either the corresponding MSB or LSB part is read.

Two different streams of acceleration data are available, **unfiltered and filtered** data. The unfiltered data is sampled with 2 kHz. The sampling rate (output data rate ODR) of the filtered data depends on the selected filter bandwidth (BW) and is always twice the selected bandwidth (BW = ODR/2). Which kind of data is stored in the data registers depends on bit 7 (*data_high_bw*) in register ACC 0x13 (ACCD_HBW). If bit 7 is 0 (1), filtered (unfiltered) data is stored in the registers. Both data streams are offset-compensated.

The **bandwidth** of filtered acceleration data is determined by setting bits <4:0> (*bw*) in register ACC 0x10 (PMU_BW) as shown in the following table.

bw	Bandwidth	Update Time
00xxx	*)	-
01000	7.81 Hz	64 ms
01001	15.63 Hz	32 ms
01010	31.25 Hz	16 ms
01011	62.5 Hz	8 ms
01100	125 Hz	4 ms
01101	250 Hz	2 ms
01110	500 Hz	1 ms
01111	1000 Hz	0.5 ms
1xxxx	*)	-

*) The *bw* settings 00xxx and 1xxxx are both reserved. It is recommended to actively set an application specific, appropriate bandwidth and to use the *bw* range from 01000 to 01111.

The acceleration measurement **range** can be selected via bits <3:0> (*range*) in register ACC 0x0F (PMU_RANGE) according to the table below.

range	**Acceleration Measurement Range**	**Resolution**
0011	±2 g	1024 LSB/g
0101	±4 g	512 LSB/g
1000	±8 g	256 LSB/g
1100	±16 g	128 LSB/g
others	reserved	-

2.6.2 Gyroscope

For each axis, the 16 bits of rate data are split into a MSB upper part (bits <15:8> of rate data) and a LSB lower part (bits <7:0> of rate data). Registers 0x02 (RATE_X_LSB) and 0x03 (RATE_X_MSB) contain the rate data for the x-channel, registers 0x04 (RATE_Y_LSB) and 0x05 (RATE_Y_MSB) for the y-channel and 0x06 (RATE_Z_LSB) and 0x07 (RATE_Z_MSB) for the z-channel. It is recommended to always start reading the rate data registers with the LSB part.

An example for the range setting of ±125 °/s is shown in the table below.

Decimal value	+32767	...	0	...	-32767
Angular rate	+125 °/s	...	0	...	-125 °/s

In order to ensure data integrity, a **shadowing procedure** can be enabled. In this case, the content of the MSB register is locked by reading the corresponding LSB register until the MSB register is read as well. This means that the MSB register always has to be read in order to remove the data lock. Shadowing can be disabled (enabled) by writing 1 (0) to bit 6 (*shadow_dis*) in the register 0x13 (RATE_HBW). When shadowing is disabled, the content of both the MSB and the LSB register is updated by a new value immediately.

Two different streams of rate data are available, **unfiltered and filtered** data. The SMI130 processes the 2 kHz data of the analog frontend with a CIC/decimation filter, followed by an IIR filter, before sending it to the interrupt handler. The possible decimation factors are 2, 5, 10 and 20. It is also possible to bypass these filters and use the unfiltered 2 kHz data. The sampling rate (output data rate ODR) of the filtered data depends on the selected filter bandwidth (BW). Which kind of data is stored in the rate data registers depends on bit 7 (*data_high_bw*) in register 0x13 (RATE_HBW). If bit 7 is 0 (1), filtered (unfiltered) data is stored in the registers.

The **bandwidth** of filtered rate data is determined by setting bits <3:0> (*bw*) in register 0x10 (BW) as shown in the following table.

bw	**Filter Bandwidth [Hz]**	**ODR [Hz]**	**Decimation Factor**
0111	32	100	20
0110	64	200	10
0101	12	100	20
0100	23	200	10
0011	47	400	5
0010	116	1000	2
0001	230	2000	0
0000	523 (unfiltered)	2000	0
1xxx	reserved	reserved	reserved

The rate measurement **range** can be selected via bits <2:0> (*range*) in register 0x0F (RANGE) according to the table below.

range	Rate Measurement Range	Resolution
000	±2000 °/s	16.4 LSB/°/s
001	±1000 °/s	32.8 LSB/°/s
010	±500 °/s	65.6 LSB/°/s
011	±250 °/s	131.2 LSB/°/s
100	±125 °/s	262.4 LSB/°/s
others	reserved	-

2.6.3 Temperature Sensor

The temperature sensor data of the SMI130 have a width of 8 bits which covers a temperature range of 128 K. Temperature data can be read from registers ACC 0x08 (TEMP) and GYR 0x08 (TEMP). The slope is typically 0.5 K/LSB.

3 Application

Proper function of the sensor in the overall system must be validated by the customer.

3.1 Sensing Axes Orientation

If the sensor is accelerated and/or rotated in the indicated directions, the corresponding channels of the device will deliver a positive acceleration and/or yaw rate signal (dynamic acceleration). If the sensor is at rest without any rotation and the force of gravity is acting contrary to the indicated directions, the output of the corresponding acceleration channel will be 'zero' (static acceleration).

Example:

If the sensor is at rest or at uniform motion in a gravity field according to Figure 3-1, the output signals are:

- ± 0 for the ACC x-channel
  ± 0 for the GYR Ω_X-channel
- ± 0 for the ACC y-channel
  ± 0 for the GYR Ω_Y-channel
- + 1 g for the ACC z-channel
  ± 0 for the GYR Ω_Z –channel

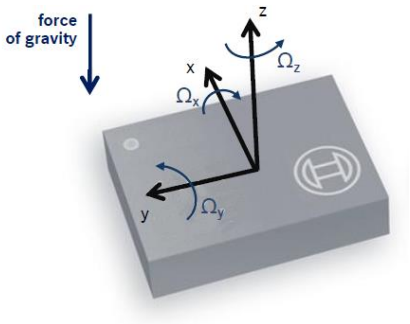
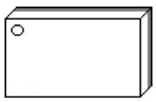
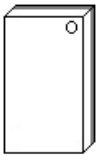
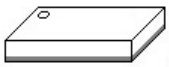
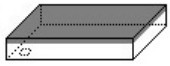


Figure 3-1: Sensing axes orientation.

The table below lists all corresponding output signals of x, y, z and Ω_X, Ω_Y, Ω_Z while the sensor is at rest or at uniform motion in a gravity field, assuming a ±2 g accelerometer range setting and a top down gravity vector as shown above.

Sensor Orientation						
Output Signal x	0 0	**+1 g** **+1024 LSB**	0 0	**-1 g** **-1024 LSB**	0 0	0 0
Output Signal y	**-1 g** **-1024 LSB**	0 0	**+1 g** **+1024 LSB**	0 0	0 0	0 0
Output Signal z	0 0	0 0	0 0	0 0	**+1 g** **+1024 LSB**	**-1 g** **-1024 LSB**
Output Signal Ω_X	0 0	0 0	0 0	0 0	0 0	0 0
Output Signal Ω_Y	0 0	0 0	0 0	0 0	0 0	0 0
Output Signal Ω_Z	0 0	0 0	0 0	0 0	0 0	0 0

3.2 Pin-out

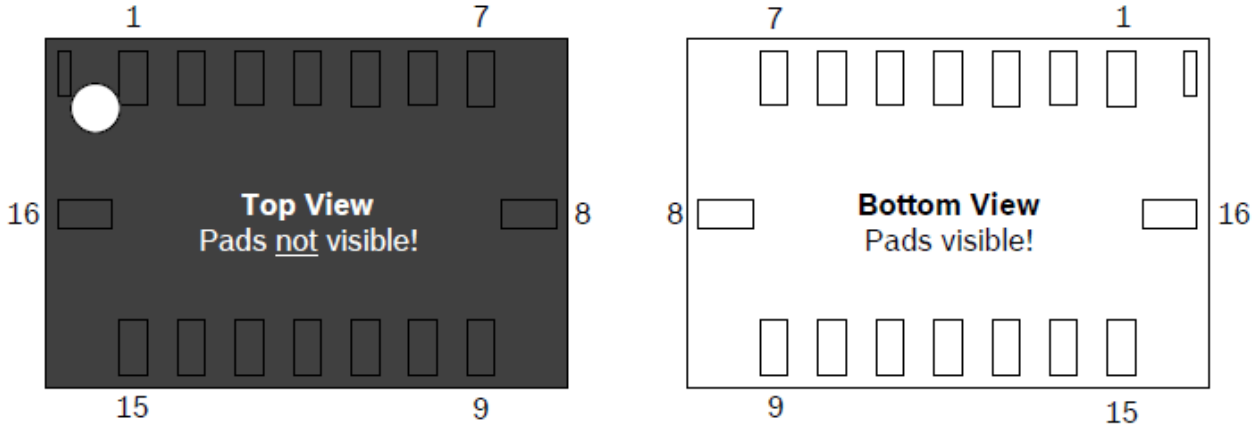


Figure 3-2: Pin-out top (left) and bottom (right) view.

Pin	Name	I/O Type	Description	Connect to - SPI -	Connect to - TWI -
1	INT2	Digital out	Interrupt pin (ACC)	INT2 / DNC	INT2 / DNC
2	NC	--	--	GND	GND
3	VDD	Supply	Power supply analog & digital domain	VDD	VDD
4	GNDA	Ground	Ground for analog domain	GND	GND
5	CSB2	Digital in	SPI chip select GYR	CSB2	DNC (float)
6	GNDIO	Ground	Ground for I/O	GND	GND
7	PS	Digital in	Protocol select	GND	VDDIO
8	SCx	Digital in	Serial clock	SCK	SCL
9	SDx	Digital I/O	SPI: serial data in; TWI: serial data in/out	SDI	SDA
10	SDO2	Digital out	SPI: serial data out GYR	SDO2	SDO2
11	VDDIO	Supply	Digital I/O supply voltage	VDDIO	VDDIO
12	INT1	Digital I/O	Interrupt pin (GYR)	INT1 / DNC	INT1 / DNC
13	NF	--	--	DNC	DNC
14	CSB1	Digital in	SPI chip select ACC	CSB1	DNC (float)
15	SDO1	Digital out	SPI: serial data out ACC	SDO1	SDO1
16	NF	--	--	DNC	DNC

DNC: Do not connect

INTx: If not needed, DNC

3.3 Dimensions and Weight

Dimensions [mm]: width: 3.0; length: 4.5; height 0.95
Weight [mg]: 27.48

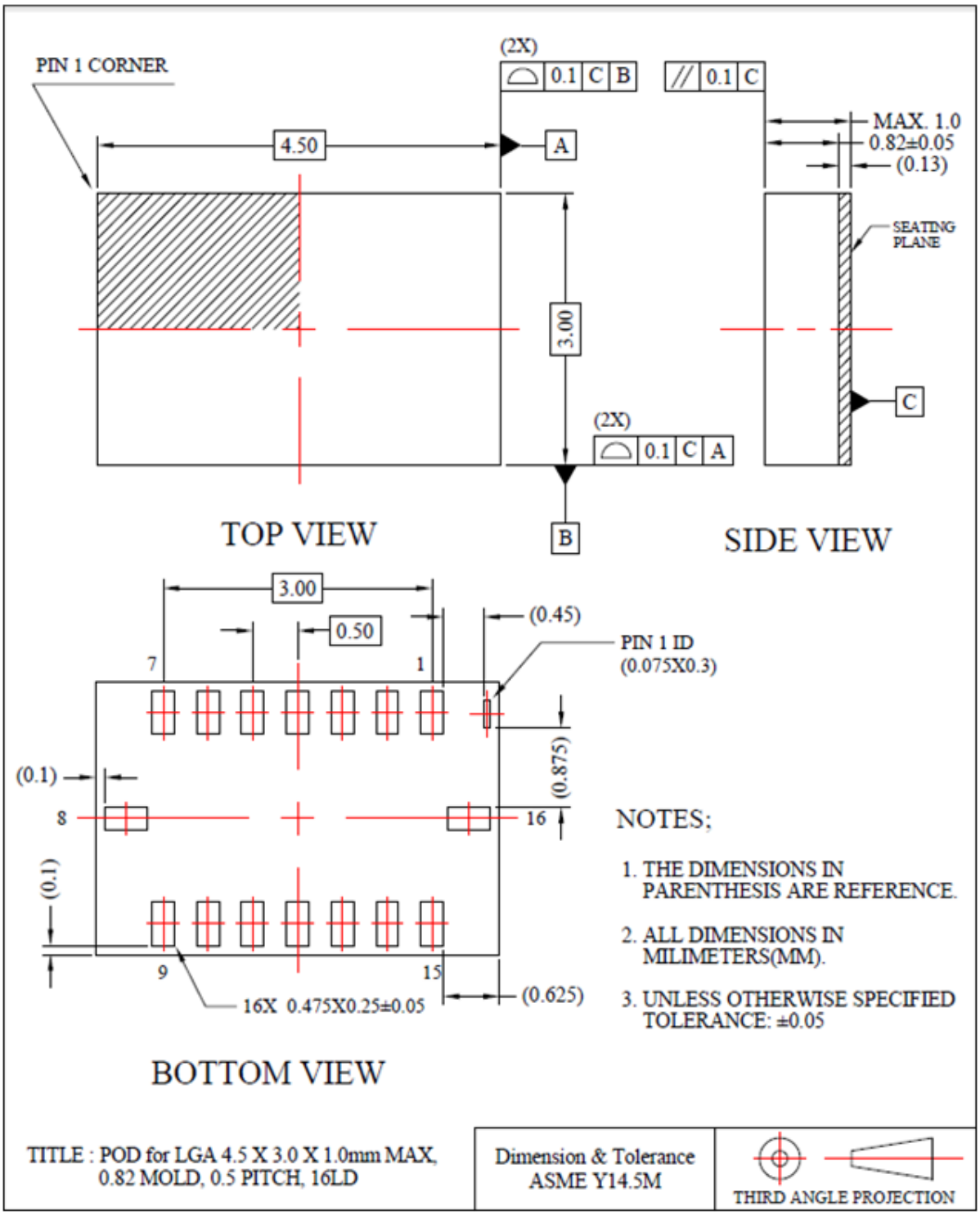


Figure 3-3: SMI130 package outline drawing.

3.4 Marking

Labeling	Name	Symbol	Remark
● xxx AYYWW CCC	Product number	xxx	3 numeric digits, fixed to identify product type
	Sub-con ID	A	1 alphanumeric digit, variable to identify sub-con
	Date code	YYWW	4 numeric digits, fixed to identify YY: “year”, WW: “working week”
	Counter ID	CCC	3 numeric digits, variable to generate trace-code
	Pin 1 identifier	●	--

3.5 Footprint

For the design of the landing patterns, the dimensioning as shown in Figure 3-4 is recommended.

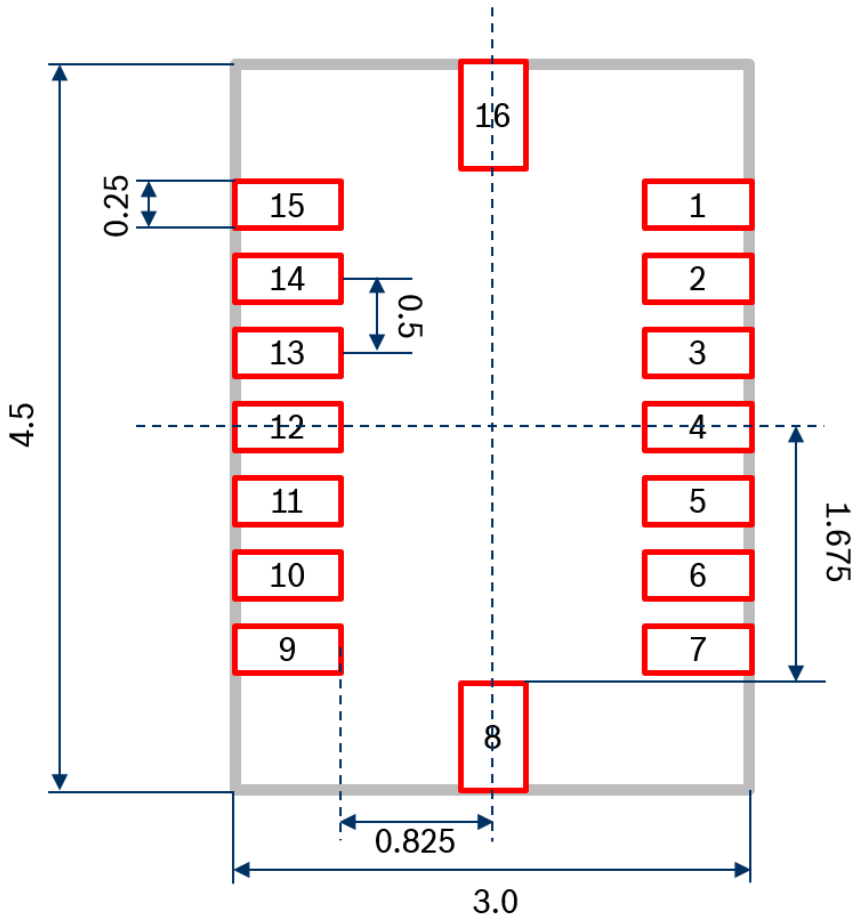


Figure 3-4: SMI130 footprint.

The sensor housing is a standard LGA package. The dimensions are given in mm.
Note: Unless otherwise specified, the tolerance is ± 0.05 mm.

3.6 SPI Connection Diagram

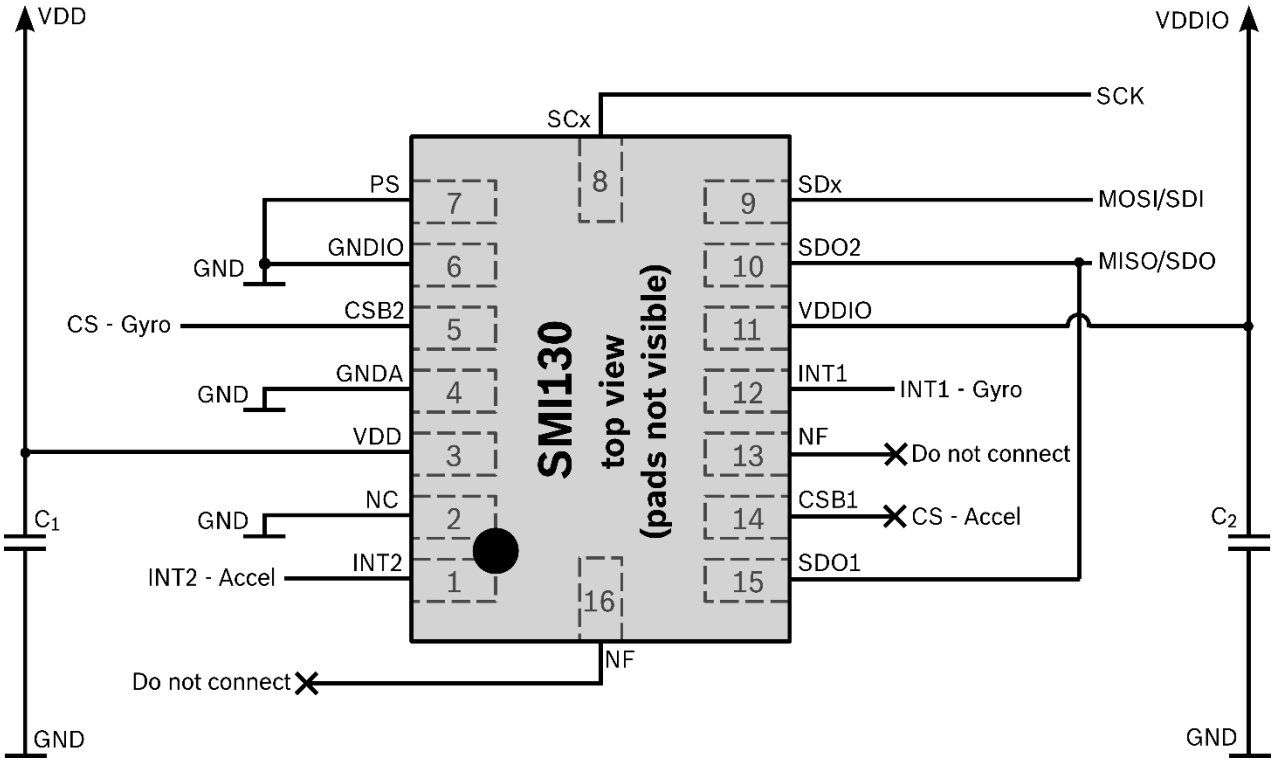


Figure 3-5: SPI connection diagram.

C_1, C_2: 100 nF
INT1: see GYR registers 0x18, 0x16
INT2: see ACC registers 0x1A, 0x20

3.7 TWI Connection Diagram

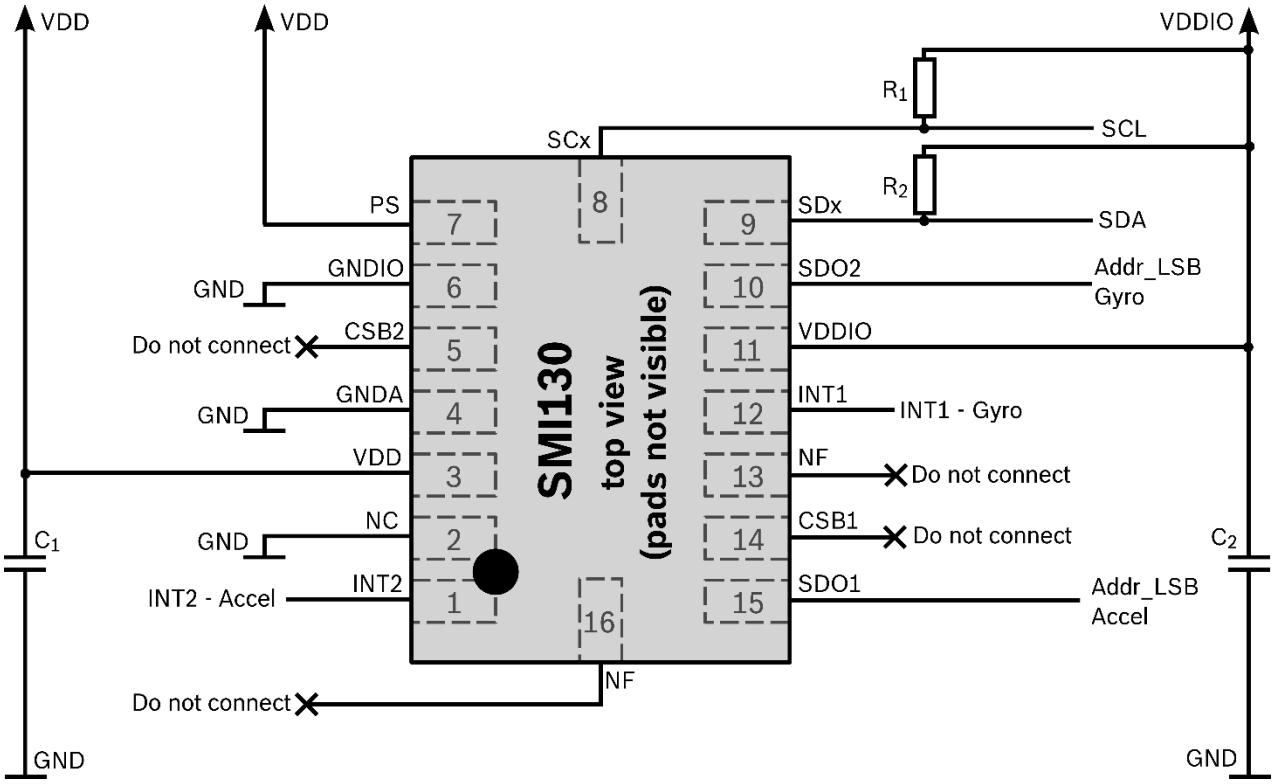


Figure 3-6: TWI connection diagram.

C_1, C_2: 100 nF
R_1, R_2: pull-up resistors
INT1: see GYR registers 0x18, 0x16
INT2: see ACC registers 0x1A, 0x20
SDO1: see Chapter 5.2
SDO2: see Chapter 5.2

4 Specified Parameters

The data in this chapter, unless otherwise noted, apply for the valid operation conditions given in Section 4.2. All following figures include voltage, temperature and lifetime effects if not noted otherwise. All figures except sensitivity are only valid without an external stimulus being applied. All operation conditions are only valid if no failure flags indicate any malfunction. All figures except for the noise itself exclude noise effects.

Proper function of the sensor in the overall system must be validated by the customer.

In any case, the electrical stability (power supply and EMC) of each system design including the SMI130 must be evaluated in advance to guarantee proper functionality during operation.

In any case, the mechanical stability of each system design including the SMI130 must be evaluated in advance to guarantee proper functionality during operation.

4.1 Absolute Maximum Ratings

Any values beyond the given ratings may seriously damage the device. The sensor must be discarded when exceeding these limits.

ABSOLUTE MAXIMUM RATINGS				
Parameter	**Condition**	**Min**	**Max**	**Unit**
Voltage at supply pin	VDD pin	-0.3	4.27	V
Voltage at supply pin	VDDIO pin	-0.3	3.6	V
Voltage at any logic pin	non-supply pin	-0.3	VDDIO + 0.3	V
Mechanical shock	free fall onto hard surfaces		1.2	m
Mechanical shock	duration <1 ms		2000	g
ESD	HBM, any pin		2	kV
ESD	CDM		500	V
ESD	MM		200	V

4.2 Operating Conditions

OPERATING CONDITIONS						
Parameter	**Symbol**	**Condition**	**Min**	**Typi-cal**	**Max**	**Unit**
Supply voltage internal do-mains	VDD		2.4	3.3	3.6	V
Supply voltage I/O domain	VDDIO		1.2	3.3	3.6	V
Voltage input low level	V_{IL}				0.3 VDDIO	-
Voltage input high level	V_{IH}		0.7 VDDIO			-
Voltage output low level	V_{OL}	I_{OL} = 3 mA			0.23 VDDIO	-
Voltage output high level	V_{OH}	I_{OH} = 3 mA	0.8 VDDIO			-
Operating temperature	T		-40		85	°C
Lifetime		According to AEC-Q100 grade 3 requirements				

4.3 Accelerometer

ACCELEROMETER (all data for range 2 g, BW 1000 Hz)						
Parameter	**Symbol**	**Condition / Comment**	**Min**	**Typical**	**Max****	**Unit**
Measurement range	g_{FS}	selectable		±2 ±4 ±8 ±16		g
Supply current	I_{DD}	w/o SPI communication		0.15		mA
Start-up time	$t_{s,up}$	POR			0.2	s
Sensitivity error		including temp., axis, and lifetime effects			±5	%
Sensitivity error		T = 25 °C over lifetime			±4	%
Sensitivity temperature drift	TCS	nominal VDD supply, over full temp. range		±0.025		% / K
Zero-g offset* - reset to zero at end of customer line -		lifetime and temperature effects		x ±35 y ±40 z ±90		mg
Zero-g offset		T = 25 °C over lifetime		±70		mg
Zero-g offset temperature drift		nominal VDD supply, over full temp. range		±1		mg / K
Bandwidth	BW	2nd order filter, selectable		8, 16, 31, 63, 125, 250, 500, 1000		Hz
Nonlinearity BW: 62.5 Hz, range: ± 2g	NL	best fit straight line, no life-time		±25		mg
Noise rms		T = 25 °C, nominal VDD supply no lifetime		6		mg
Temperature sensor slope				0.5		K / LSB
Temperature sensor offset		T = 25 °C		±5		K
Cross axis sensitivity		including temp., axis, and lifetime effects		±3		%

* Assumption: ACC is offset corrected at end of customer production line on system level
** For specified maximum values, please refer to the Technical Customer Documentation.

4.4 Gyroscope

Gyroscope (all data for range 2000 °/s, BW 47 Hz)						
Parameter	**Symbol**	**Condition / Comment**	**Min**	**Typical**	**Max****	**Unit**
Measurement range	R_{FS}	selectable		±125 ±250 ±500 ±1000 ±2000		°/s
Supply current	I_{DD}	w/o SPI communication			6.5	mA
Start-up time	$t_{s,up}$	POR			0.2	s
Sensitivity error		including temp., axis, and lifetime effects			±5.5	%
Sensitivity error		T = 25 °C over lifetime		±1	±2.1	%
Sensitivity temperature drift	TCS	nominal VDD supply, over full temp. range		±0.03	±0.06	% / K
Zero-rate offset* - reset to zero at end of customer line -		lifetime and temperature effects		±0.5	±2	°/s
Zero-rate offset		T = 25 °C over lifetime			±1	°/s
Zero-rate offset temperature drift		nominal VDD supply, over full temp. range		±0.015	±0.03	°/s / K
Bandwidth	BW			12, 23, 32, 47, 64, 116, 230, 523 (unfiltered)		Hz
Nonlinearity BW: 23 Hz; range: ±125 °/s	NL	best fit straight line, no life-time			±1	°/s
Noise rms		T = 25 °C, nominal VDD supply no lifetime		0.1	0.3	°/s
Temperature sensor slope				0.5		K / LSB
Temperature sensor offset		T = 25°C		±5		K
Cross axis sensitivity		including temp., axis, and lifetime effects		±2	±5.5	%

* Assumption: GYR is offset corrected at end of customer production line on system level
** For specified maximum values, please refer to the Technical Customer Documentation.

5 Communication

5.1 Serial Peripheral Interface (SPI)

For communication, the SMI130 supports the SPI 4-wire protocol as a slave with a host device. The mapping for the interface of both accelerometer and gyroscope is given in the table below:

Pin	Name	Description
15	SDO1	ACC data output
10	SDO2	GYR data output
9	SDx	SDI serial data in
14	CSB1	ACC chip select (enable)
5	CSB2	GYR chip select (enable)
8	SCx	SCK serial clock

The SPI timing specification of the SMI130 is given in the following table:

Parameter	Symbol	Condition	Min	Max	Units
Clock frequency	f_{SPI}	max. load on SDI or SDO = 25 pF		10	MHz
SCK low pulse	t_{SCKL}		20		ns
SCK high pulse	t_{SCKH}		48		ns
SDI setup time	t_{SDI_setup}		20		ns
SDI hold time	t_{SDI_hold}		20		ns
SDO output delay	t_{SDO_OD}	load = 25 pF		40	ns
		load = 250 pF, VDDIO = 2.4 V		40	ns
CSB setup time	t_{CSB_setup}		20		ns
CSB hold time	t_{CSB_hold}		40		ns
Idle time between write accesses	$t_{IDLE\_wacc\_nm}$		2		µs

Figure 5-1 shows the definition of the SPI timing.

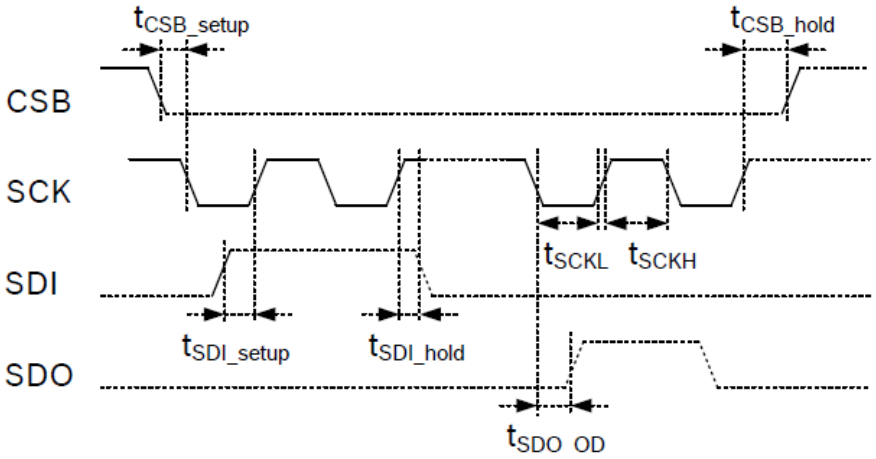


Figure 5-1: SPI timing diagram.

The SPI interface of the SMI130 is compatible with two modes, 00 and 11. The automatic selection between [CPOL = 0 and CPHA = 0] and [CPOL = 1 and CPHA = 1] is controlled based on the value of SCK after a falling edge of CSB (1 or 2). For single byte read as well as write operations, 16-bit protocols are used. The SMI130 also supports multiple-byte read operations.

For standard SPI configuration, CSB (1 or 2 - chip select low active), SCK (serial clock), SDI (serial data input) and SDO (1 or 2 - serial data output) pins are used. The communication starts when CSB (1 or 2) is pulled low by the SPI master and stops when CSB (1 or 2) is pulled high. SCK is also controlled by the SPI master. SDI and SDO (1 or 2) are driven at the falling edge of SCK and should be captured at the rising edge of SCK.

The basic write operation waveform for the 4-wire configuration is depicted in Figure 5-2. During the full write cycle, SDO remains in high-impedance state.

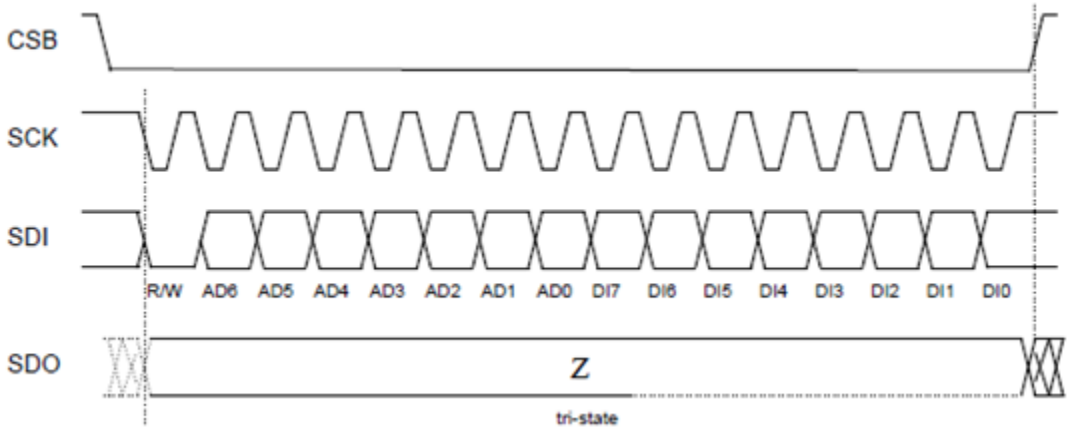


Figure 5-2: 4-wire basic SPI write sequence (mode 11).

The basic read operation waveform for the 4-wire configuration is depicted in Figure 5-3.

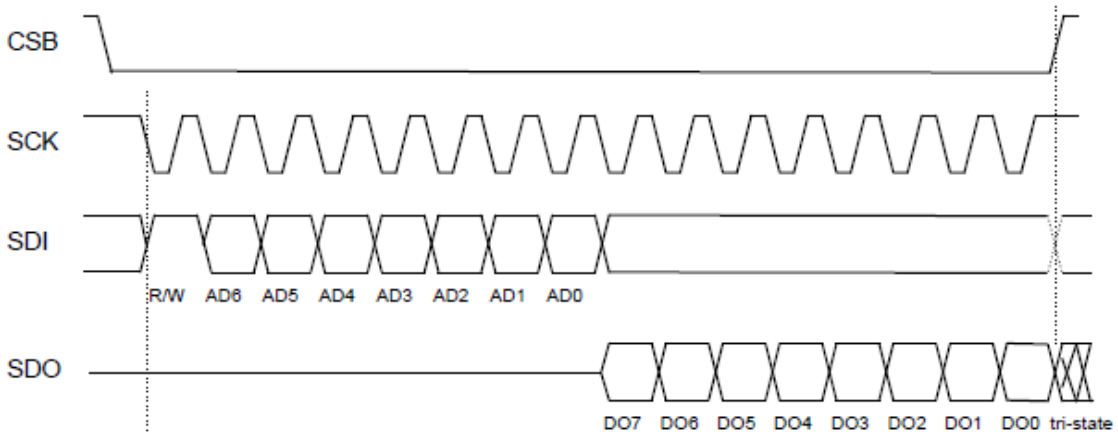


Figure 5-3: 4-wire basic SPI read sequence (mode 11).

The data bits are used as follows:

Bit <15>: Read/write bit. When 0, the data SDI is written into the chip. When 1, the data SDO from the chip is read.

Bits <14:8>: Address AD(6:0).

Bits <7:0>: When in write mode, these are the data SDI which will be written into the address. When in read mode, these are the data SDO which are read from the address.

Multiple read operations are possible by keeping CSB low and continuing the data transfer. Only the first register address has to be written. Addresses are automatically incremented after each read access as long as CSB stays active low.

The principle of multiple read is shown in Figure 5-4.

	Control byte								Data byte								Data byte								Data byte								
Start	RW	Register adress (02h)								Data register - adress 02h								Data register - adress 03h								Data register - adress 04h								Stop
CSB = 0	1	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CSB = 1

Figure 5-4: SPI multiple read.

5.2 Two-Wire Interface (TWI)

The TWI interface uses SCL (= SCx pin, serial clock) and SDA (= SDx pin, serial data input and output) signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

With some exceptions, the TWI interface of the SMI130 is compatible to the I²C specification UM10204 Rev. 03 (19 June 2007), available at http://www.nxp.com:

- The SMI130 supports the I²C standard and fast mode, but only the 7-bit address mode.
- For VDDIO = 1.2 ... 1.8 V the granted voltage output levels are slightly relaxed compared to the specification.
- The internal data hold time (t_{HDDAT}) of 300 ns is not met under all operation conditions. The device achieves a minimum value of 120 ns across process corners and temperature.
- The minimum data fall time (t_F) of ≥ 20 ns cannot be met.
- Only single byte write is supported.
- Detection of a stop condition is not supported. All data transfer protocols are fully operational by means of detecting the start condition only.
- The device does not support the high-impedance mode while VDDIO is tied to GND.
- The device does not perform clock stretching, i.e., clock frequencies may not exceed the one specified in the parameter section, and wait times between subsequent write accesses (as specified in Section 5.3) have to be ensured by the bus master.

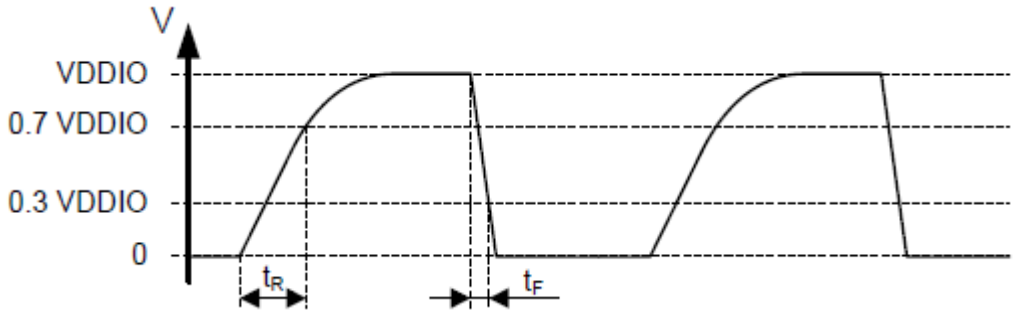


Figure 5-5: Definition of the rise and fall time of TWI signals.

The default TWI address of the SMI130 accelerometer is 0x18 (ACC: 0011000), the one of the gyroscope is 0x68 (GYR: 1101000). It is used if the SDO (1 and 2) pin is pulled to GND. The alternative address (ACC: 0011001 or GYR: 1101001) is selected by pulling the SDO (1 and/or 2) pin to VDDIO.

The TWI timing specification of the SMI130 is given in the table below.

Parameter	Symbol	Min	Max	Units
Clock frequency	f_{SCL}	0	400	kHz
SCL low period	t_{LOW}	1.3		µs
SCL high period	t_{HIGH}	0.6		
SDA setup time	t_{SUDAT}	0.1		
SDA hold time	t_{HDDAT}	0.12		
Setup time for a repeated start condition	t_{SUSTA}	0.6		
Hold time for a start condition	t_{HDSTA}	0.6		
Setup time for a stop condition	t_{SUSTO}	0.6		
Time before a new transmission can start	t_{BUF}	1.3		
Idle time between write accesses normal mode	$t_{IDLE\ wacc\ nm}$	2		
Fall time	t_F	0	300	ns
Rise time (determined by external pull-up resistance)	t_R	20	300	ns

Figure 5-6 shows the definition of the TWI timing given in the table above.

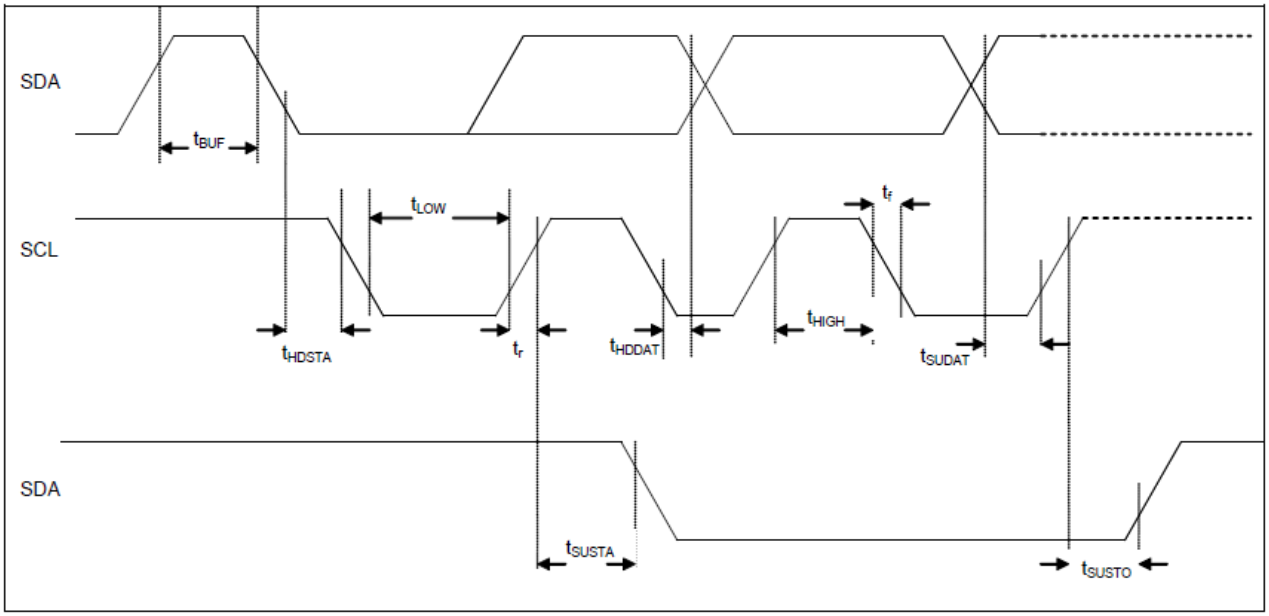


Figure 5-6: SMI130 TWI timing specification.

The TWI protocol works as follows:

START: Data transmission on the bus begins with a high to low transition on the SDA line while SCL is held high (start condition (S) indicated by the TWI bus master). Once the start signal is transferred by the master, the bus is considered busy.

STOP: Each data transfer should be terminated by a stop signal (P) generated by the master. The stop condition is a low to high transition on the SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. It is indicated by an acknowledge bit sent by the receiver. The transmitter must release the SDA line (no pull down) during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

In the following diagrams these abbreviations are used:

S	Start
P	Stop
ACKS	Acknowledge by slave
ACKM	Acknowledge by master
NACKM	Not acknowledge by master
RW	Read / Write

A start (S) immediately followed by a stop (P) (without SCL toggling from VDDIO to GND) is not supported and not recognized by the SMI130.

TWI write access can be used to write a data byte in one sequence.

The sequence begins with a start condition generated by the master, followed by 7 bits of slave address and a write bit (RW = 0). The slave sends an acknowledge bit (ACK = 0) and releases the bus. Then the master sends the one byte register address. The slave again acknowledges the transmission and waits for the 8 bits of data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol. Figure 5-7 shows an example of a TWI write access to the accelerometer.

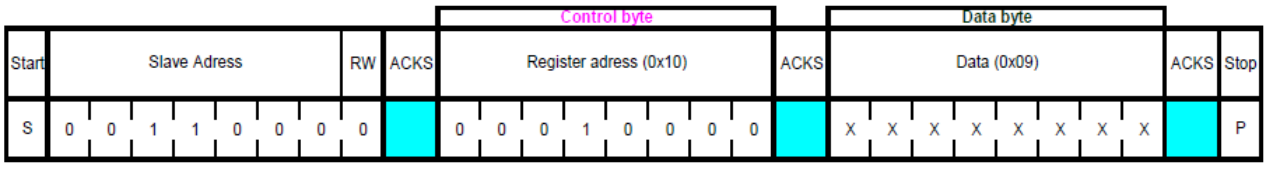


Figure 5-7: Example of a TWI write access to the accelerometer.

TWI read access can be used to read one or multiple data bytes in one sequence.

A read sequence consists of a one-byte TWI write phase followed by the TWI read phase. Both parts of the transmission must be separated by a repeated start condition (Sr). The TWI write phase addresses the slave and sends the register address to be read. After the slave acknowledges the transmission, the master again generates a start condition and sends the slave address together with a read bit (RW = 1). Then the master releases the bus and waits for the data bytes to be read out from the slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACKM (ACK = 1) from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a stop condition and terminate the transmission.

The register address is automatically incremented. Hence, more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the latest TWI write command. By default the start address is set as 0x00. In this way, repetitive multi-byte reads from the same starting address are possible.

In order to prevent the TWI slave from locking the TWI bus, a watchdog timer (WDT) is implemented. The WDT observes internal TWI signals and resets the TWI interface if the bus is locked up. Activity and timer period of the WDT can be configured via bits 2 (*i2c_wdt_en*) and 1 (*i2c_wdt_sel*) in registers ACC 0x34 (BGW_SPI3_WDT) and GYR 0x34 (BGW_SPI3_WDT).

- Writing 1 (0) to *i2c_wdt_en* activates (de-activates) the WDT.
- Writing 0 (1) to *i2c_wdt_se* sets a timer period of 1 ms (50 ms).

Figure 5-8 shows an example of a TWI read access to the accelerometer.

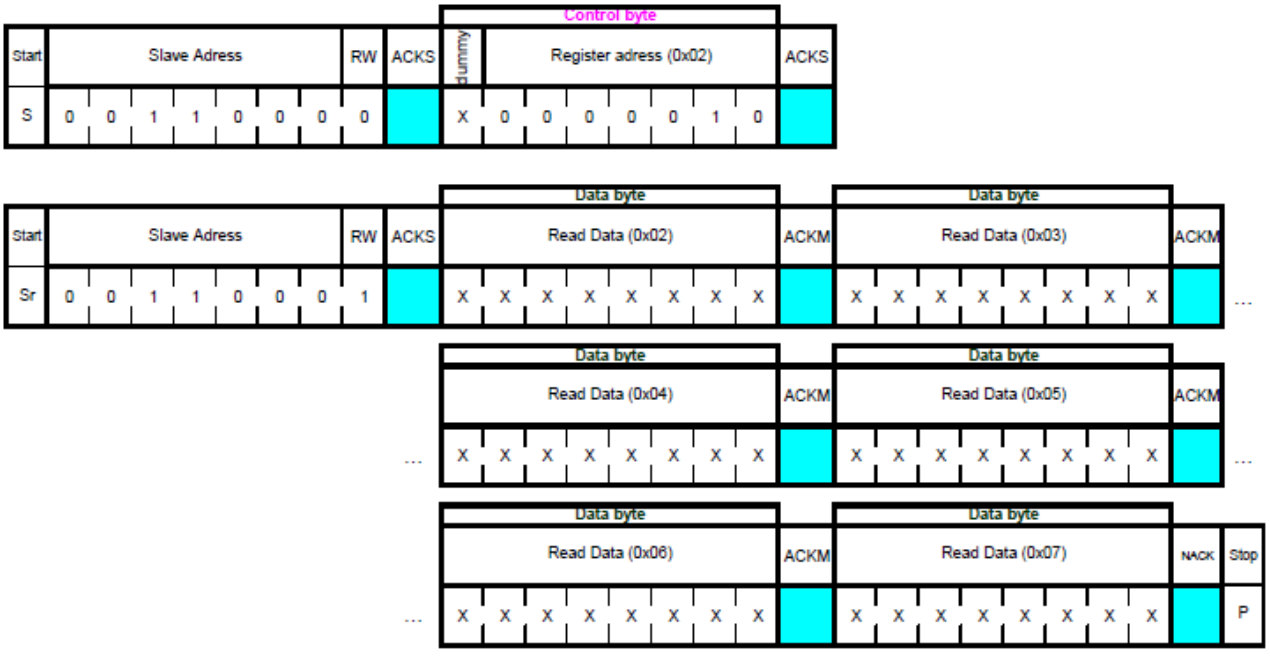


Figure 5-8: Example of a TWI read access to the accelerometer.

Note (Gyroscope Soft Reset):

The SMI130 shows a specific behavior after performing a soft reset of the gyroscope. After carrying out the soft reset, the TWI slave is reset. This releases the bus before completing the command and a NACK is sent instead of an ACK. The user may ignore the first NACK after a soft reset of the gyroscope.

5.3 Access Restrictions (SPI and TWI)

In order to allow for the correct internal synchronization of data written to the SMI130, certain access restrictions apply for consecutive write accesses or a write/read sequence through the SPI and TWI interface.

As illustrated in Figure 5-9, an interface idle time of at least 2 µs is required following a write operation when the device operates.

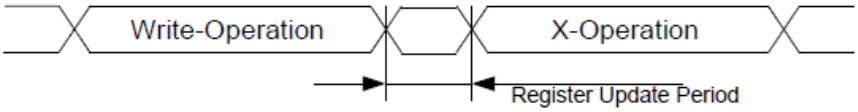


Figure 5-9: Post-write access timing constraints.

5.4 Self-Test

Accelerometer

The self-test feature allows for checking the sensor functionality by applying electrostatic forces to the sensor core instead of external accelerations. By physically deflecting the seismic mass, the entire signal path of the sensor is tested. Activation of the self-test results in a static offset in the acceleration data. Any external acceleration or gravitational force which is applied to the sensor during a self-test will be observed in the sensor output as a superposition of the acceleration and the self-test signal.

Before enabling the self-test, the acceleration measurement range should be set to **8 g**.

The self-test is activated for **each axis separately** by setting bits <1:0> (*self_test_axis*) of register ACC 0x32 (PMU_SELF_TEST) to 01 for the x-axis, 10 for the y-axis or 11 for the z-axis. For *self_test_axis* = 00, the self-test is disabled. The **direction of the deflection** is controlled via bit 2 (*self_test_sign*). The deflection is negative (positive) when setting *self_test_sign* to 0 (1). The amplitude of the deflection has to be set high by setting bit 4 (*self_test_amp*) to 1. When a self-test is performed, only the acceleration data readout value of the selected axis is valid.

ACC 0x32; bits <1:0> *self_test_axis*	**00**	**01**	**10**	**11**
self-test	deactivate self-test	x-axis	y-axis	z-axis

For each axis, a waiting time of 50 ms is mandatory after enabling the self-test.

For a proper interpretation of the self-test signals, it is recommended to perform the self-test for both the positive and the negative direction and to then calculate the difference of the resulting acceleration values. The minimum difference for each axis is shown in the table below. The actually measured signal differences can be significantly larger.

	x-axis	**y-axis**	**z-axis**
minimum difference signal	800 mg	800 mg	400 mg

After performing a self-test, a reset of the device is recommended. If the reset cannot be performed, the following sequence must be kept to prevent unwanted interrupt generation:

1. Disable interrupts.
2. Change parameters of interrupts.
3. Wait for at least 50 ms.
4. Enable desired interrupts.

Gyroscope

A built-in self-test (BIST) has been implemented which provides a quick way to determine if the gyroscope is operational within the specifications.

The BIST uses three parameters for the evaluation of proper device operation:

- Drive voltage regulator
- Sense frontend offset regulator of x-, y- and z-channel
- Quad regulator for x-, y- and z-channel

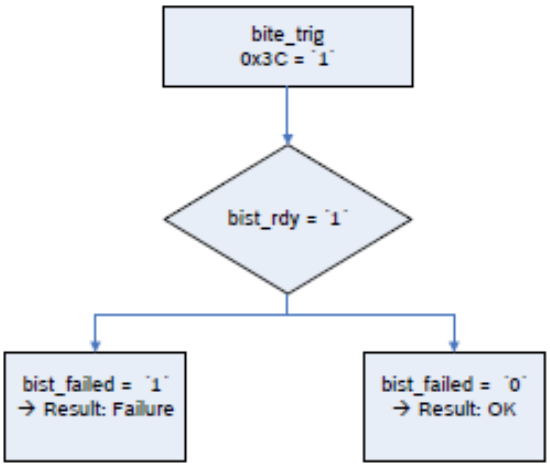


Figure 5-10: SMI130 BIST sequence.

If any of the three parameters is not within the limits, the BIST results in a ‘fail’.

To trigger the BIST, set bit 0 (*trig_bist*) in register GYR 0x3C (BIST) to 1.

Two bits (read-only) have to be checked in register GYR 0x3C (BIST):

- bit 1(*bist_rdy*)
- bit 2 (*bist_fail*)

bist_rdy = 1 indicates that a test was performed. *bist_fail* contains the result of the BIST. *bist_fail* = 1 corresponds to a ‘fail’.

A simple option to check for the sensor status is to read out bit 4 (*rate_ok*) in register GYR 0x3C (BIST). No trigger is needed for this, and proper sensor function is indicated by a 1.

A waiting time of 50 ms is mandatory after enabling the self-test.

Note: In contrast to the self-test of the accelerometer, the BIST of the gyroscope is fully decoupled from the sensing element. This means that the MEMS element is not deflected, and the current state of the MEMS element (e.g. its orientation) has no influence on the result of the BIST.

6 Register Description

6.1 Accelerometer - Register Map

Figure 6-1 shows the register map of the SMI130 accelerometer.

Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Default
0x34						i2c_wdt_en	i2c_wdt_sel		0x00
0x32				self_test_amp		self_test_sign	self_test_axis<1:0>		0x00
0x20					int2_od	int2_lvl			0x05
0x1E			int_src_data						0x00
0x1A	int2_data								0x00
0x17				data_en					0x00
0x14	softreset								0x00
0x13	data_high_bw	shadow_dis							0x00
0x10				bw <4:0>					0x0F
0x0F					range <3:0>				0x03
0x0A	data_int								0x00
0x08	temp <7:0>								0x00
0x07	acc_z_msb <11:4>								0x00
0x06	acc_z_lsb <3:0>							new_data_z	0x00
0x05	acc_y_msb <11:4>								0x00
0x04	acc_y_lsb <3:0>							new_data_y	0x00
0x03	acc_x_msb <11:4>								0x00
0x02	acc_x_lsb <3:0>							new_data_x	0x00
0x00	chip_id <7:0>								0xFA

	w/r
	write only
	ready only
	reserved

Figure 6-1: SMI130 accelerometer register map.

common w/r registers: Application specific settings – in general different from default. After each POR or soft reset, values are reset to default.

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits. They are mapped to a common space of 64 addresses from ACC 0x00 up to ACC 0x3F. Within this range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’ at all. Furthermore it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as ‘reserved’.

Registers with addresses from ACC 0x00 up to ACC 0x0E are read-only. Any attempt to write to these registers will be ignored. There are bits within some registers which trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register ACC 0x14 (BGW_SOFTRESET).

6.1.1 ACC Register 0x00 (BGW_CHIPID)

This register contains the chip identification code.

Name	0x00	BGW_CHIPID		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <3:0>			

chip_id <7:0>: Fixed value 11111010 = FA

6.1.2 ACC Register 0x02 (ACCD_X_LSB)

This register contains the least significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_X_LSB at any time except during power-up.

Name	0x02	ACCD_X_LSB		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_lsb* <3:0>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*undefined*			*new_data_x*

acc_x_lsb <3:0>: Least significant 4 bits of the acceleration x-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_x: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.1.3 ACC Register 0x03 (ACCD_X_MSB)

This register contains the most significant bits of the x-channel acceleration readout value. When reading out x-channel acceleration values, data consistency is guaranteed if the ACCD_X_LSB is read out before the ACCD_X_MSB and *shadow_dis* = 0. In this case, after the ACCD_X_LSB has been read, the value in the ACCD_X_MSB register is locked until the ACCD_X_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_X_MSB at any time except during power-up.

Name	**0x03**	**ACCD_X_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <11:8>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_x_msb* <7:4>			

acc_x_msb <11:4>: Most significant 8 bits of the acceleration x-channel read-back value (two's complement format)

6.1.4 ACC Register 0x04 (ACCD_Y_LSB)

This register contains the least significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_Y_LSB at any time except during power-up.

Name	**0x04**	**ACCD_Y_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_lsb* <3:0>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*undefined*			*new_data_y*

acc_y_lsb <3:0>: Least significant 4 bits of the acceleration y-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_y: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.1.5 ACC Register 0x05 (ACCD_Y_MSB)

This register contains the most significant bits of the y-channel acceleration readout value. When reading out y-channel acceleration values, data consistency is guaranteed if the ACCD_Y_LSB is read out before the ACCD_Y_MSB and *shadow_dis* = 0. In this case, after the ACCD_Y_LSB has been read, the value in the ACCD_Y_MSB register is locked until the ACCD_Y_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_Y_MSB at any time except during power-up.

Name	**0x05**	**ACCD_Y_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <11:8>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_y_msb* <7:4>			

acc_y_msb <11:4>: Most significant 8 bits of acceleration y-channel read-back value (two's complement format)

6.1.6 ACC Register 0x06 (ACCD_Z_LSB)

This register contains the least significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_Z_LSB at any time except during power-up.

Name	**0x06**	**ACCD_Z_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_lsb* <3:0>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*undefined*			*new_data_z*

acc_z_lsb <3:0>: Least significant 4 bits of the acceleration z-channel read-back value (two's complement format)

undefined: Random data, to be ignored

new_data_z: 0: acceleration value has not been updated since it has been read out last
1: acceleration value has been updated since it has been read out last

6.1.7 ACC Register 0x07 (ACCD_Z_MSB)

This register contains the most significant bits of the z-channel acceleration readout value. When reading out z-channel acceleration values, data consistency is guaranteed if the ACCD_Z_LSB is read out before the ACCD_Z_MSB and *shadow_dis* = 0. In this case, after the ACCD_Z_LSB has been read, the value in the ACCD_Z_MSB register is locked until the ACCD_Z_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Acceleration data may be read from register ACCD_Z_MSB at any time except during power-up.

Name	**0x07**	**ACCD_Z_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <11:8>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*acc_z_msb* <7:4>			

acc_z_msb <11:4>: Most significant 8 bits of the acceleration z-channel read-back value (two's complement format)

6.1.8 ACC Register 0x08 (TEMP)

This register contains the current chip temperature as a 8 bit data word in two's complement format. The slope is typically 0.5K/LSB.

Name	**0x08**	**TEMP**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <3:0>			

temp <7:0>: Temperature value (two's complement format)

***temp* <7:0>**	**Temperature [°C]**
01111111	87.5
...	...
00000010	25
...	...
10000000	-40

6.1.9 ACC Register 0x0A (INT_STATUS_1)

This register contains the interrupt status flag *data_int* of the new data interrupt.

The new data interrupt allows for synchronous reading of acceleration data. It is generated after a new value of z-axis acceleration data has been stored in the data register.

The interrupt is cleared automatically when the next data acquisition cycle starts. The interrupt status is 0 for a minimum of 50 µs. It is fixed to the non-latched mode.

The interrupt function associated with a specific status flag has to be enabled via setting bit 4 (*data_en*) in register ACC 0x17 (INT_EN_1) to 1.

Name	**0x0A**	**INT_STATUS_1**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*data_int*	*reserved*		

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*reserved*			

data_int: Data ready interrupt status
0: inactive
1: active

reserved: Random data, to be ignored

6.1.10 ACC Register 0x0F (PMU_RANGE)

This register allows for the selection of the accelerometer g-range.

Name	**0x0F**	**PMU_RANGE**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1
Content	*range* <3:0>			

range <3:0>: Selection of the accelerometer g-range

		Resolution [LSB / g]
0011:	±2 g	1024
0101:	±4 g	512
1000:	±8 g	256
1100:	±16 g	128

All other settings: reserved (do not use)

reserved: Write 0

6.1.11 ACC Register 0x10 (PMU_BW)

This register allows for the selection of the acceleration data filter bandwidth.

Name	0x10	PMU_BW		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*bw* <4>

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1
Content	*bw* <3:0>			

bw <4:0>: Selection of the data filter bandwidth:

00xxx:	reserved	01010:	31.25 Hz	01101:	250 Hz
01000:	7.81 Hz	01011:	62.50 Hz	01110:	500 Hz
01001:	15.63 Hz	01100:	125.00 Hz	01111:	1000 Hz
				1xxxx:	reserved

reserved: Write 0

6.1.12 ACC Register 0x13 (ACCD_HBW)

This register controls the acceleration data acquisition and data output format.

Name	0x13	ACCD_HBW		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*data_high_bw*	*shadow_dis*	*reserved*	

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_high_bw: Data-read from the acceleration data registers
1: unfiltered
0: filtered

shadow_dis: The shadowing mechanism for the acceleration data output registers. When shadowing is enabled, the content of the acceleration data component in the MSB register is locked when the component in the LSB is read, thereby ensuring the integrity of the acceleration data during read-out. The lock is removed when the MSB is read.
1: disable
0: enable

reserved: Write 0

6.1.13 ACC Register 0x14 (BGW_SOFTRESET)

This register controls the user triggered reset of the sensor.

Name	0x14	BGW_SOFTRESET		
Bit	7	6	5	4
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

Bit	3	2	1	0
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

softreset: Writing 0xB6 to the register triggers a reset. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. Please note that all application specific settings which are not equal to the default settings (refer to the accelerometer register map in Section 6.1) must be reconfigured to their designated values.

6.1.14 ACC Register 0x17 (INT_EN_1)

This register enables the new data interrupt. See bit *data_int* in register ACC 0x0A (INT_STATUS_1).

Name	0x17	INT_EN_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*data_en*

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_en: Data ready interrupt
0: disabled
1: enabled

reserved: Write 0

6.1.15 ACC Register 0x1A (INT_MAP_1)

This register controls the interrupt signals to be mapped to the INT2 pin.

Name	0x1A	INT_MAP_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*int2_data*	*reserved*		

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

int2_data: Map data ready interrupt to INT2 pin
0: disabled
1: enabled

reserved: Write 0

6.1.16 ACC Register 0x1E (INT_SRC)

This register controls the data source definition for interrupts with selectable data source.

Name	0x1E	INT_SRC		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*		*int_src_data*	*reserved*

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

int_src_data: Data for new data interrupt
0: filtered
1: unfiltered

reserved: Write 0

6.1.17 ACC Register 0x20 (INT_OUT_CTRL)

This register controls the electrical behavior and configuration of the interrupt pins.

Name	0x20	INT_OUT_CTRL		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	n/a	n/a	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	1	0	1
Content	*int2_od*	*int2_lvl*	*reserved*	

int2_od: Behavior for the INT2 pin
0: push-pull
1: open drain

int2_lvl: Level for the INT2 pin:
0: active low
1: active high

reserved: Write 0

6.1.18 ACC Register 0x32 (PMU_SELF_TEST)

This register contains the settings for the sensor self-test configuration and trigger.

Name	0x32	PMU_SELF_TEST		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*self_test_amp*

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*self_test_sign*	*self_test_axis* <1:0>	

self_test_amp: Select the amplitude of the self-test deflection
1: high
0: low (default)

self_test_sign: Select the sign of self-test excitation
1: positive
0: negative

self_test_axis <1:0>: Select the axis to be self-tested
00: self-test disabled
01: x-axis
10: y-axis
11: z-axis
When a self-test is performed, only the acceleration data readout value of the selected axis is valid; after the self-test has been enabled, a delay of at least 50 ms is necessary for the read-out value to settle.

reserved: Write 0

6.1.19 ACC Register 0x34 (BGW_SPI3_WDT)

This register contains settings for the digital interfaces.

Name	**0x34**	**BGW_SPI3_WDT**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*i2c_wdt_en*	*i2c_wdt_sel*	*reserved*

i2c_wdt_en: Watchdog timer at the SDA pin in TWI mode
0: disable
1: enable

i2c_wdt_sel: Watchdog timer period
0: 1 ms
1: 50 ms

reserved: Write 0

6.2 Gyroscope – Register Map

Figure 6-2 shows the register map of the SMI130 gyroscope.

Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Default
0x3C				rate_ok		bist_fail	bist_rdy	trig_bist	0x00
0x34						i2c_wdt_en	i2c_wdt_sel		0x00
0x18								int1_data	0x00
0x16							int1_od	int1_lvl	0x0F
0x15	data_en								0x00
0x14	softreset								0x00
0x13	data_high_bw	shadow_dis							0x00
0x10	bw <3:0>								0x80
0x0F	range <2:0>								0x00
0x0A	data_int								0x00
0x08	temp <7:0>								0x00
0x07	rate_z_msb <15:8>								0x00
0x06	rate_z_lsb <7:0>								0x00
0x05	rate_y_msb <15:8>								0x00
0x04	rate_y_lsb <7:0>								0x00
0x03	rate_x_msb <15:8>								0x00
0x02	rate_x_lsb <7:0>								0x00
0x00	chip_id <7:0>								0x0F

	w/r
	write only
	ready only
	reserved

Figure 6-2: SMI130 gyroscope register map.

common w/r registers: Application specific settings – in general different from default. After each POR or soft reset, values are reset to default.

The entire communication with the device is performed by reading from and writing to registers. Registers have a width of 8 bits. They are mapped to a common space of 64 addresses from GYR 0x00 up to GYR 0x3C. Within this range range some registers are either completely or partially marked as ‘reserved’. Any reserved bit is ignored when it is written and no specific value is guaranteed when the bit is read. It is recommended not to use registers which are completely marked as ‘reserved’ at all. Furthermore it is recommended to mask out (logical and with zero) reserved bits of registers which are partially marked as ‘reserved’.

Registers with addresses from GYR 0x00 up to GYR 0x0E are read-only. Any attempt to write to these registers will be ignored. There are bits within some registers which trigger internal sequences. These bits are configured for write-only access and read as 0. An example for such a write-only access is the entire register GYR 0x14 (BGW_SOFTRESET).

6.2.1 GYR Register 0x00 (CHIP_ID)

This register contains the chip identification code.

Name	0x00	CHIP_ID		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*chip_id* <3:0>			

chip_id <7:0>: Fixed value 00001111 = 0x0F

6.2.2 GYR Register 0x02 (RATE_X_LSB)

This register contains the least significant bits of the x-channel angular rate readout value. When reading out x-channel angular rate values, data consistency is guaranteed if the RATE_X_LSB is read out before the RATE_X_MSB and *shadow_dis* = 0. In this case, after the RATE_X_LSB has been read, the value in the RATE_X_MSB register is locked until the RATE_X_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_X_LSB at any time except during power-up.

Name	0x02	RATE_X_LSB		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_x_lsb* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_x_lsb* <3:0>			

rate_x_lsb <7:0>: Least significant 8 bits of the rate x-channel read-back value (two's complement format)

6.2.3 GYR Register 0x03 (RATE_X_MSB)

This register contains the most significant bits of the x-channel angular rate readout value. When reading out x-channel angular rate values, data consistency is guaranteed if the RATE_X_LSB is read out before the RATE_X_MSB and *shadow_dis* = 0. In this case, after the RATE_X_LSB has been read, the value in the RATE_X_MSB register is locked until the RATE_X_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_X_MSB at any time except during power-up.

Name	**0x03**	**RATE_X_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_x_msb* <15:12>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_x_msb* <11:8>			

rate_x_msb <15:8>: Most significant 8 bits of the rate x-channel read-back value (two's complement format)

6.2.4 GYR Register 0x04 (RATE_Y_LSB)

This register contains the least significant bits of the y-channel angular rate readout value. When reading out y-channel angular rate values, data consistency is guaranteed if the RATE_Y_LSB is read out before the RATE_Y_MSB and *shadow_dis* = 0. In this case, after the RATE_Y_LSB has been read, the value in the RATE_Y_MSB register is locked until the RATE_Y_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_Y_LSB at any time except during power-up.

Name	**0x04**	**RATE_Y_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_y_lsb* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_y_lsb* <3:0>			

rate_y_lsb <7:0>: Least significant 8 bits of the rate y-channel read-back value (two's complement format)

6.2.5 GYR Register 0x05 (RATE_Y_MSB)

This register contains the most significant bits of the y-channel angular rate readout value. When reading out y-channel angular rate values, data consistency is guaranteed if the RATE_Y_LSB is read out before the RATE_Y_MSB and *shadow_dis* = 0. In this case, after the RATE_Y_LSB has been read, the value in the RATE_Y_MSB register is locked until the RATE_Y_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_Y_MSB at any time except during power-up.

Name	**0x05**	**RATE_Y_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_y_msb* <15:12>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_y_msb* <11:8>			

rate_y_msb <15:8>: Most significant 8 bits of the rate y-channel read-back value (two's complement format)

6.2.6 GYR Register 0x06 (RATE_Z_LSB)

This register contains the least significant bits of the z-channel angular rate readout value. When reading out z-channel angular rate values, data consistency is guaranteed if the RATE_Z_LSB is read out before the RATE_Z_MSB and *shadow_dis* = 0. In this case, after the RATE_Z_LSB has been read, the value in the RATE_Z_MSB register is locked until the RATE_Z_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_Z_LSB at any time except during power-up.

Name	**0x06**	**RATE_Z_LSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_z_lsb* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_z_lsb* <3:0>			

rate_z_lsb <7:0>: Least significant 8 bits of the rate z-channel read-back value (two's complement format)

6.2.7 GYR Register 0x07 (RATE_Z_MSB)

This register contains the most significant bits of the z-channel angular rate readout value. When reading out z-channel angular rate values, data consistency is guaranteed if the RATE_Z_LSB is read out before the RATE_Z_MSB and *shadow_dis* = 0. In this case, after the RATE_Z_LSB has been read, the value in the RATE_Z_MSB register is locked until the RATE_Z_MSB has been read. This condition is inherently fulfilled if a burst-mode read access is performed. Angular rate data may be read from register RATE_Z_MSB at any time except during power-up.

Name	**0x07**	**RATE_Z_MSB**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_z_msb* <15:12>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*rate_z_msb* <11:8>			

rate_z_msb <15:8>: Most significant 8 bits of the rate z-channel read-back value (two's complement format)

6.2.8 GYR Register 0x08 (TEMP)

This register contains the current chip temperature as a 8 bit data word in two's complement format. The slope is typically 0.5 K/LSB.

Name	**0x08**	**TEMP**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <7:4>			

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	0	0	0	0
Content	*temp* <3:0>			

temp <7:0>: Temperature value (two's complement format)

***temp* <7:0>**	**Temperature [°C]**
01111111	87.5
...	...
00000010	25
...	...
10000000	-40

6.2.9 GYR Register 0x0A (INT_STATUS_1)

This register contains the interrupt status flag *data_int* of the new data interrupt.

The new data interrupt allows for synchronous reading of angular rate data. It is generated after storing a new z-axis angular rate value in the data register.

The interrupt clears automatically after 280 – 400 µs depending on settings.

Note: The interrupt mode of the new data interrupt is non-latched.

The interrupt function associated with the status flag has to be enabled via setting bit 7 (*data_en*) in register GYR 0x15 (INT_EN_0) to 1.

Name	**0x0A**	**INT_STATUS_1**		
Bit	7	6	5	4
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*data_int*	*reserved*		

Bit	3	2	1	0
Read/Write	R	R	R	R
Reset Value	n/a	n/a	n/a	n/a
Content	*reserved*			

data_int: Data ready interrupt status
0: inactive
1: active

reserved: Random data, to be ignored

6.2.10 GYR Register 0x0F (RANGE)

This register allows for the selection of the gyroscope angular rate measurement range.

Name	**0x0F**	**RANGE**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*range* <2:0>		

range <2:0>: Selection of the gyroscope angular rate range

		Resolution
000:	±2000 °/s	16.4 LSB/°/s
001:	±1000 °/s	32.8 LSB/°/s
010:	±500 °/s	65.6 LSB/°/s
011:	±250 °/s	131.2 LSB/°/s
100:	±125 °/s	262.4 LSB/°/s
Others:	reserved	

reserved: Write 0

6.2.11 GYR Register 0x10 (BW)

This register allows for the selection of the rate data filter bandwidth.

Name	**0x10**	**BW**		
Bit	7	6	5	4
Read/Write	R	R/W	R/W	R/W
Reset Value	1	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*bw* <3:0>			

range <3:0>: Selection of the data filter bandwidth

0111:	32 Hz
0110:	64 Hz
0101:	12 Hz
0100:	23 Hz
0011:	47 Hz
0010:	116 Hz
0001:	230 Hz
0000:	unfiltered (523 Hz)
Others:	unused/reserved

reserved: Write 0

6.2.12 GYR Register 0x13 (RATE_HBW)

This register controls the angular rate data acquisition and data output format.

Name	0x13	RATE_HBW		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*data_high_bw*	*shadow_dis*	*reserved*	

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_high_bw: Data-read from the rate data registers
1: unfiltered
0: filtered

shadow_dis: The shadowing mechanism for the rate data output registers. When shadowing is enabled, the content of the rate data component in the MSB register is locked when the component in the LSB is read, thereby ensuring the integrity of the rate data during read-out. The lock is removed when the MSB is read.
1: disable
0: enable

reserved: Write 0

6.2.13 GYR Register 0x14 (BGW_SOFTRESET)

This register controls the user triggered reset of the sensor.

Name	0x14	BGW_SOFTRESET		
Bit	7	6	5	4
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

Bit	3	2	1	0
Read/Write	W	W	W	W
Reset Value	0	0	0	0
Content	*softreset*			

softreset: Writing 0xB6 to the register triggers a reset. Other values are ignored. After a delay, all user configuration settings are overwritten with their default values. Please note that all application specific settings which are not equal to the default settings (refer to the register map in Section 6.2) must be reconfigured to their designated values.

6.2.14 GYR Register 0x15 (INT_EN_0)

This register enables the new data interrupt. See bit *data_int* in register GYR 0x0A (INT_STATUS_1).

Name	0x15	INT_EN_0		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*data_en*	*reserved*		

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

data_en: New data interrupt
0: disabled
1: enabled

reserved: Write 0

6.2.15 GYR Register 0x16 (INT_EN_1)

This register contains interrupt pin configurations.

Name	0x16	INT_EN_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1
Content	*reserved*		*int1_od*	*int1_lvl*

int1_od: Behavior for INT1 pin
0: push-pull
1: open drain

int1_lvl: Active level for INT1 pin
0: disabled
1: enabled

reserved: Write 0

6.2.16 GYR Register 0x18 (INT_MAP_1)

This register controls if interrupt signals are mapped to the INT1 pin.

Name	0x18	INT_MAP_1		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			*int1_data*

int1_data: Map new data interrupt to the INT1 pin
0: disabled
1: enabled

reserved: Write 0

6.2.17 GYR Register 0x34 (BGW_SPI3_WDT)

This register contains settings for the digital interfaces.

Name	0x34	BGW_SPI3_WDT		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*			

Bit	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0
Content	*reserved*	*i2c_wdt_en*	*i2c_wdt_sel*	*reserved*

i2c_wdt_en: Watchdog timer at the SDA pin in TWI mode
0: disable
1: enable

i2c_wdt_sel: Watchdog timer period
0: 1 ms
1: 50 ms

reserved: Write 0

6.2.18 GYR Register 0x3C (BIST)

This register contains the built-in self-test (BIST) options – see Chapter 5.4.

Name	**0x3C**	**BIST**		
Bit	7	6	5	4
Read/Write	R/W	R/W	R/W	R
Reset Value	0	0	0	0
Content	*reserved*			*rate_ok*

Bit	3	2	1	0
Read/Write	R/W	R	R	W
Reset Value	0	0	0	0
Content	*reserved*	*bist_fail*	*bist_rdy*	*trig_bist*

rate_ok: 1: indicates proper sensor function, no trigger is needed for this

bist_fail: Contains the fail flag

bist_rdy: If *bist_rdy* is 1 and *bist_fail* is 0, the result of the BIST is ok, meaning “sensor ok”. If *bist_rdy* is 1 and *bist_fail* is 1, the result of the BIST is not ok, meaning “sensor values not in expected range”.

trig_bist: Write 1: perform the BIST

reserved: Write 0

7 Handling and Storage

Sensors with visible damages (housing, connectors, pins, etc.) and sensors which might have exceeded the absolute maximum ratings (e.g. dropped down from a height of more than 120 cm onto a hard surface) must not be mounted in the vehicle. These sensors must be scrapped.

7.1 Moisture Sensitivity Level (MSL)

The moisture sensitivity level (MSL) of BOSCH SMI130 corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitivity Surface Mount Devices"

The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e., reflow soldering with a peak temperature up to 260°C.

7.2 Mounting Recommendations

MEMS sensors in general are high-precision measurement devices which consist of electronic as well as mechanical structures. BOSCH sensor devices are designed for precision, efficiency and mechanical robustness.

However, in order to achieve best possible results of your design, the following recommendations should be taken into consideration when mounting the sensor on a printed circuit board (PCB).

In order to evaluate and optimize the considered placement position of the sensor on the PCB, it is recommended to use additional tools during the design in phase, e.g.:

- Regarding thermal aspects: infrared camera
- Regarding mechanical stress: warpage measurements and/or FEM-simulations
- Regarding shock robustness: drop test of the devices after soldering on the target application PCB

Recommendations in Detail

- It is recommended to keep a reasonable distance between the sensor mounting location on the PCB and the critical points described in the following examples. The exact value for a "reasonable distance" depends on many customer specific variables and must therefore be determined case by case.
- It is generally recommended to minimize the PCB thickness (recommended: ≤0.8 mm) since a thin PCB shows less intrinsic stress, e.g. while being bent.
- It is not recommended to place the sensor directly under or next to push-button contacts as this can result in mechanical stress.
- It is not recommended to place the sensor in direct vicinity of extremely hot spots regarding temperature (e.g. a µController or a graphic chip) as this can result in heating up the PCB and consequently also of the sensor.

- It is not recommended to place the sensor in direct vicinity of a mechanical stress maximum (e.g. in the center of a diagonal crossover). Mechanical stress can lead to bending of the PCB and the sensor.
- Do not mount the sensor too closely to a PCB anchor point where the PCB is attached to a shelf (or similar) as this could also result in mechanical stress. To reduce potential mechanical stress, minimize redundant anchor points and/or loosen respective screws.
- Avoid mounting the sensor in areas where resonant amplitudes (vibrations) of the PCB are likely or to be expected.
- Please avoid partial coverage of the sensor by any kind of (epoxy) resin, as this can possibly result in mechanical stress.
- Avoid mounting (and operation) of the sensor in the vicinity of strong magnetic, strong electric and/or strong infrared radiation fields (IR).
- Avoid electrostatic charging of the sensor and of the device in which the sensor is mounted.

In case you have any questions regarding the mounting of the sensor on your PCB or the evaluation and/or optimization of the considered placement position of the sensor on your PCB, do not hesitate to contact us.

If the above mentioned recommendations cannot be realized appropriately, a specific in-line offset-calibration after placement of the device onto your PCB might help to minimize potentially remaining effects.

7.3 Soldering Guidelines

Repair and manual soldering of the sensor is not permitted.

7.3.1 Reflow Soldering Recommendation for Sensors in LGA Package

Please make sure that the edges of the LGA substrate of the sensor are free of solder material. Avoid solder material forming a high meniscus covering the edge of the LGA substrate (see Figure 7-1).

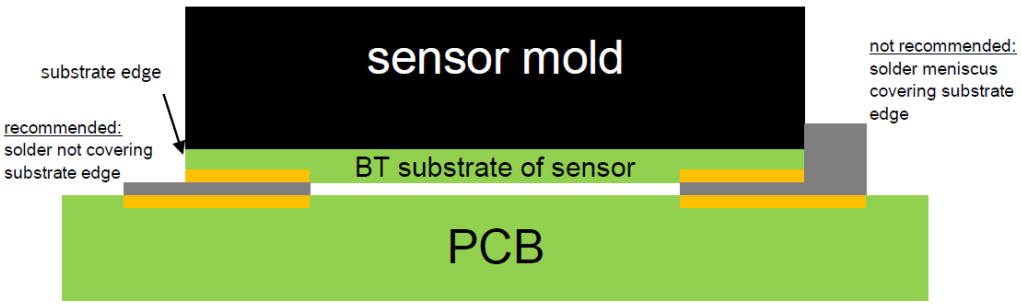


Figure 7-1: Reflow soldering recommendation.

7.3.2 Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_{Smax} to T_p)	3 °C/s max.
Preheat - Temperature min (T_{Smin}) - Temperature max (T_{Smax}) - Time (t_{Smin} to t_{Smax})	 150 °C 200 °C 60 – 180 s
Time maintained above: - Temperature (T_L) - Time (t_L)	 217 °C 60 s – 150 s
Peak classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (t_p)	20 s – 40 s
Ramp-down rate	6 °C/s max.
Time 25 °C to peak temperature	8 min max.

Note: All temperatures refer to the topside of package, measured on the package body surface.

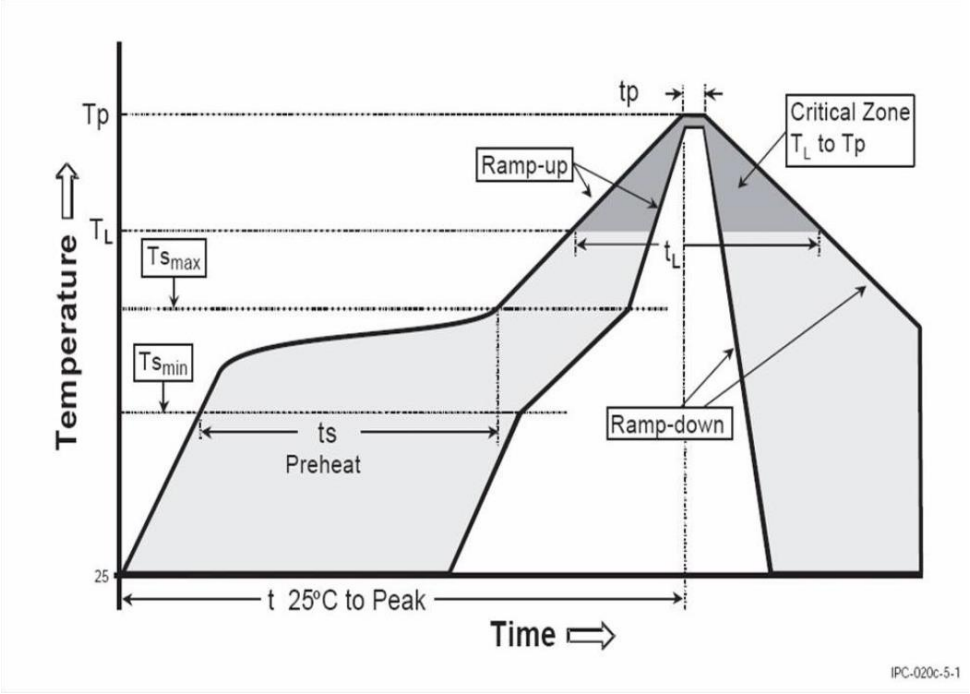


Figure 7-2: Soldering profile.

7.3.3 Multiple Reflow Soldering Cycles

The product can withstand up to 3 reflow soldering cycles in total.

This could be a situation where a PCB is mounted with devices from both sides (i.e., 2 reflow cycles necessary) and where, in the next step, an additional re-work cycle could be required (1 reflow).

7.4 Tape on Reel

7.4.1 Tape on Reel Specification

The SMI130 is shipped in a standard cardboard box.
The box dimensions for one reel are L x W x H = 35 cm x 35 cm x 6 cm.
SMI130 quantity: 5000 pcs per reel. Please handle with care.

Tape dimensions:

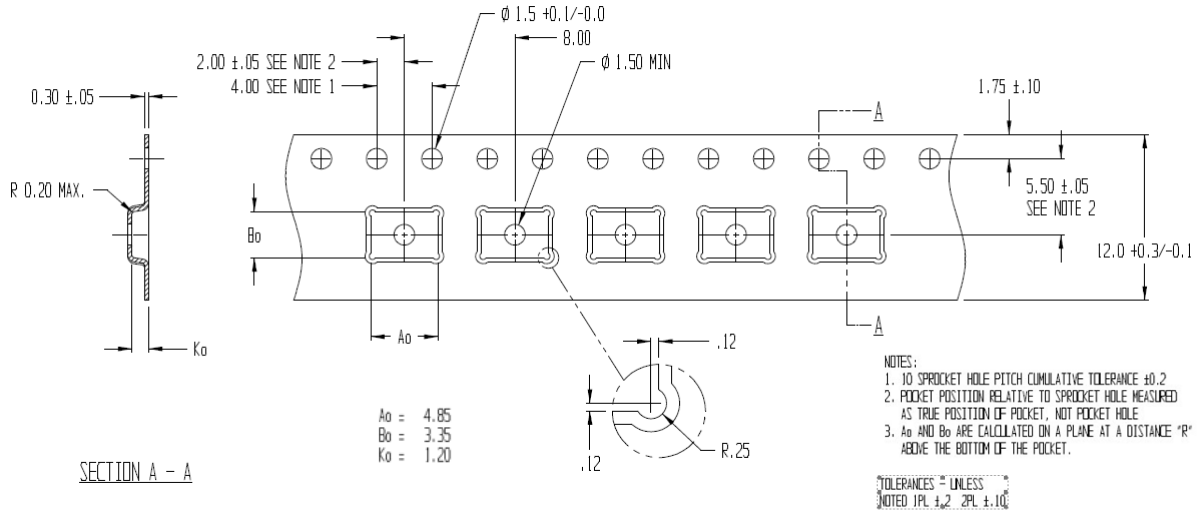
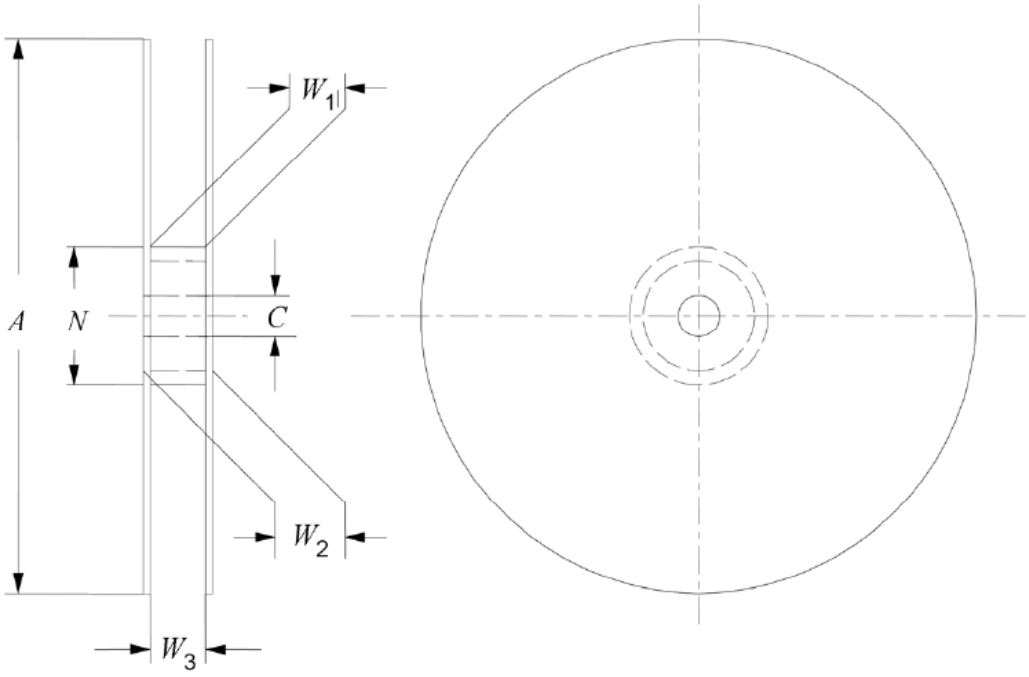


Figure 7-3: Tape dimensions in mm.

Reel dimensions:



Parameter	Meaning	Dimensions [mm]
W (not depicted)	tape width	12
A	reel diameter	330
N	hub diameter	100
W_1	inner width of reel	12.4 +2
W_2	total width of reel	18.4
W_3, min	inner width of reel, minimum	11.9
W_3, max	inner width of reel, maximum	15.4

Details on hub hole dimension C:

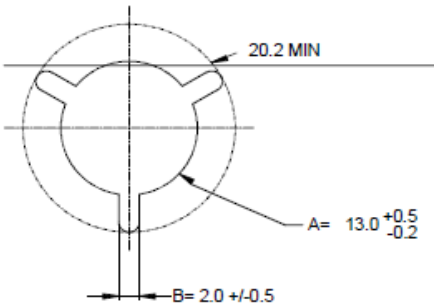


Figure 7-4: Reel dimensions in mm.

7.4.2 Orientation within the Reel

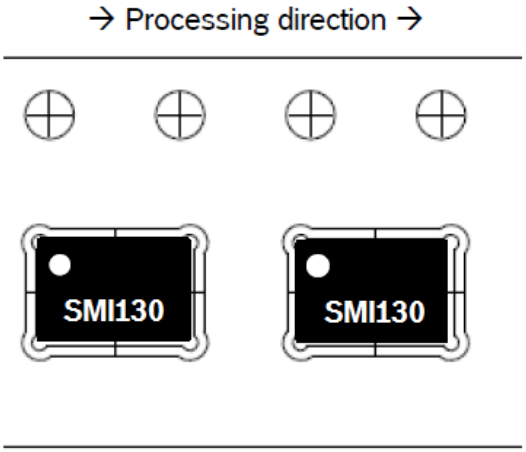


Figure 7-5: Orientation of the SMI130 devices relative to the tape.

7.5 Further Important Mounting and Assembly Recommendations

The SMI130 is designed to sense angular rates and accelerations with high accuracy even at low amplitudes and contains highly sensitive structures inside the sensor element. The MEMS sensor can tolerate mechanical shocks up to several thousand g's. However, these limits might be exceeded in conditions with extreme shock loads such as e.g. hammer blow on or next to the sensor, dropping the sensor onto hard surfaces etc.

We strongly recommend to avoid any g forces beyond the limits specified in the data sheet during transport, handling and mounting of the sensors in a defined and qualified installation process.

This device has built-in protections against high electrostatic discharges or electric fields (2 kV HBM); however, anti-static precautions should be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be connected to a defined logic voltage level.

8 Test Specifications

8.1 Environmental Safety

The SMI130 sensor meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also:

Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Halogen content

The SMI130 is halogen-free. For more details on the analysis results, please contact your Bosch representative.

8.2 Qualification

The SMI130 passed the following qualification: AEC-Q100 grade 3.

9 Legal Disclaimer

Assessment of Products Returned from Field

Returned products are considered good if they fulfill the specifications / test data for 0-mileage and field listed in this document.

Engineering Samples

Engineering samples are marked with (e) or (E). Samples may vary from the valid technical specifications of the series product contained in this data sheet. Therefore, they are not intended or fit for resale to third parties or for use in end products. Their sole purpose is internal client testing. The testing of an engineering sample may in no way replace the testing of a series product. Bosch assumes no liability for the use of engineering samples. The purchaser shall indemnify Bosch from all claims arising from the use of engineering samples.

Product Usage

The SMI130 is tested and qualified according to Section 8. The SMI130 only has to be used within the parameters of this product data sheet. In particular, the SMI130 is not fit for use in life-sustaining or safety sensitive systems. Safety sensitive systems are those for which a malfunction may lead to bodily harm or significant property damage. The resale and/or use of products are at the purchaser's own risk and responsibility. The examination of the SMI130 is the sole responsibility of the purchaser.

The purchaser shall indemnify Bosch from all third party claims arising from any product use not covered by the parameters of this product data sheet or not approved by Bosch and reimburse Bosch for all costs in connection with such claims.

The purchaser must monitor the market for the purchased products, particularly with regard to product safety, and inform Bosch without delay of all security relevant incidents.

Application Examples and Hints

With respect to any application examples, advice, normal values, and/or any information regarding the application of the device, Bosch hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights or copyrights of any third party. The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. They are provided for illustrative purposes only and no evaluation regarding infringement of intellectual property rights or copyrights or regarding functionality, performance or error has been made.