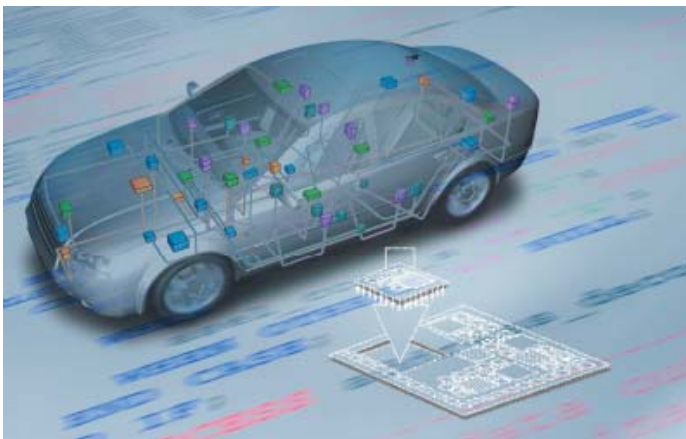# Automotive Electronics
Product Information
Generic Timer Module (GTM) IP

BOSCH

Invented for life

Customer benefits:
- Complex timer IP for various application domains and classes.
- Easy integration due to generic interfaces and hierarchical architecture.
- Scalable and configurable architecture.
- SystemC model support for in-system verification and early software development.

Features
- Counters (free running and reset counter)
- 3 global time bases representing time and/or angle
- Multi-action capture/compare
- PWM input processing (period, duty cycle, time stamps)
- Complex PWM output functions
- Digital phase locked loop (DPLL) for angle base generation and angle prediction
- Input signal filtering
- BLDC support

General characteristics

GTM is not just a timer:
- It also does arithmetics for signal processing.
- Most of the functions are performed in parallel with dedicated HW units (such as digital signal processing ICs).
- GTM features programmable Multi Channel Sequencer (MCS)with a RISC-like instruction set and deterministic task execution.
- No latency challenge since most of the functions run in parallel.

GTM reduces the CPU load:
- No need for low-latency interrupts.
- In low-end projects, CPU can run with slow clock which results in low power dissipation and low EME.
- In high-end projects where even 200 MHz multi-core CPUs normally reach their performance limit, GTM allows for more functionality.
- Less data traffic between CPU and GTM thanks to dedicated RAM for FIFOs, programmable Multi Channel Sequencer (MCS) and dedicated engine position evaluation HW.

GTM functionality

1. Engine Position Evaluation
- Edge processing with very low (< 5 μs) and jitter-free dead time.
- Hardware implemented, sophisticated angle prediction algorithms allow for low end applications with minimal μC load - even at high engine speed.
- Hardware implemented angle-minus-time event prediction for complex adaptive functions support cheap mechanics in low end projects with very low CPU load.

2. PWM Generation

- Up to 192 PWM generators.
- Resolution of >12 bit at any frequency.
- Synchronous update thanks to shadow registers.
- Immediate update due to GE- or LE comparators.
- Highest / lowest frequency > 1000000. No need for a priori frequency range selection. Any frequency can be generated on the fly.
- Coherent update mechanism for up to 8 PWM generators
- Configurable trigger mechanism for up to 2*96 PWM generators.

3. Complex Waveform Generation

- Up to 96 Outputs (within the 192 PWM outputs).
- 24 bit arithmetics.
- Data may come from FIFOs, ring buffers or programmable cores with little or no CPU interaction.
- Works on time and/or angle domain.
- Supports generation of complex output sequences.
- Complex logical combination of output signals

4. **Programmable** Multi Channel Sequencer (MCS)

- Up to 8 programmable cores with up to 32 channels each, working fully in parallel with no CPU load.
- RISC-like instruction set.
- Determinstic task execution without interference by other tasks
- Integrated RAM for program and data.
- Support of direct interaction between all channels within a programmable core.
- Support of indirect interaction between channels of different programmable Multi Channel Sequencer (MCS).
- Close interaction with CPU ("live-update").
- Supports generation of complex output sequences.
- Possibility to sum up input periods for increased precision.
- Interrupt generation at any desired timing.
- Other complex functions like windowing possible by hardware.

5. PWM evaluation and signal detection

- Support of up to 64 Inputs.
- Digital 24 bit filter for every input. Filtered input level available to SW.
- Independent filter timings and strategies for rising and falling edge.
- Synchronous capture of duty-cycle and period, 24 bit resolution.
- Edge counter in hardware.
- Timeout detection for every input.
- Works on time and/or angle domain.

6. Motor Control

- BLDC support.
- PMSM's support.
- Hardware deadtime generation
- Configurable emergency shut-off

Deliverables

- Module implementation
- Basic software
- Test environment (test bench and integration tests)
- SystemC executable-Model for in-system verification and early software development.
- Documentation including specification, integration guide, application notes and verification reports.