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Use of DBARCs Beyond Implant

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Almost a decade ago, the integrated circuit (IC) industry realized that traditional implant layers required new technology to achieve the specifications of the shrinking design rules and increased topography effects. In response, developer-soluble bottom anti-reflective coatings (DBARCs) were introduced as a solution. DBARCs offered the resolution and critical dimension (CD) control needed for the increasingly critical implant layers.

In this paper the benefits DBARCs can bring to other lithographic processes are reviewed. Back-end-of-line (BEOL) dual damascene processes are surveyed. Front-end-of-line (FEOL) processes are examined, including high-k metal gate (HKMG), double patterning, and spacer. All processes are defined, and the value that a DBARC brings to each process is examined, along with potential challenges.

Introduction

Advancements in technology beget more complex development. This inevitability is especially true in the semiconductor industry. As integrated circuit (IC) technology evolves, the materials and processes used to manufacture ICs become more sophisticated. This driving force exists for most materials used in the semiconductor industry, including bottom anti-reflective coatings (BARCs). In the early 1980s, BARCs advanced lithography patterning by reducing standing waves in photoresists by attenuating light (1). This success led to using BARCs to increase the substrate adhesion of photoresists. Subsequently, BARCs were adapted to fill vias and improve the dual damascene process (2).

Developer-soluble BARCs (DBARCs) are different than traditional dry-etch BARCs in that DBARCs are patterned with the resist during the develop step (1,3). The original application for DBARCs was to enhance the patterning of implant layers (3,4,5). These initial DBARCs developed isotropically and were adjustable by process modifications (6). DBARCs that developed anisotropically were brought to market next to answer the need for smaller features and less bias between the isolated and dense features (7,8,9).

Part of what drives technology growth is the ability of engineers to adapt knowledge from one focus area to another. An example is how dry-etch BARCs were adapted from use in line and space patterns on the front-end-of-line (FEOL) technology, to their use for filling vias and enhancing patterning in the back-end-of-line (BEOL) dual damascene process mentioned above. In this paper we will examine applications beyond implant in which DBARCs are being used. We will look at the use of a DBARC in the dual-damascene process. We will then look at the use of a DBARC as an adhesion promoter and will continue by reviewing a DBARC's role in advanced litho processes such as double patterning and spacer applications.

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Dual Damascene Processes

The via-first dual damascene process is common in BEOL interconnect processes. The basic flow is to pattern vias in the interlayer dielectric (ILD), then to pattern trenches aligned with the vias. After the ILD has been etched, a single metal deposition is used to fill the vias and trenches to form the interconnects. Because the dual damascene process creates the wires that connect the transistors, improvements in uniformity, alignment, and dimension control have a direct positive impact on yield and manufacturing cost reduction.

Given DBARC's establishment in the FEOL use in implant steps, one of DBARC's initial implementations beyond the implant process was the BEOL dual damascene process. The first application was to use a non-photosensitive DBARC as a via-fill BARC (10). After the vias were formed, the DBARC was used to partially fill the vias in preparation to pattern trenches. This reduced the thickness bias seen with isolated versus dense via fields, so the resist was more planar when coated. Ultimately, the DBARC helped to reduce the iso-dense bias offset seen when patterning trenches (10).

The next adaptation of DBARC into dual damascene processes was to replace the dry BARC used to form vias with a DBARC (11). The typical challenge of developing a process that sufficiently controls undercut was not needed, as the undercut did not affect the transfer of the resist pattern into the ILD, as shown in Figure 1 (11).

Using a DBARC to pattern vias provides several advantages. When using a dry BARC and resist to form vias, reactive ion etching (RIE) is needed to transfer the pattern through the BARC; this step is commonly known as the BARC open etch. During the BARC open etch, the top of the resist can be damaged, and a loss of circularity in the via pattern can result. Because the resist pattern transfers through the DBARC during the develop step, the BARC open etch is not needed and circularity would be maintained. Thus, using a DBARC to pattern vias would increase the fidelity and uniformity of the via pattern as it is transferred into the ILD.

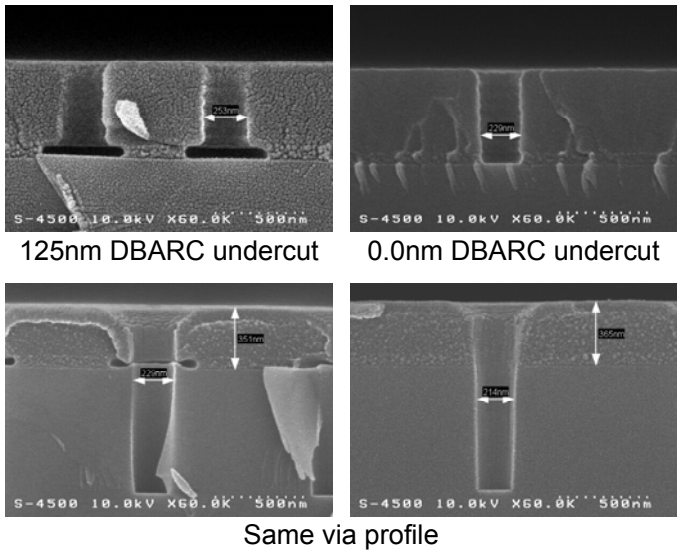


Figure 1: DBARC used in via formation (11).

The work on developing advanced photosensitive DBARCs (PS-DBARCs) for via patterning to realize these strengths has continued (12, 13). Features down to 80 nm have been shown with straight profiles. Because the PS-DBARC responds in many ways like a photoresist, one challenge to overcome is to establish what mask error enhancement factor (MEEF) will be required to accommodate the needed dose to clear both isolated and dense vias in the same exposure.

High-k Metal Gate (HKMG) Processes

The complementary metal oxide semiconductor (CMOS) process flow has adapted over the years to meet the challenges of each node. As the gate oxide thickness scaled with successive nodes, a new gate material was needed. The answer to this challenge was a metal gate, coupled with a high-k dielectric (HKMG) (15). The metal gate was needed because the common polysilicon gate was prone to defects at the low voltages used to switch the gate (16). The HKMG reduced gate leakage by increasing the transistor capacitance and allowed chips to function with reduced power needs.

Two process flows were developed to pattern the HKMG stack, a gate-first and a gate-last process. In the gate-first process, the thin capping metal in the HKMG needed to be patterned, and the process would be very sensitive. Photoresists did not adhere well to the metal layers, which was made worse by the wet chemistries needed to etch the capping metal (17). So to pattern the HKMG stack, a new process was needed.

DBARC was adapted as the enabler to pattern the metal capping layers in the gate-first HKMG process. DBARC protected the substrate by eliminating the use of RIE in the dry-BARC open etch step. Due to a DBARC's crosslinking ability, it increased substrate adhesion so the wet-etch process could transfer the pattern (9,17). An example of a process flow showing DBARC being used with HKMG technology is shown in Figure 2. The photoresist and DBARC are used in steps 2c and 2e, along with a wet etch to pattern the capping layers (17).

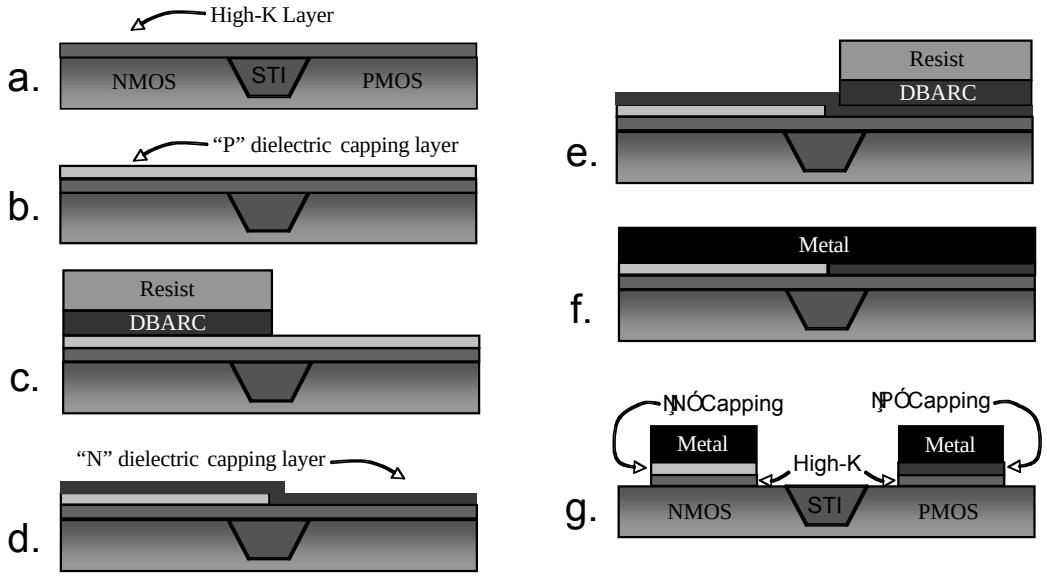


Figure 2: Gate-first HKMG process using DBARC.

As is often the case with shifts in technology, new issues emerged. One issue that DBARCs have faced many times is the thin layer of residue that is left behind after development. A significant amount of research has gone into quantifying and understanding the trends of residue produced by different DBARCs. The residue has been quantified using ellipsometry, X-ray photoelectron spectroscopy (XPS), and atomic force microscopy (AFM) (9, 18, 19, 20, 21, 22). Trends through processing conditions have also been evaluated. For non-photosensitive DBARC, BARC bake temperature emerged as the biggest process control for residue (20). BARC bake temperature was also found to affect certain PS-DBARCs (18). For PS-DBARC, the contributors to

residue were more complex. The chemistry components, thickness, and exposure dose all affected the post-develop residue (9, 21, 22). In both PS and non-PS DBARCs, it was found that the substrate also influenced the residue (19, 20). With the diverse factors that are involved with residue, it is a challenge that will continue to garner focus, especially as HKMG processes move into production.

Advanced Patterning Processes

As the gate length of devices shrink, so does almost every other part of a device. The solutions that lithographers have employed to maintain pace with shrinking features have become more complex than the end devices being made. To produce smaller features and maintain dense pitches, a common approach is to pattern twice, with the second pattern set between the first, thus doubling the pitch of the final pattern. These processes are called double patterning. The most basic approach is to use RIE to etch the first pattern into the substrate, then to create a second pattern and use RIE to etch it into the substrate as well. This litho-etch-litho-etch (LELE) process can be expensive, as wafers need to travel between the litho and etch modules twice. A solution to this problem can be found by incorporating a DBARC into the process (23, 24, 25). An example of a double-pattering process using DBARC is shown in Figure 3.

A double patterning process such as this takes advantage of multiple DBARC features. The attenuation of light helps the photoresist form the litho patterns. The solubility of DBARC in developer allows the resist pattern to be retained in the DBARC without a RIE. Also, the resist can be selectively removed with a solvent, as the DBARC is crosslinked and not dissolvable in resist solvents. This process can use a non-photosensitive DBARC or a PS-DBARC.

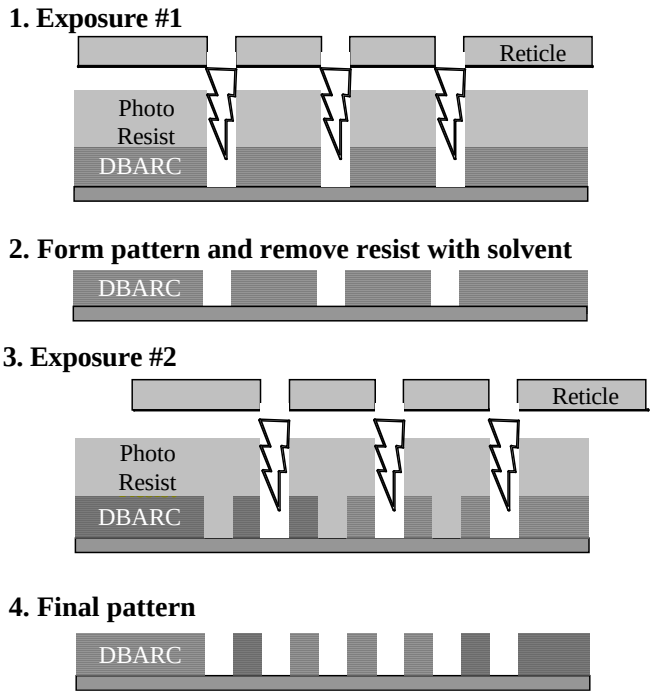


Figure 3: Double-patterning approach using a DBARC.

One question that would need to be addressed is if a DBARC had sufficient RIE resistance to allow the pattern to transfer. To overcome this, a hardmask could be incorporated into the process (26). An example of how this might work is shown in Figure 4. Once the pattern is transferred into the DBARC, a RIE could be used to move the pattern into the hardmask. This process could be repeated for the second patterning step. In this case, the wafers would need to go through the etch module twice, so this process would only provide a limited advantage of removing the BARC open etch.

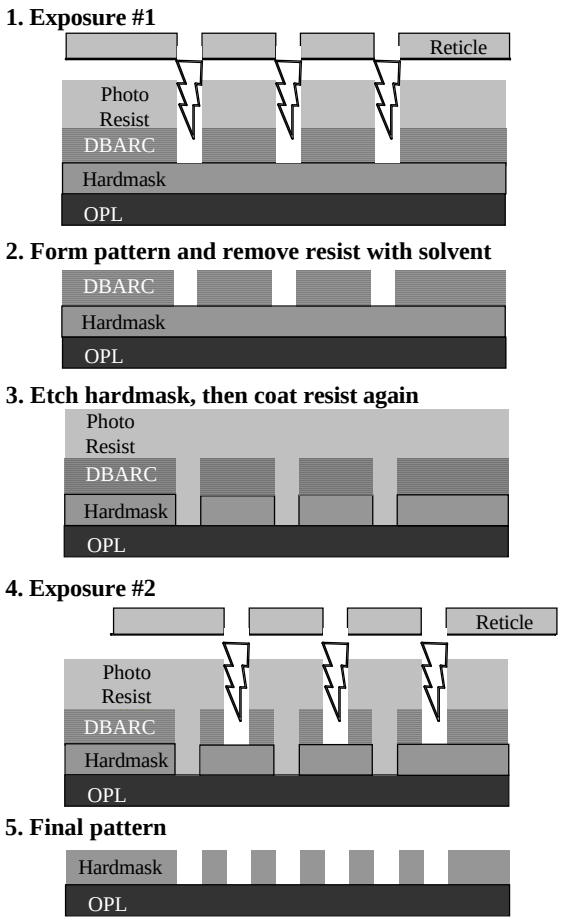
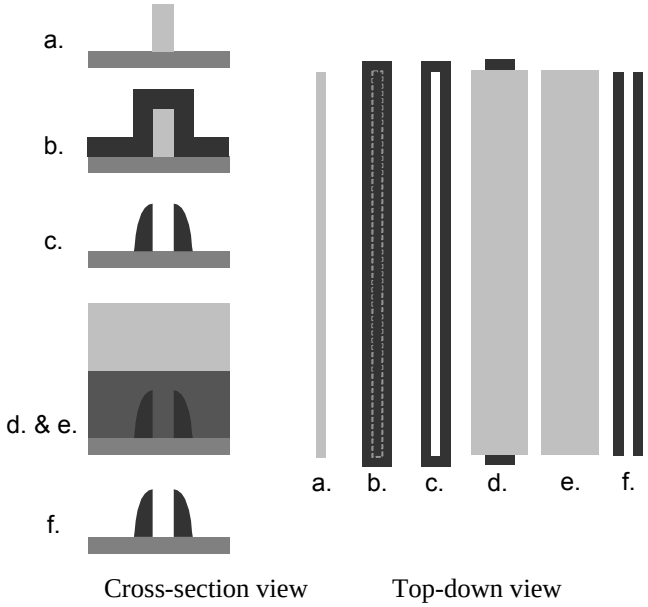


Figure 4: Double-patterning approach using a DBARC and hardmask.

DBARC Uses Beyond Semiconductors

This paper has examined several processes in which DBARCs are being used beyond implant. DBARCs have the potential to be used in processes to make devices beyond semiconductors. Lift-off layers are an example of such processes. Lift-off layers are commonly used when metal depositions are needed, and the surface of the substrate is sensitive. Figure 6 shows a basic lift-off process using a DBARC as the lift-off layer. For the process to work, some undercut is needed to allow the

Processes beyond double patterning are also using DBARC's unique capabilities. Spacer processes used in advanced patterning are a good example. Once lines are created using spacer technology, a loop is formed, as shown in Figure 5c. To trim the ends off the loop, an RIE is needed. An etch mask is needed that can easily be removed without damaging the delicate features. One approach is to use a DBARC and photoresist (27). This process forms spacer features as shown in Figure 5a, 5b, and 5c. In Figure 5d, the DBARC and resist are coated. Then in Figure 5e the RIE step removes the loop ends, while the DBARC and resist protect the rest of the features. Since the dissolution rate of DBARC is adjustable, a very high rate can easily be achieved. This high develop rate would allow DBARC to be removed from in-between the spaces as shown in Figure 5f.



a. Photoresist line. b. CVD layer. c. RIE of CVD layer. d. DBARC and resist pattern. e. RIE of exposed spacer. f. Trimmed spacer after resist and DBARC removal.

Figure 5: Spacer process using a DBARC.

stripping solution to contact the DBARC, as shown in steps 6b and 6c. The stripping solution dissolves the DBARC, allowing the remainder of the litho stack to lift off, as shown in step 6d. A DBARC offers the advantage of providing smaller photoresist features, controlling dimensions over topography, and providing controlled undercut to allow lift-off. To prove the concept for large feature sizes, a thick DBARC and photoresist were used in figure 7. Different develop times were tested to create different profiles. An undercut profile was achieved with 40 seconds of develop time.

Conclusions

DBARC applications have matured over the past several years. The initial success of DBARCs in implant layers provided a knowledge base for it to broaden into other process areas. In BEOL dual damascene processes, a DBARC could be used as a partial fill BARC. DBARCs also had value to add to BEOL via processes, such as increased etch budget and improved pattern fidelity. This history paved the way for DBARCs to be used in FEOL applications other than implant. In the FEOL, DBARCs are being used in HKMG patterning to promote adhesion and reduce the use of RIE at the gate level. Advanced double-patterning schemes are also using DBARCs. The ability to retain a pattern in the DBARC because of its resistance to resist solvents has made DBARC a key component in current double-pattering patents and applications. Spacer technology has also benefited from using a DBARC's ability to easily adjust solubility. As use of DBARCs in the semiconductor industry has matured, it was proposed that other industries might benefit as well.

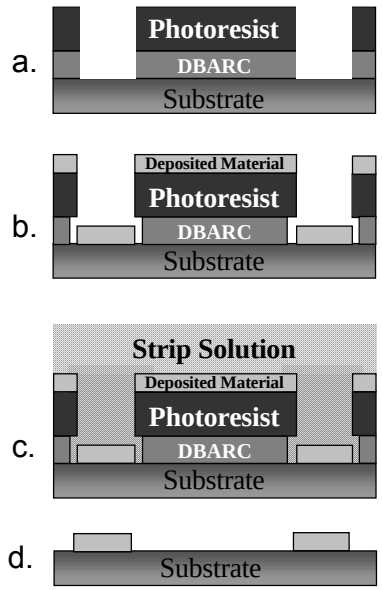


Figure 6: Lift-off process using a DBARC.

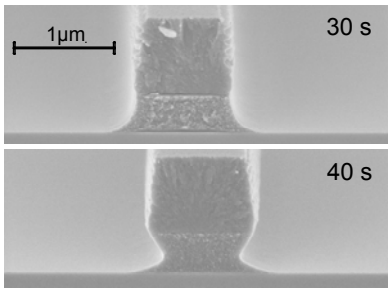


Figure 7: DBARC cross sections through develop time.

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