Process Development for Developer-Soluble Bottom Anti-Reflective Coatings (BARCs)

Carlton Washburn, Alice Guerrero, Ramil Mercado, Douglas Guerrero & Jim Meador

Brewer Science, Inc., 2401 Brewer Dr., Rolla, MO 65401 USA

Abstract

This paper will present guidelines for developing processes that use thermosetting and photosensitive developer-soluble bottom anti-reflective coatings (BARCs). Process considerations for a dry etch BARC (dry BARCs) are distinctly different from those required for developer-soluble BARCs (DS-BARCs). Developing a process for a dry BARC is straightforward and can occur rather quickly once resist compatibility has been established. Developing a process for thermosetting developer-soluble BARCs (TDS-BARC) takes more time due to the need to optimize bake temperature, bake time and developer conditions. TDS-BARCs have been used in early generations of lithography (g-line, i-line, and KrF) and are well understood. Designing a process utilizing a photosensitive developer-soluble BARCs (PDS-BARC) for use in ArF technology is more complex than for its BARC predecessors. Though the development nature of a PDS-BARC is more anisotropic, post-exposure baking parameters and acid diffusion must be optimized. Even though the process development becomes more complex as technology advances, the processes can actually improve isotropic versus anisotropic development and bake windows. In this paper we present the advantages of using a DS-BARC in the implant process to overcome issues including CD control and topography. The differences between developing processes using dry and TDS-BARCs will also be explored. Moreover, differences in processing TDS-BARCs and PDS-BARCs will be described based on resist/BARC compatibility, BARC thickness, topography issues, and bake sensitivity. Finally, advantages and disadvantages of using PDS-BARCs compared to TDS-BARCs will be discussed.

Introduction

As integrated circuit (IC) technology advances, the materials used in manufacturing become more sophisticated. As materials advance, the processing required to optimize and qualify the materials used in manufacture of ICs becomes more complex. This complexity places more pressure on the process engineer to develop processes that are both robust and cost-effective.

This driving force exists for all materials used in the semiconductor industry, including bottom anti-reflective coatings. Limitations in using dyed resists for patterning in the implant process have led to i-line and KrF TDS-BARCs for the implant process. The next generation of DS-BARC is the PDS-BARC for ArF applications. For each advance in BARC technology there is a unique process consideration. For example, dry-etch BARCs have a large range in which they can be baked and still provide optimal performance, but they must be removed by reactive ion etching (RIE). TDS-BARCs are removed with the resist by the developer, but they have a specific range over which they

Reprinted with permission from FULIFILM Electronic Materials, as published in connection with
Interface 2006, the 43rd Proceedings of the FUJIFILM Electronic Materials Microlithography Symposium.

can be baked. PDS-BARCs have a wide bake range and are removed during the resist development, but they must be customized to each resist because of their precise photospeed.[1] Thus process development for the implant layer becomes much more complex as the technology advances.

Producing a usable pattern for the implant layer has a unique set of challenges. Of these many challenges, most process engineers tend to focus mainly on critical dimension (CD) control, topography issues, and pattern overlay. CD control is vital to maintaining implant profiles and is complicated by existing topography on the substrate. Topography can also cause reflective notching. Pattern overlay is also a challenge, especially if different scanners are used for critical and implant layers. To mitigate the issues of CD control and topography, TDS-BARCs were developed.[2,3] As technology advanced, critical layers were imaged by ArF scanners, but older KrF scanners were retained for implant layers to increase throughput while decreasing capital costs. This strategy also created a serious overlay problem because of the two different scanner wavelengths used.[4] One solution to this overlay problem was to use an ArF scanner for both implant and critical layers.[4]

Discussion

To properly develop a process for the implant layer, many factors must be considered. For this paper, four factors related to the patterning step preceding implantation will be explored. These factors will focus on DS-BARCs and will include resist/BARC compatibility, BARC thickness, topography issues, and bake sensitivity. Resist-specific factors such as exposure latitude and depth of focus are well characterized and will be set aside for the purpose of this paper.

Resist Compatibility

The first step in developing a process for pattering an implant layer using a DS-BARC is to establish the compatibility of the resist and BARC. Matching resist compatibility is less demanding for TDS-BARCs. TDS-BARCs for KrF technology has been developed to match both ESCAP and acetal resists. For PDS-BARCs, resist compatibility is more complex. The post-exposure bake (PEB) step the resist must undergo also acts as the PEB step for the PDS-BARC.[1] Thus, the PEB requirements that the BARC and resist need must match. Because PEB steps for resists can vary by several degrees and cannot be adjusted without CD degradation, the PDS-BARC must be designed accordingly. The requirement for PEB matching of the resist and PDS-BARC adds a BARC formulation optimization step to process implementation for each resist.

Several formulations of different ratios of the constituents of a PDS-BARC can be generated, but lithography testing is expensive and proper metrology data are time-consuming to generate. Thus using contrast curves to screen different PDS-BARC samples for resist matching is proposed. Figure 1 shows the contrast curve of a PDS-BARC that is designed to work with a PEB of 110°C. This method of generating contrast curves employs the use of a Clean Track ACT® 8 and VUVES-4500 mini exposure tool. Results indicate the PEB range in which a given PDS-BARC sample will clear, dose-to-clear and the quality of the contrast. Once a PDS-BARC with a PEB matching that for the resist is chosen, diffusion must be considered. Diffusion of photoacid generators

(PAGs) in the resist will determine the final ratios of the PDS-BARC constituents. A properly designed experiment utilizing lithography and measuring EL, DOF and profiles will optimize the ratio of PDS-BARC constituents to produce the best results with a chosen resist.

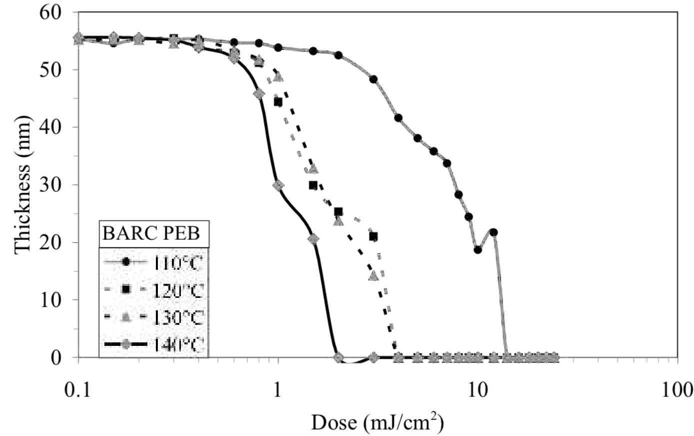


Figure 1. Contrast curves of a photosensitive BARC through PEB.

BARC Thickness Determination

After compatibility of the resist and BARC has been established, the proper BARC thickness for the given application must be determined. Factors such as substrate type, variation in silicon oxide, and even topography thickness can contribute to this decision. Both TDS-BARCs and PDS-BARCs, as opposed to a dry-etch BARC, operate best at a first reflectivity maximum on flat silicon. It is believed that the extra light that is allowed through cleans up the node characteristic of TDS-BARCs at the BARC/resist interface as shown in Figure 2.[3] In a PDS-BARC, the extra light gives the PAG a second chance to react, which results in better clearing of the BARC.[1] When the substrate is something other than silicon, the first maximum may not provide the best solution. Figure 3 shows Prolith® simulations for substrate reflectivity using the same settings, except for using a light exposure wavelength of 248 nm for BSI.N0889A, a TDS-BARC, and 193 nm for BSI.W05039, a PDS-BARC. If 200 nm ± 10 nm is simulated, the best thickness solution for reflectance control is no longer the first maximum, represented in the circles. Instead, a new minimum is achieved, designated in the squares.

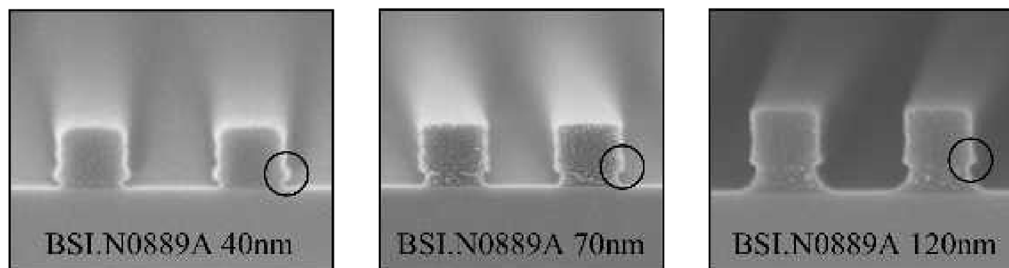


Figure 2. Node at TDS-BARC and resist interface for different BARC thicknesses.

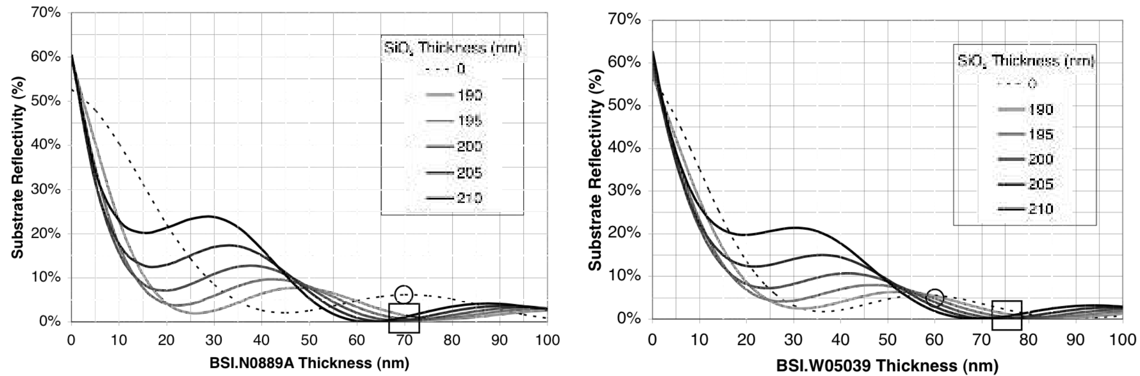


Figure 3. Substrate reflectivity of a TDS-BARC (BSI.N0889A) and PDS-BARC (BSI.W05039) on various SiO_2 thicknesses.

Topography Considerations

Existing topography can drastically complicate designing a process using DS-BARCs. This difficulty is due not only to the inability to simulate the final film profile across a step, but also to the difficult and tedious nature of developing a process that takes into account the small spaces common on modern substrates. The problem is further convoluted by the fact that each fab has a unique topography pattern and step height, thus each fab must have a separate set of tests run to develop the best process for that unique topography.

It has been previously proven that for a dry BARC the first minimum is not always the best BARC thickness for covering topography due to the change in BARC thickness as it coats over a step.[5] This principle is also true for a DS-BARC. Figure 4 shows how a thin film might change thickness as it coats an isolated step.

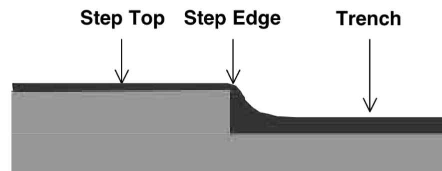


Figure 4. Measurement locations on a topography substrate.

A PDS-BARC was coated using a Brewer Science CB100 coat/bake system at 1500 rpm and was contact baked at 160°C for 60 seconds using the same equipment. Flat 100-mm silicon wafers and silicon substrates with a silicon oxide isolated step of 150 nm were coated with several thicknesses of BSI.W05039I. The results are shown in Figure 5. It can be seen that a PDS-BARC that produces a coating of 60 nm on flat silicon produces a much thinner film at the step top, and a much thicker film at the step edge. This coating behavior changes the reflectivity control of the PDS-BARC, and resulting CDs can be simulated to find the high and low swing of the CD, but this only shows the extremes. This method does not reveal other problems such as possible BARC undercutting and post-develop residue. Thus a test must be designed and executed with special attention to cross-section results in trench and open areas.

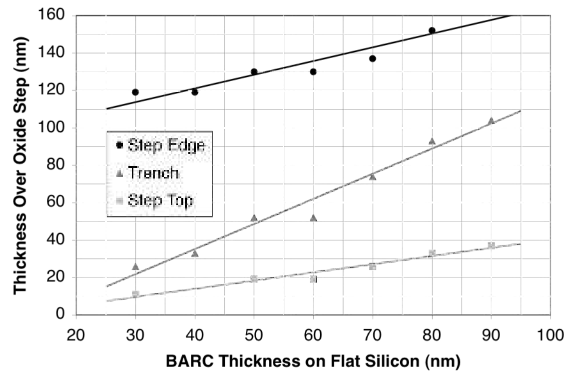
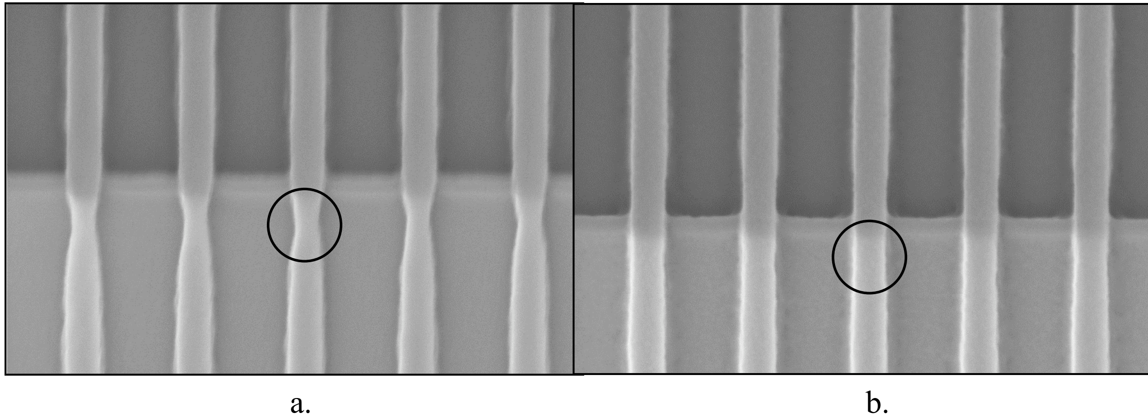


Figure 5. BARC thickness measurements over an isolated step.

To further study the effects that topography might have on different PDS-BARC thicknesses, lithography was shot using the same processing conditions and resist, but using a first-minimum (38 nm) and first-maximum (55 nm) PDS-BARC. The wafer with existing 150-nm silicon dioxide topography was rotated 90° in the scanner so that the printed lines would be perpendicular to the topography. Figure 6 shows a top-down SEM image of an isolated step with perpendicular lines. As the 38-nm PDS-BARC coated the step, it thinned across the step edge as shown in Figure 4. This thin BARC cannot provide as much reflection control. Table I helps to explain the CD shift of the line in Figure 6. The 38-nm BARC produced a thinner film over the step edge than the 55-nm BARC. This variation produced a 20% difference in substrate reflection, and resulted in a large change in the resist line width. The 55-nm thickness provided much better reflection control.



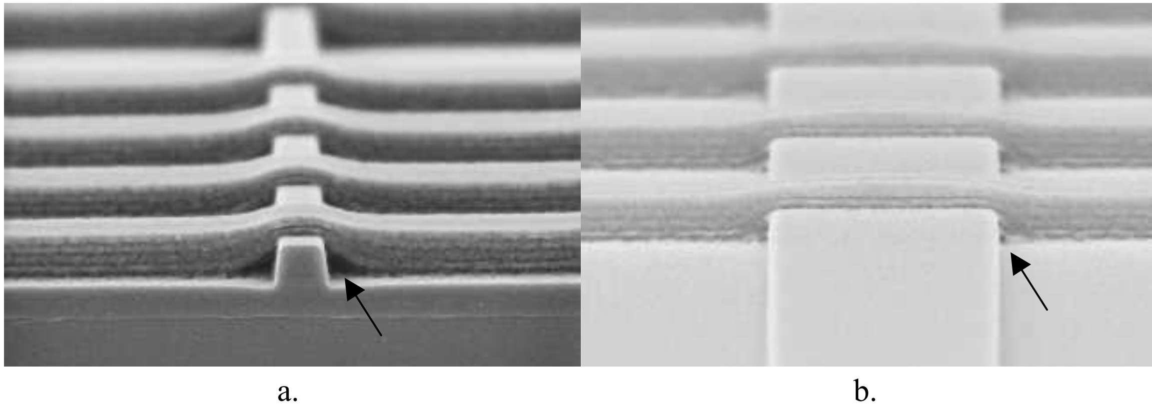
a. b.

Figure 6. Top-down SEM images of resist lines processed with (a.) 38-nm and (b.) 55-nm PDS-BARC perpendicular to existing topography.

Table I. Results from topography test in Figure 6.

	a.	b.
PDS-BARC thickness (nm)	38	55
Thickness at step edge (nm)	~10	~20
Resulting substrate reflectivity (%)	30	10

When considering topography, the constituent ratios that were earlier checked to optimize PEB must now be refined. Figure 7 shows and un-optimized and optimized PDS-BARC formulation. Figure 7a. shows a ratio that worked well on flat silicon, producing good profiles, but when it was processed over topography, it was discovered that the PDS-BARC developed out from under the resist line as the line coated over another isolated line. After an adjustment to the PDS-BARC formulation, Figure 7b. shows that the PDS-BARC remains after the develop step.



a. b.

Figure 7. Cross-sections of (a.) un-optimized and (b.) optimized PDS-BARC.

Bake Temperature

The last factor to consider when developing a process with a TDS or PDS-BARC is the BARC bake temperature. The bake temperature affects TDS-BARCs much more than PDS-BARCs. A PDS-BARC's bake temperature can vary as much as 15°C without a significant change in CD, as shown in Figure 8. However, bake temperature is a key element in performance for a TDS-BARC. A plot of the bulk develop rate of BSI.N0889-A is shown in Figure 9. As the TDS-BARC bake temperature increases, the bulk develop rate decreases. This relationship allows the process engineer to tune the develop rate of the TDS-BARC to his or her process by using bake temperature. Varying the bake temperature of the BARC will also show what range the process can tolerate.

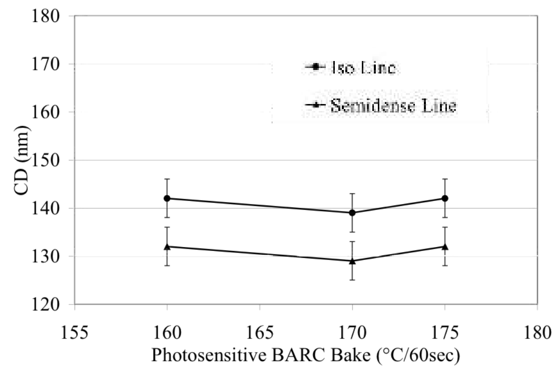


Figure 8. CD variation across TDS-BARC bake temperature of BSI.W05039I.

The change in develop rate of a TDS-BARC will change the amount of undercutting or footing of the BARC, as shown in Figure 9. This develop rate can change implant profiles and must be properly optimized. SEM cross-sections are the typical method for establishing the BARC footing/undercutting, but scatterometry may be another option.

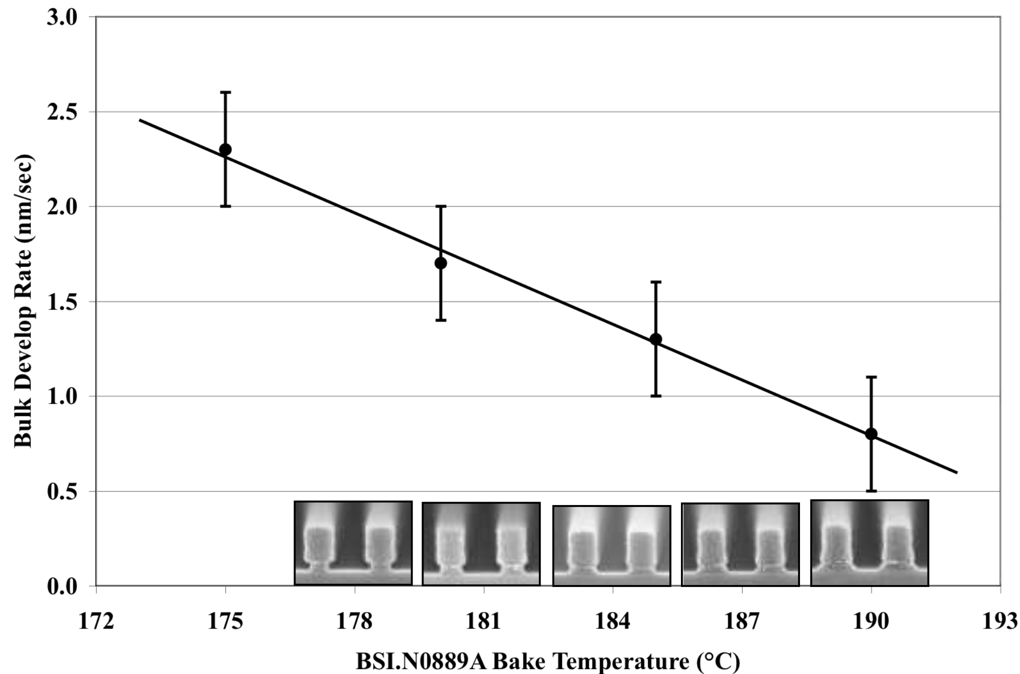


Figure 9. As bake temperature increases bulk develop rate decreases and TDS-BARC undercut decreases.

Conclusions

In conclusion, process development guidelines for TDS-BARCs and PDS-BARCs were explored. Resist/BARC compatibility was discussed with heavy importance placed on optimizing the constituent ratios for a PDS-BARC. BARC thickness issues were discussed, and it was shown that a DS-BARC's first maximum reflectivity node is usually the best thickness. Topography was discussed, and it was shown that a DS-BARC should be fine-tuned using topography cross-sections. Finally, bake sensitivity was explored, and it was learned that a TDS-BARC's bake temperature can be used to tune the develop rate of the BARC, while a PDS-BARC has at least a 15°C window for BARC bake.

Acknowledgments

The authors would like to thank John Thompson and Dennis Howard for their diligent SEM work and Mariya Nagatkina and John Massey for their processing skills.

References

1. D.J. Guerrero, R. Mercado, C. Washburn, J. Meador, *Journal of Photopolymer Science and Technology*, Vol. 19, no. 3, 2006, pp. 343-347.
2. X. Shao, A. Guerrero, Y. Gu, *SEMICON China 2004 Technology Symposium*, March 17-19, 2004.
3. I. Guilmeau, A. Guerrero, V. Blain, S. Kremer, V. Vachellerie, D. Lenoble, P. Nogueira, S. Mougel, and J. Chapon, *Proceedings of SPIE*, Vol. 5376, 2004, pp. 461-470.
4. D.C. Oweyang, H. Chen, R.M. Deng, B.C. Ho, *Proceedings of SPIE*, Vol. 5038, 2003, pp. 1095-1106.
5. A.H. Gabor, S.D. Halle, C. Kallingal, *Proceedings of SPIE*, Vol. 5753, 2005, pp. 699-707.