

Edge Protection of Temporarily Bonded Wafers during Backgrinding

Dongshun Bai^a, Xing-Fu Zhong^a, Rama Puligadda^a, Jurgen Burggraf^b,
Daniel Burgstaller^b, Chris Lypka^c, and James Verzosa^c

^a Brewer Science, Inc., 2401 Brewer Dr., Rolla, MO 65401, USA

^b EV Group, A 4780 Schaerding, DI Erich Thallner Strasse 1, Austria

^c DISCO HI-TEC AMERICA, Inc., 3270 Scott Blvd., Santa Clara, CA 95054 USA

Edge chipping during backgrinding is one of the main challenges of processing temporarily bonded wafers. The edge chipping may propagate during subsequent process steps and eventually result in yield loss. We conducted a study to compare different methodologies for wafer edge protection during backgrinding, including using pre-thinned carrier wafers, large carrier wafers, edge-trimmed device wafers, and material edge modification. This paper will introduce the metrology developed to quantify edge chipping and compare the results from different protection methods.

Introduction

Industry-leading experts claim that three-dimensional (3-D) integration and packaging present the semiconductor industry's direction for the future. To meet the industry need for handling increasingly thin and fragile product wafers, Brewer Science and EV Group have collaborated to create a new temporary wafer bonding technology to provide a novel solution for processing ultrathin wafers (1-8). To prevent thin wafers from being damaged during processing, they can undergo temporary bonding to a carrier wafer by using temporary wafer bonding materials. The carrier wafer provides mechanical support during backside processing, and the temporary wafer bonding material protects the active surface of the device wafer. However, edge chipping during backgrinding is one of the main challenges for temporarily bonded wafers. The edge chipping may propagate during subsequent process steps and eventually result in yield loss. We conducted a study to compare different methodologies for wafer edge protection during backgrinding. This paper will introduce the metrology developed to quantify edge chipping and compare the results from different protection methods.

Experiment

Wafer Edge Protection Schemes

As listed in Table I, three known methods, that is, using pre-thinned carrier wafers, large carrier wafers, and edge trimmed device wafers, as well as a material edge modification method developed by Brewer Science were applied to achieve edge protection. Four wafer pairs were used in each scheme in this study. Other known methods such as edge extraction (where the device wafer edge is cut off by 1 to 2 mm during grinding) are not included in this study because of the inaccessibility of the tools.

D. Bai, X.-F. Zhong, R. Puligadda, J. Burggraf, D. Burgstaller, C. Lypka, J. Verzosa, "Edge protection of temporarily bonded wafers during backgrinding," *ECS Transactions*, vol. 18, no. 1, 2009, pp. 757-762.
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Table I. Schemes for Wafer Edge Protection

Scheme	Description
Pre-thinned carrier wafers	The carrier wafers were pre-thinned to 480 μm to provide more supporting area.
Large carrier wafers	Large carrier wafers were used to provide protection of the edge of device wafer
Edge trimming	The device wafers were pre-trimmed along the edge by 1 mm in width and 100 μm in depth. (see Figure 1f for details)
Material edge modification	The profile of the temporary wafer bonding material along the edge of each bonded wafer pair was modified to provide good support during grinding

Materials

Wafers. Wafers used in this study were 8-inch ultra-flat silicon wafers with a diameter of 200 ± 0.2 mm, unless specified, from Silicon Quest International (SQI). The pre-thinned silicon carrier wafers with a diameter of 200 ± 0.2 mm were thinned on a DISCO DFG8540 grinder. The large silicon carrier wafers were from MEMC and had a diameter of 200.1 ± 0.1 mm. The device wafers that were bonded to the large carrier wafers had a diameter of 200 ± 0.1 mm. The edge-trimming process was done on a DISCO DFD6361 Fully Automatic Dicing Saw, and the front side of each wafer had 100 μm in depth trimmed from the outermost 1-mm-wide band. The thickness of the wafers was 725 ± 25 μm except for the pre-thinned carrier wafers. The wafer to be ground was called the “device wafer,” and the wafer used to support the thinned wafer was called the “carrier wafer.” All wafers used in this study were blank wafers having no features.

Temporary Wafer Bonding Material. The temporary wafer bonding material used was WaferBOND™ HT.10.10 material from Brewer Science, Inc.

Coating and Bonding of Wafers

All wafers were coated and bonded on an EVG® 850TB automatic bonding system at EVG USA except for the wafers bonded to large carriers, which were coated and bonded on the auto-centering system at EVG Austria. The process used for coating and bonding the wafers was the same for all wafers and is described below.

Coating and Baking. The device wafers were coated with WaferBOND™ HT.10.10 material at 1200 rpm for 30 seconds. After coating, the wafers were proximity baked at 160°C for 4 minutes. The coating thickness of one wafer was measured on a Filmetrics thickness measuring system and the coating had a mean thickness of 19.6 μm and minimum and maximum thicknesses of 19.1 and 20.2 μm , respectively.

Bonding. The device wafers were then bonded to the carrier wafers at 180°C and 3500 N for 2 minutes under vacuum. The bonding quality was very good, as no voids or

sharp color variations were observed by scanning acoustic microscopy (SAM) on all bonded wafer pairs.

Material Edge Modification

Material edge modification was performed to repair the non-uniformity of the bonding materials created during the bonding process. After bonding, the temporary wafer bonding materials between two bonded wafers were removed along the edge by side rinsing with solvent by 0.5 mm into the wafer edge. Then the space that was occupied by the removed material was refilled with WaferBOND™ HT.10.10 material with a nozzle along the bonded wafers' edge. The wafer pairs were then baked at 150°C for 2 minutes. After modification, the wafer edge section was inspected with a camera. The material covered the entire wafer edge including the bevel evenly.

Grinding and Polishing

Grinding was performed on a DISCO DFG8540 Fully Automatic Grinder. All wafer pairs were ground from the backside of the device wafers to about 92 µm with wheel Z1, and then further ground to about 52 µm with Poligrind wheel Z2. To reduce the stress generated during grinding, a dry polishing step was used to smooth the ground wafer surface on a DISCO DFG8140 Fully Automatic Polisher. The final thickness of the ground wafers after dry polishing was about 50 µm. Detailed information on the wheel type used in each step is listed in Table II.

Table II. Detailed information on grinding and dry polishing wheels

Wheel	Z1	Z2	Dry Polishing Wheel
Code	DRSJ0072	DRAA0005	PAZZ0014
Specification	GF01-SDC320-BT300-50	PW-005	DPW-014 DP-F05
Size	200x4Wx5T-SD	200x7Tx3W	300x11Tx60

Wafer Edge Inspection

After grinding and dry polishing, the device wafer edges were inspected with a Keyence VHZ100 microscope. A quick survey was conducted first around the wafer circumference to ensure that no large chips were missed during inspection. To quantify the edge chipping, the wafer edge was inspected every 30 degrees along the edge with 100X magnification. The number of chips within each range was counted and categorized into four grades according to the chipping distance into the wafer edge. The four grades are <10 µm, 10 to 50 µm, 51 to 100 µm, and 101 to 200 µm.

Results and Discussion

For all 20 wafer pairs that went through the grinding and dry polishing process, we noticed only a single small blister on each of two device wafers. We did not observe any cracking or delamination along the wafer edges. The largest chipping we observed with a microscope was less than 150 µm into the wafer edge. Thus, the temporary wafer bonding material worked very well during backside grinding and polishing of the device wafers.

Because we previously observed large chips and cracks in the thinned device wafers while they were still bonded to the carriers after shipping, we decided to do the edge inspection immediately after dry polishing to eliminate the chance of later detecting possible shipping damage to the wafer edges. Automatic wafer edge inspection systems are currently on the market, such as the VisEdge system from KLA-Tencor and the E30™ system from Rudolph Technologies. However, we could not find a place that could do both the grinding and then the automatic wafer edge inspection. Therefore, we developed a metrology to quantify the wafer edge chipping after grinding and stress relief.

As discussed above in the Experiment section, we performed a 12-point inspection along the wafer edges on each of the thinned device wafers and categorized the chipping according to the distance into the wafer edge. The overall results are listed in Table III.

Table III. The number of chips and their size distribution on 12 inspection spots

Scheme	Chipping numbers on twelve inspected spots				
	Total number	<10 μ m	10 to 50 μ m	51 to 100 μ m	101 to 200 μ m
Pre-thinned carrier wafers	16 \pm 5.6	9.0 \pm 3.7	6.3 \pm 3.2	0.8 \pm 1.0	0.0 \pm 0.0
Large carrier wafers	39.3 \pm 8.7	18.8 \pm 2.5	19.3 \pm 7.5	1.3 \pm 1.3	0.0 \pm 0.0
Edge trimming	7.3 \pm 2.1	5.5 \pm 0.6	1.8 \pm 1.7	0.0 \pm 0.0	0.0 \pm 0.0
Material edge modification	25.3 \pm 8.5	9.3 \pm 5.4	15.5 \pm 2.9	0.5 \pm 1.0	0.0 \pm 0.0
Control	66.3 \pm 12.1	14.0 \pm 5.5	43.3 \pm 8.5	8.0 \pm 9.5	1.0 \pm 1.2

All four edge protection methods showed improvement in reducing the edge chipping. Edge chipping was reduced by at least 40% based on the total chipping number. The chipping size was remarkably reduced as well, and we did not observe chips larger than 100 μ m for all protection schemes. Figure 1 shows pictures of the device wafers taken by the microscope after backgrinding and dry polishing. These pictures were taken of the same position on the thinned wafers for different schemes. The grid lines in the picture were used for determining the chipping size into the edge.

Among the four protection schemes, the edge trimming method provided the best edge protection. It not only reduced the total number of chips by 89% but also reduced the chip size. All chips from this scheme were less than 50 μ m and most of them were less than 10 μ m. Figure 1f shows a picture of the edge-trimmed device wafer. By cutting the wafer along the edge by a width of 1 mm and a depth of 100 μ m, the resulting wafer edge was protected very well during grinding and polishing to reduce edge chipping.

The pre-thinned carrier wafers provided the second-best results. The total number of chips was reduced by 76 percent and the chip size was dramatically reduced as well. The pre-thinned carrier also provided good thickness uniformity so that the total thickness variation of the device wafer after thinning could be reduced as well.

The material edge modification method also exhibited remarkable improvement in reducing chipping. The uniform support from the materials around the edge of the bonded wafer pair provides a better support of the device wafer edge.

The protection from the large carrier wafer is not as good as that of the other methods. The diameter of large carrier wafers in this study was 200.1 ± 0.1 mm, which may not cover the edges of device wafers with a diameter of 200 ± 0.1 mm, and the alignment becomes very critical in this situation. A large carrier wafer with a diameter of 200.2 ± 0 mm is ideal in this situation and is also acceptable for most semiconductor equipment.

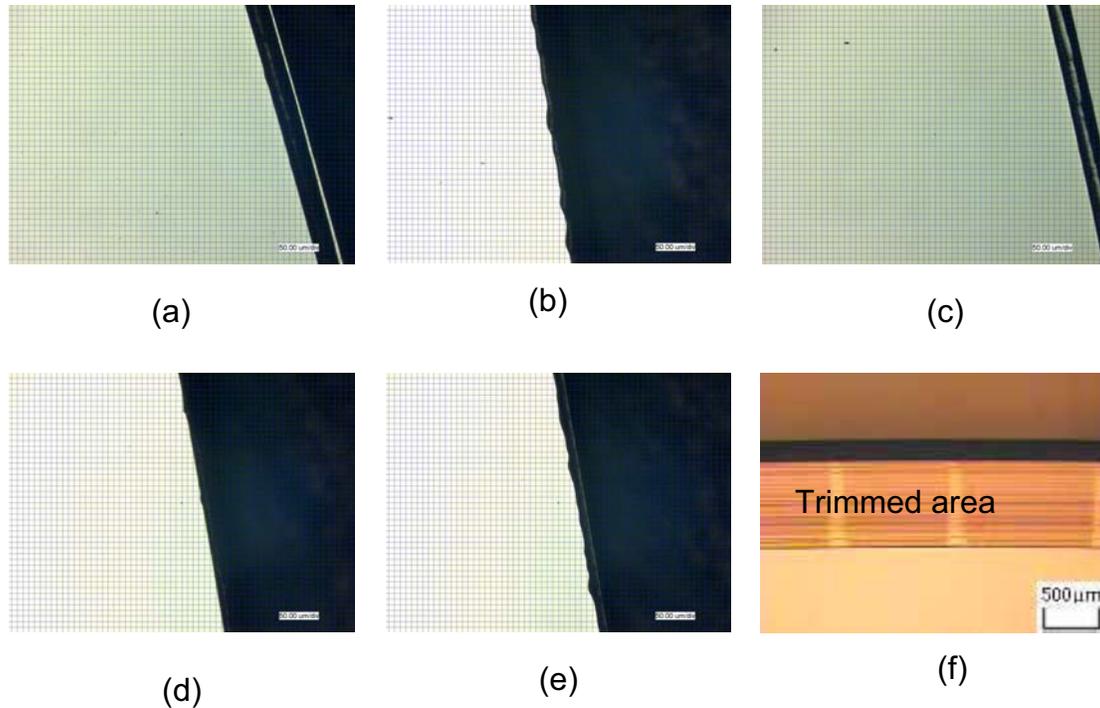


Figure 1. Pictures of device wafer edges after grinding and dry polishing for schemes of a) a pre-thinned carrier wafer, b) a large carrier wafer, c) edge trimming, d) material edge modification, e) control. f) shows a front view of the edge-trimmed wafer.

Statistical analysis of the chipping data

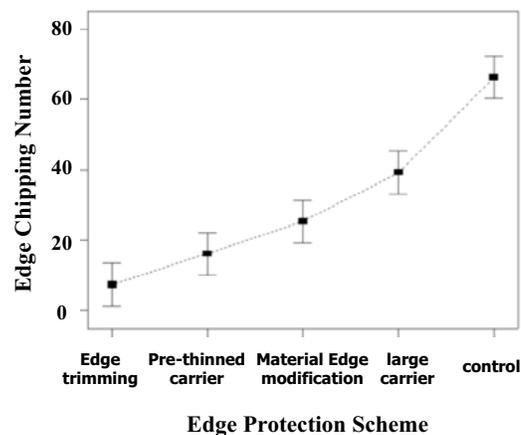


Figure 2. Statistical analysis of the chipping data based on total number of chips from 12 inspection spots.

We also analyzed the total number of chips from the 12 inspection spots by using Design-Expert software. The study was treated as one factor 5 level designed experiment with four replicates. The analysis of variants (ANOVA) resulted in a model F-value of 32.34, which implies that the model is significant. There is only a 0.01% chance that a model F-value this large could occur due to noise. The 95% confidence intervals for each scheme are also plotted in Figure 2. The model graph clearly shows that the effect of treatment is very significant, with edge trimming giving the least chipping, followed by pre-thinned carrier wafers, material edge modification, large carrier wafers and control wafers without treatment.

Conclusions

Four edge protection schemes were tested to protect wafer edges from chipping during backgrinding. All schemes showed improvement in reducing the number of edge chips. The edge trimming method is the most effective method of the four, followed by the pre-thinned carrier wafer and the material edge modification methods. Large carrier wafers used in this study may not be able to protect the entire device wafer edge, they only reduced the number of chips by 40%.

Acknowledgments

Thanks to Mark Privett from Brewer Science for his suggestions on this study. Also, the material edge modification assistance provided by Gary Brand and Jeremy McCutcheon from Brewer Science is greatly appreciated. Thanks to Chad Brubaker from EV Group for his support on wafer coating and bonding.

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