Rework/stripping of multilayer materials for FEOL and BEOL integration using single wafer tool techniques

Stephen Turner
Brewer Science, Inc., 2401 Brewer Dr., Rolla, MO, USA 65401

ABSTRACT

As feature sizes continue to the 45nm and 32nm nodes, significant challenges will continue to arise in both front-end-of-line (FEOL) and back-end-of-line (BEOL) applications. The reduced thickness, as well as the reduced etch resistance, of the photoresist (PR) makes it nearly impossible to use the PR as both an imaging and a pattern transfer layer. This etch challenge has led device manufacturers and vendors to explore the use of multi-layer (trilayer) stacks. Multilayer stacks are typically comprised of a thick via-filling organic layer that will provide adequate etch resistance while etching into low-k and ultra-low-k dielectrics. A silicon-containing layer is then applied on top of the via-filling layer, which will provide improved imaging, as well as etch resistance for the organic layer. The PR is then applied on top to complete the multilayer stack. While many challenges have presented themselves in multilayer stacks, new challenges such as rework and cleaning have arisen. As low-k and ultra-low-k dielectrics become more prevalent, traditional oxygen ashing processes for the removal of PR and anti-reflective coatings can cause damage to the dielectric layer due to the chemical and physical structures of the materials involved. While some processes have been developed to replace damaged dielectric material during ashing and etching through silyation, alternate processes are being developed where entirely wet stripping processes can remove multilayer stacks. One advantage of an entirely wet removal process is that it can prevent damage caused by ashing or etching, and the wet stripper is developed so it does not attack the dielectric films. While an entirely wet removal process has potential advantages, it still must be proven that these processes can remove residues that are left after etch processes, sufficient removal of particles are obtained, and any material loss of the dielectric layer meets the requirements of the customer and the International Technology Roadmap for Semiconductors (ITRS). Other challenges are presenting themselves, as many customers would like to move from batch-type wet rework or cleaning processes to single wafer tool processes.

It is the intent of this paper to not only identify new wet cleaning materials that can be used to remove multilayer materials by means of an entirely wet process, but also to find single wafer tool processes that produce fewer particles (defects) and cause no dielectric material loss.

1 INTRODUCTION

As the semiconductor industry continues to design devices for the 45nm and 32nm nodes, the industry as a whole is also going through continuous change. Device manufacturers are constantly using new dielectric materials to lower the dielectric constant and improve device performance. With these new materials and devices, new challenges present themselves that might have not been as important in the past. One important factor is that the new dielectric materials will not stand up to the older rework/strip processes that manufacturers are accustomed to using. Another factor is that devices that use advanced multilayer materials cannot simply be removed by traditional oxygen ashing techniques since the hardmask layer has inorganic components that are very similar to those in the dielectric. While these two factors will be very device and materials specific, the industry as a whole is also looking at moving away from batch type tools for rework/strip processes and moving to advanced single wafer processing tools. While device manufacturers decide on what type of processing techniques they will require for their devices, the industry is also aggressively looking to reduce both acceptable defect sizes and overall defect counts. The following figure shows how aggressive the 2005 ITRS is for both acceptable defect size and defect counts after both the lithography cell and the cleaning process.

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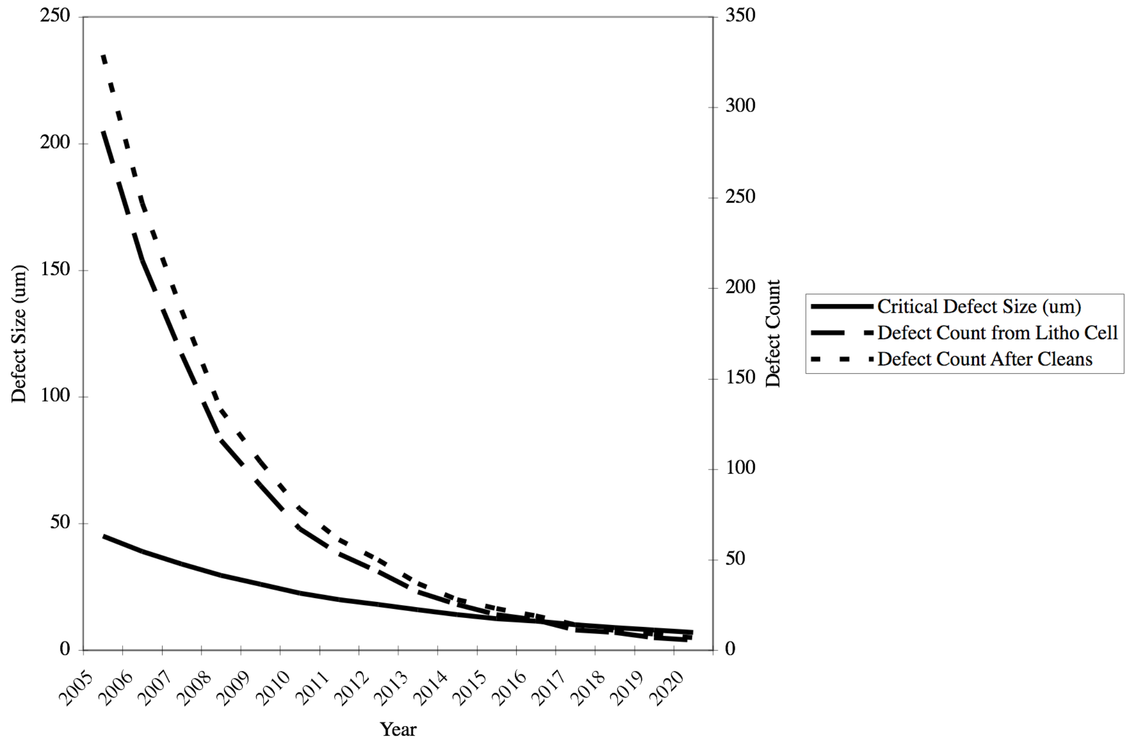
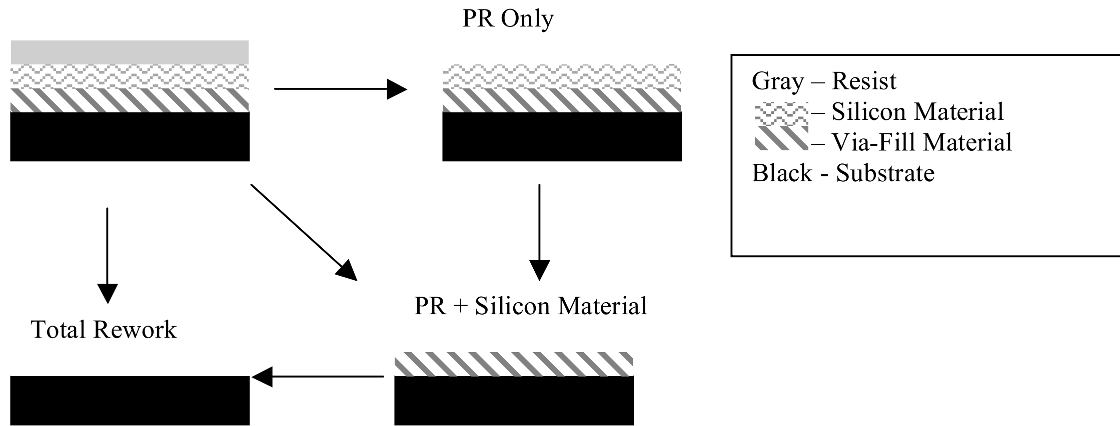


2 RESULTS & DISCUSSION

2.1 Rework/Strip Processes

There are a variety of reasons that device manufacturers would need to remove bottom anti-reflective coating (BARC) and resist materials from their substrates. One of the leading reasons that a device would need to have BARC and resist materials removed, or reworked, would be loss of critical dimension (CD) control. As feature sizes continue to shrink on devices, the CD must be accurately controlled on each wafer, as well as from wafer to wafer. Another reason for rework would be an incorrect overlay where the placement of the image does not line up with the underlying layers. A third reason for needing a rework process would be defect control. These issues, as well as many others, can cause electrical shorts in the device and can lead to yield loss.

Now that some of the reasons have been identified for rework processes, decisions must be made with regards to which layers must be removed in multilayer systems. There can be a variety of potential ways to rework multilayer stacks. The following diagram illustrates some of the potential ways to rework BARC and resist materials on multilayer stacks.



While there can be a variety of rework processes to choose from, this paper will focus on rework of the silicon material only and of the PR plus the silicon material, and on the rework of the via-filling material in a separate step. The rework of the PR layer by itself is not discussed in this paper due to the significant amount of prior art in the industry regarding this process.

2.2 Rework/Strip Materials

Several different commercial vendors provide many rework/strip materials. It is not the intent of this paper to push a specific material or vendor, but this paper will try to identify key elements of the removers and processes tested to gain knowledge in process development and defect reduction techniques. With the multitude of removers available, it was decided to make two classes of materials: acidic-based removers and basic-based removers. Other elements of the removers will be identified when possible, such as active ingredients, chelators, solvent type, etc. The following table identifies both similarities and differences among the different removers that were used for this experiment.

Remover	pH	Fluorides	Amines	Hydroxides	Organic Acids	Organic Solvents	BP (°C)
1	4.7	Yes	No	No	Yes	Yes	100
2	4.8	Yes	No	No	Yes	Yes	100
3	11.9	No	Yes	Yes	Yes	Yes	127
4	12.3	No	Yes	Yes	No	Yes	100
5	10.8	No	No	Yes	No	Yes	132
6	10.4	No	No	Yes	No	Yes	118
7	12.1	No	No	Yes	No	Yes	189
8	12.4	No	No	Yes	No	Yes	98
9	11.5	No	No	Yes	No	Yes	165
10	12.5	No	Yes	Yes	No	Yes	100
11	12.3	No	Yes	Yes	No	Yes	170

Even though some of the removers work for the BARC or PR materials in question, they must be tested further with regards to more stringent processing requirements (time and temperature), defect levels after rework, and susceptibility to attack of various substrate materials. The same removers were first looked at for compatibility with various substrate materials. Removers were selected for testing that were compatible with Al, Ti, W, TEOS, SiO_2, Black Diamond®, Black Diamond® II, Coral®, and SiN. The compatibilities of these various materials in each remover were tested at 60°C for 20 minutes. In order to be considered compatible, it was decided that <5 Å/min of thickness loss for each material was targeted.

2.3 Screening Studies

Before moving forward with using single wafer tools and more advanced processing, screening studies were conducted to determine applicable ranges with regards to time and temperature for removers and their corresponding BARC and PR materials. The silicon material (BSI.S06069), which was developed by Brewer Science, Inc., was coated on a variety of flat substrates (for example, polysilicon, Black Diamond®, Coral®, and SiN) to a nominal thickness of 70nm. The silicon material was baked at 205°C for 60 seconds. The PR material used was a leading 193nm resist with a nominal thickness of 150nm. The PR was baked at 130°C for 90 seconds. In order to test for "worst-case" scenarios, the PR was not exposed for the screening studies. The via-fill materials were coated nominally at 300nm and baked at 205°C for 60 seconds. The coated wafer pieces were submersed in each remover for an allotted time and at different temperatures. In order to ensure complete removal, the wafer pieces were measured both before the materials were coated on them as well as after removal. The following table shows the applicable times, temperatures, and results.

Remover	Time (min)	Temp (°C)	Silicon material	Via-fill 1	Via-fill 2
1	5	23	X	0	0
1	3	30	X	0	0
1	1	35	X	0	0
2	5	23	X	0	0
2	3	35	X	0	0
2	1	45	X	0	0
3	5	30	X	0	0
3	3	40	X	0	0
3	1	50	X	0	0
4	5	30	X	0	0
4	3	45	X	0	0
4	1	60	X	0	0
5	5	50	0	0	0
6	5	50	0	0	0
7	5	50	0	0	0
8	5	50	0	0	0
9	5	50	0	0	0
10	5	23	X	0	0
10	3	30	X	0	0
10	1	40	X	0	0
11	5	80	X	0	X
11	3	80	X	0	X
11	2	60	X	0	X

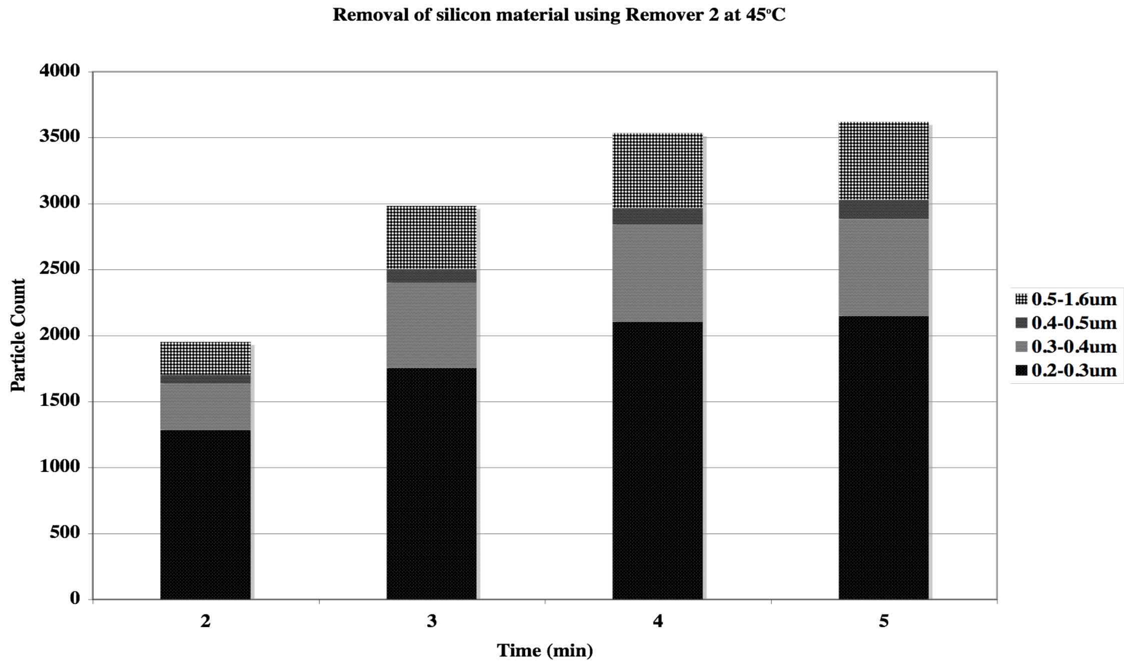
X represents fully clean
0 represents not clean

2.4 Single Wafer Tool Studies

Once the screening studies were completed, a selected number of removers were chosen to continue further experiments on single wafer tools to determine process requirements that would result in low defects after rework. Because differences exist among single wafer tools, processing requirements were specified to be

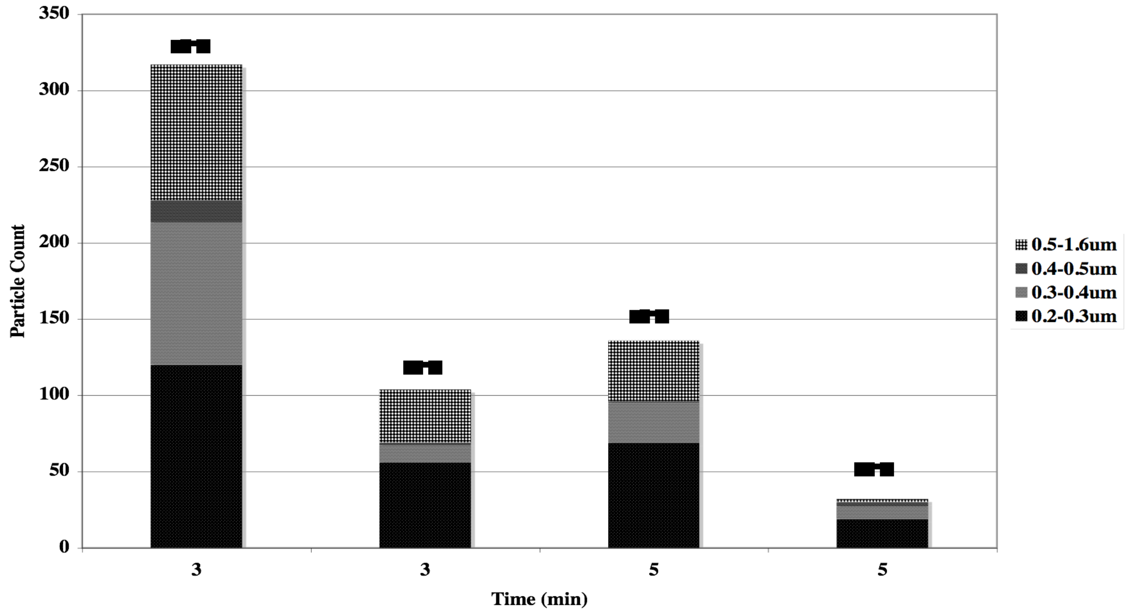
below 60°C for temperature and 5 minutes for time where materials were in contact with removers. These processing requirements were chosen since the majority of single wafer tools can process wafers at or below both the selected temperature and time.

The first removers to be experimented with on a single wafer tool were the acidic-based removers. Remover 2 was chosen to run the first set of experiments. It was first determined that the acidic-based removers did not remove PR or via-fill materials. Since this was the case, the silicon material was tested on flat 8-inch silicon wafers. The material was coated and baked under the same conditions as described above in the screening studies. The defects were measured on a Surfscan, with particle ranges from 0.25-1.6 microns.



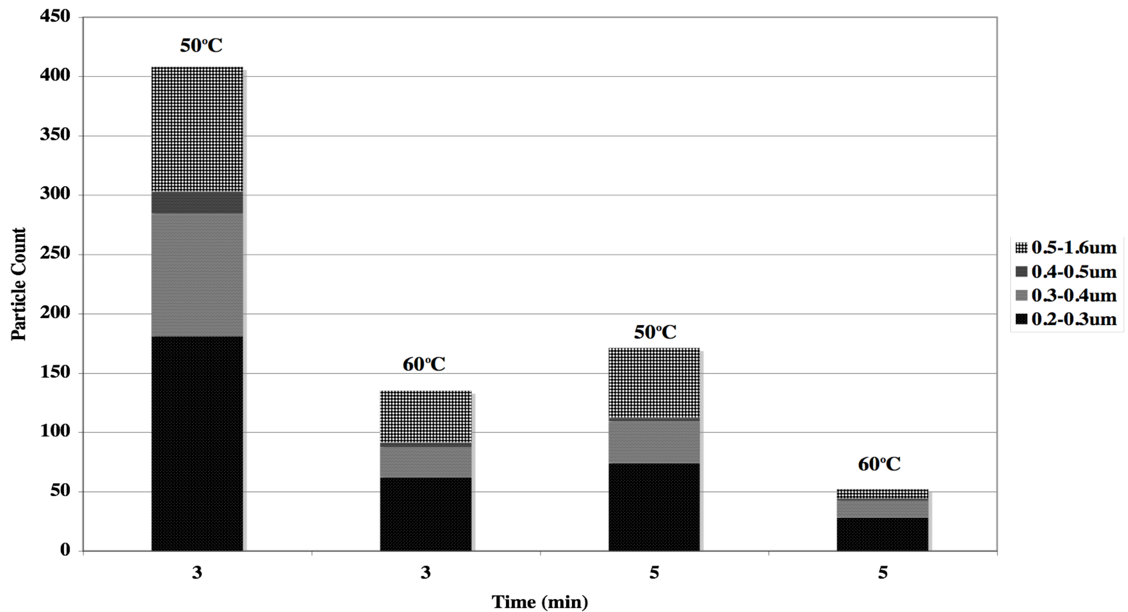
While both the screening studies and experiments on a single wafer tool proved that Remover 2 would completely remove the silicon material with regards to film thickness loss, a process could not be found to give low defects. While the formulation of Remover 2 was shown to be compatible with several different substrate materials, it was found that it could attack silicon in localized areas. This remover needs to be tested further using alternate substrates such as low-k or ultra-low-k dielectrics.

After determining that the acidic-based removers that were tested would only remove the silicon material and could attack silicon substrates, it was decided to move on to test the basic-based removers to see their removal efficiencies in single wafer tool type processes and in alternate removal processes. Set-up wafers were run first to determine the best two temperatures and times for the rework of the silicon material. The temperatures and times were determined by looking at thickness loss and total defect counts. The following graph shows total defect counts for the rework of the silicon material using Remover 3 at both 50°C and 60°C.



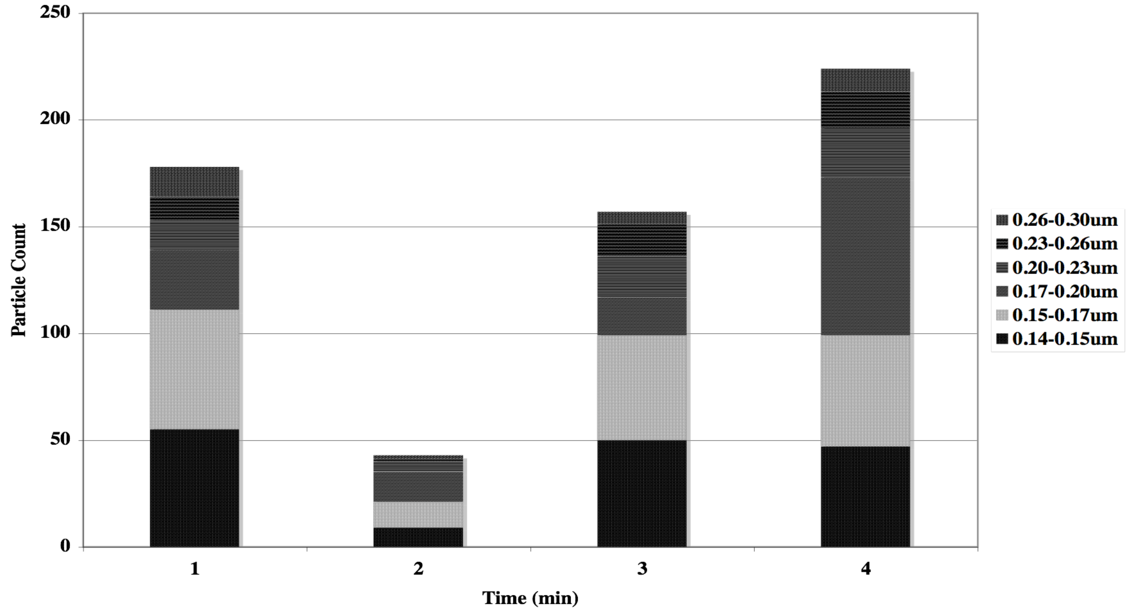
Since Remover 3 was able to remove the silicon material from silicon wafers (without damaging the wafer) and produce low defect levels, an alternate removal process was tested in which the PR was also removed in conjunction with the silicon material. The same temperatures and times were used to see how adding the PR layer would affect defect counts.

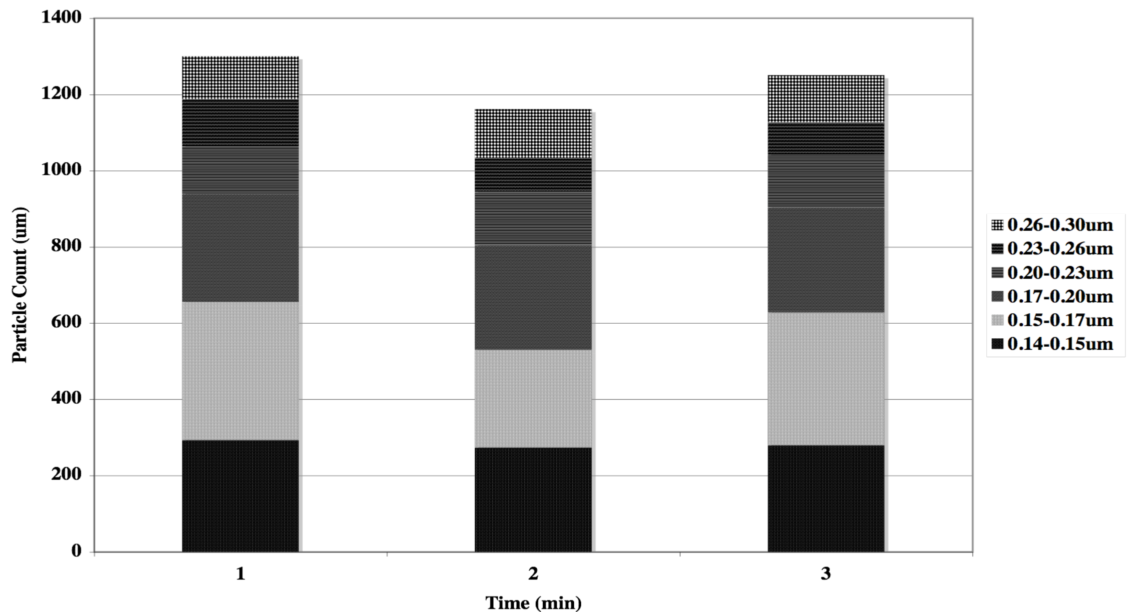
This experiment shows that Remover 3 will not only remove the silicon material, but it can also remove the silicon material and the PR at the same time. Further experiments would need to be conducted to find an optimal process to decrease the defect counts for advanced defect testing (<0.14um), but a reasonably



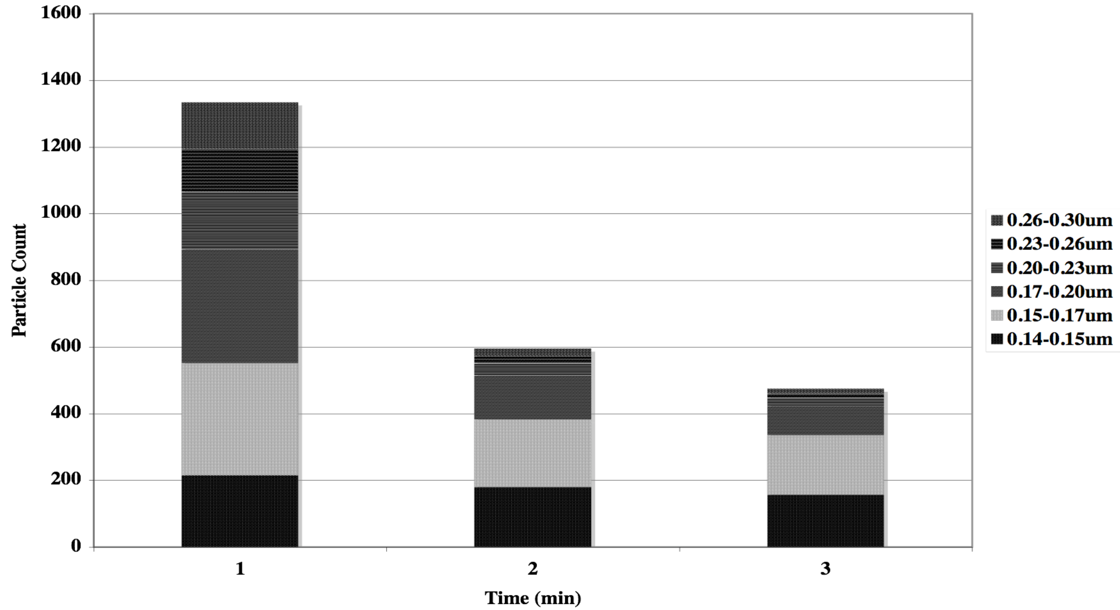
acceptable starting process has been identified.

Since the basic-based removers seemed to remove both the silicon material and the PR layer together, another basic-based remover was selected for defect studies. Remover 10 was selected because it also could remove the silicon material by itself or in conjunction with the PR layer. It was also found that Remover 10 could be used at 25°C, which is the ambient temperature of the clean room. The experiment was also able to use a KLA SP1 for more advanced defect analysis down to 0.14 micron. The following graphs show both the removal of the silicon material by itself, and then the removal of the silicon material in conjunction with the PR layer.





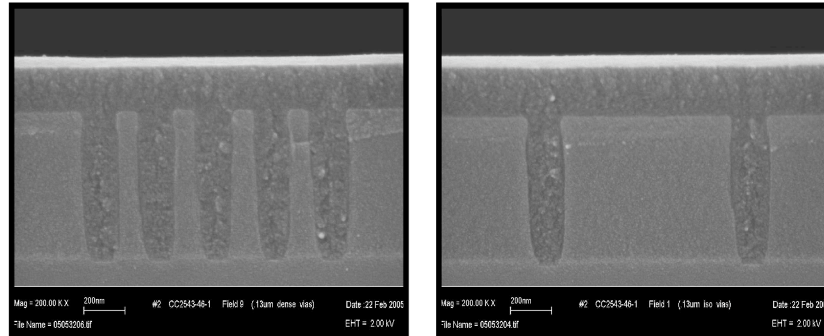
While Remover 10 was able to remover both the silicon material, as well as the PR layer and silicon material at the same time, the defect counts are noticeably higher when the PR layer was included. To see if a more suitable process could be found, the temperature of the rework solution was increased to 40ºC.



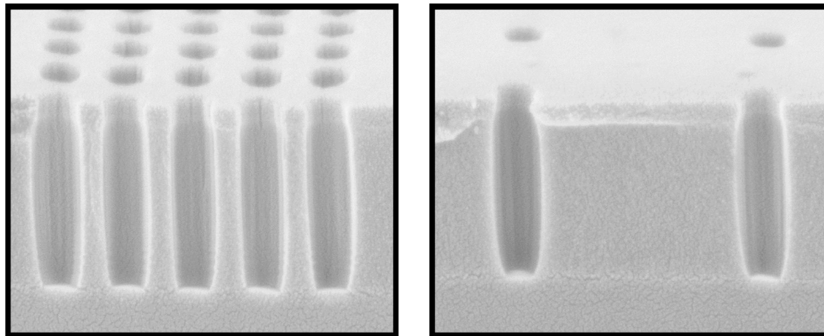
The increase in the rework solution temperature did reduce the defect counts, but they were still not as low as those resulting from the removal of the silicon material by itself. While the silicon material does have some organic components in it, Remover 10 has no trouble removing the coating with reasonably low defect counts. When the PR layer, which is totally organic, is included, Remover 10 has much more trouble removing both layers while maintaining low defect counts. Many questions remain as to why a specific remover works better than others for the removal of the multilayer materials in question. More specific information will need to be compared between removers to pinpoint why certain removers work better than others with regard to defects.

In most multilayer applications, the PR layer and silicon material will not have to planarize any topography, so they can be tested on flat substrates with regards to defects. On the other hand, the via-fill material will have to planarize a variety of via diameters and depths. To test for the removal of the organic via-fill material from vias, a Carl-Zeiss 1560 scanning electron microscope (SEM) was used to look at cross-sections of the vias before and after removal.

As coated



After removal



The testing was conducted using 130nm x 700nm vias that were Black Diamond® with a SiN cap. Remover 11 was used to remove the via-fill material. Further experiments need to be conducted to determine what temperature and time is needed to not only remove the material from the vias, but to also leave behind low defect counts. To date, it takes temperatures between 60 – 80°C to remove the via-fill material completely. While some single wafer tools can achieve temperatures this high, studies are underway to decrease process removal temperatures so it will be in line with a broad cross section of the single wafer tool industry and customer requests.

2.5 Future Work

Much more work must be completed to thoroughly understand remover and multilayer material interactions. More work also must be completed in the area of advanced defect analysis. While it could suffice to start studies analyzing defects in the ranges presented in this paper, further analysis of defects (<80nm) will need to be tested in order to provide device manufacturers with appropriate information and data. Work must also be completed in other process areas such as the rinse and dry step during the entire single wafer process.

2.6 Summary

As the semiconductor industry continues to shrink feature sizes of their devices, rework processes are also trying to keep up with design and material changes. As device manufacturers start to look at multilayer materials, rework materials and processes need to be identified. Experiments conducted looked at a variety of different removers and their efficiencies of removing specific multilayer stacks. The goal of the experiments was to determine rough process requirements that would ensure complete removal of materials in question and also to determine any trends in defect levels after removal. It has been shown that the multilayer materials in question can be removed in various ways that will give device manufacturers options when and if problems arise and rework processes must be used.