Cadence Palladium XP II Verification Computing Platform

The Cadence® Palladium® XP II verification computing platform is the next-generation state-of-the-art hardware-assisted verification platform. Building on the successful Palladium XP platform, the Palladium XP II platform offers higher capacity, better performance, faster upload speeds, improved debug, and best-in-class simulation acceleration and emulation capabilities in a single environment to boost verification throughput and productivity. Its processor-based compute engine and Unified Xccelerator Emulator (UXE) software offers fast and predictable compiles, runs high-performance verification applications and enables flexible new use models that transcend traditional emulation.

System-Level Verification Challenge

Traditional verification tools have not kept pace with the rapid rate at which system-on-chip (SoC)/ASIC design size and complexity are growing. This widens the hardware/software verification gap, limiting reusability and productivity, resulting in an increased likelihood of re-spins and schedule delays. As RTL/gate design size increases, traditional simulators slow down significantly, which delays hardware/software (system) integration and prolongs the overall verification cycle.

Today's SoC designs can be complex (see Figure 2). As systems grow more sophisticated, the risk associated with not adequately verifying hardware/software interaction also grows. Scalable performance is critical to eliminating these risks. Traditional hardware-assisted verification tools can take you outside of your native simulation environment with steep learning curves, lengthy setup times, difficult debug methods, and reuse issues. Furthermore, there is no easy way to transition among simulation, simulation acceleration, and emulation environments without re-compilation.

Figure 1: Palladium XP II platform

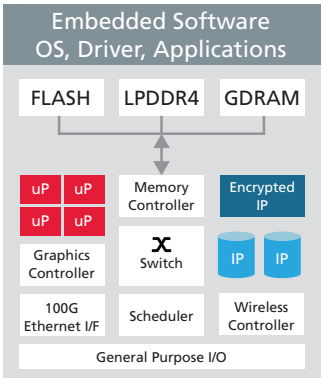

Figure 2: This example SoC design includes hardware and software.

System-Level Verification Solution

To keep pace with the demands of advanced SoC development and to close the hardware/software verification gap, the Palladium XP II platform offers the industry's most comprehensive verification platform. The Palladium XP II platform enhances the verification flow and capabilities and removes the barrier to entry in acceleration and emulation by offering a unified environment that

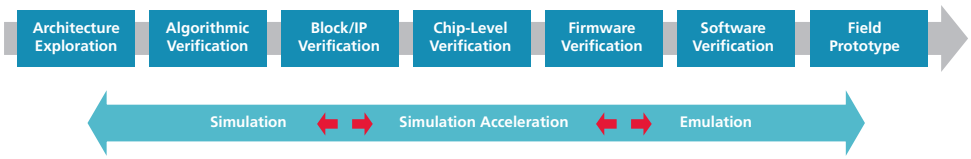

Figure 3: The Palladium XP II platform offers an enhanced, unified flow and allows users to transition between simulation, simulation acceleration, and emulation for better performance and enhanced debug.

leverages the native simulation environment. The environment also allows a Cadence Incisive® simulator user to hot-swap among simulation, simulation acceleration, and emulation environments at runtime without re-compilation (Figure 3). The Palladium XP II platform can be used at various design and verification phases, from early architectural analysis to block, chip, and system-level integration to software development and system verification.

The Palladium XP II platform offers enhancements above and beyond what traditional acceleration and emulation use models offer. The Palladium XP II platform introduces new use models to improve verification productivity through metric-driven verification acceleration (MDV), hardware verification language-based testbench acceleration, in-circuit acceleration (ICA), Universal Verification Methodology (UVM) acceleration, vector-based acceleration (VBA), comprehensive coverage capabilities, Power Shutoff Verification (PSO), and Dynamic Power Analysis (DPA), among others for RTL and gate-level emulation (Figure 4).

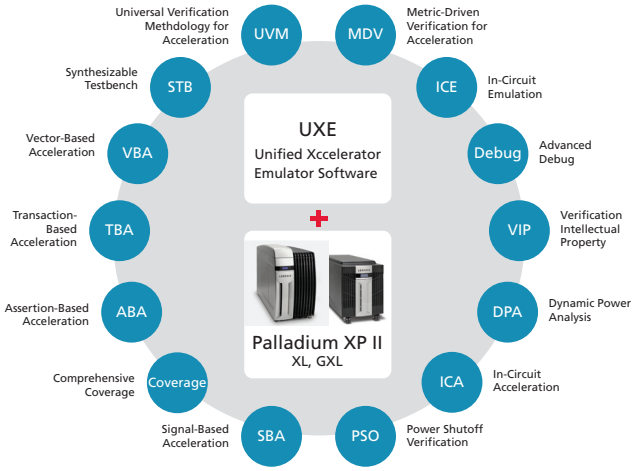

Figure 4: Palladium XP II platform offers comprehensive use models for hardware/software co-verification and system realization across RTL and gate-level designs

Palladium XP II Features

Highest scalability and flexibility

- Enables centralized or locally distributed verification computing with scalable resources to serve a single user or as many as 512 simultaneous users for up to 2.3 billion gates capacity
- Supports flexible executable functional models at various abstraction levels (C/C++, SystemC®, instruction set or cycle accurate, silicon, RTL, gates)

Unparalleled verification computing productivity

- Enables quick bring-up with its fast, automated, intelligent compiler that includes a rich set of behavior construct support and congruent (match) behavior between simulation and hardware

Better design bring-up predictability

- Boosts runtime predictability with "hot-swap" to acceleration or emulation and the most flexible use models
- Enables quick system-level bring-up with the comprehensive and proven Cadence SpeedBridge® portfolio (comprising hardware rate adapters for standard protocols)

Platform extension

- Supports metric-driven verification for acceleration with coverage and advancements in hardware verification/hardware design languages
- Supports the most comprehensive emulation and acceleration VIP for standard protocols
- Enhances system-level low-power analysis with DPA option and power-verification techniques such as power shutoff

Superior debug capabilities

- Supports advanced debug capabilities like SDL trigger, FullVision, Dynamic Probes, Infinitrace, continuous waveform upload, etc. to identify any design bugs

Comprehensive Verification Computing Platform

The Palladium XP II compute engine comprises an advanced custom processor grid. Each processor includes multimillion transistors embedded in multi-chip modules (MCMs). This processor grid allows the Palladium XP II platform to support up to 2.3 billion ASIC gates of design capacity, supporting a single user or up to 512 simultaneous users, and running up to 4MHz.

The UXE software component of the Palladium XP II platform integrates simulation and acceleration in a single environment, thereby enabling fast bring-up, superior debug, hot-swap capability, and fast, fully automated, predictable design compile on a single workstation.

Flexible Resource Allocation and Model Support

The Palladium XP II platform offers verification computing resources with best-in-class flexibility for an enterprise. It can be utilized for multiple projects/tests as it can support multiple concurrent jobs, including those with a mixture of acceleration and emulation, without affecting other jobs. Users can set-up

jobs queuing for regression or interactive use, and can relocate jobs to other available symmetrically configured resources (MCMs, memories, I/Os) without re-compilation. Furthermore, users can respond to on-demand resource allocation requirements as project needs evolve.

A highly flexible verification platform is critical to assemble the SoC rapidly. The Palladium XP II platform allows rapid integration of various abstracted IP models on the basis of performance, accuracy, availability, reuse, hard/soft IP, or legacy environment-support requirements. It supports industry interface standards such as the Standard Co-Emulation Modeling Interface (SCE-MI), SystemVerilog DPI, and Virtual Interface (VIF), which provide even more flexibility in expanding the system-level verification environment.

Since the Palladium XP II platform supports concurrent use of different types of IP, testers, debuggers, and test stimulus generators, it significantly reduces the development schedule (Figure 5). Users can comprehensively verify system interactions with a real-world environment and/or a testbench for a directed, constrained-random, or metric-driven verification environment while significantly improving verification throughput.

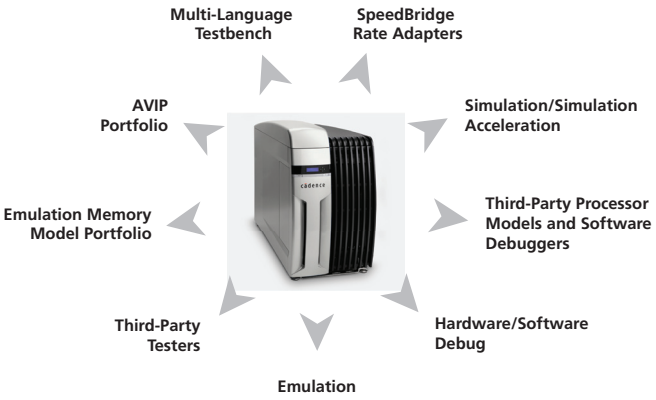

Figure 5: The Palladium XP II platform allows concurrent use of different types of models

Power analysis

The Palladium XP II platform offers system-level power verification in which the common side file is read to help designers verify power intent through the integrated SimVision waveform viewer and log file messages.

- **Dynamic Power Analysis (DPA):** Identifies "true peaks" during long runs, which are often not captured in simulation. Integration of Cadence Encounter® RTL Compiler power estimation engine with Palladium XP II provides the first high-performance, cycle-accurate, integrated solution delivering full-system power analysis of hardware/software designs
- **Common Power Format (CPF):** Specifies the low-power intent modeled into CPF so low-power activities can be captured and shown in waveform for debugging. Also aids in effective low-power verification including memory/flip-flop (FF) randomization after power shut off (PSO).

Advanced Debug

The Palladium XP II platform enhances the design debug process with its easy-to-use, high-performance debug features. The Palladium XP II advanced debug also supports hardware/software co-verification and various assertions languages.

Feature	Specification
FullVision	• At-speed full visibility of any nets for typically up to 2 million samples during runtime
Dynamic Probes	• Fast waveform upload of up to 80 million samples • Select signals to analyze before run
Infinitrace	• Unlimited trace-capture depth • Allows users to revert back to any checkpoint and restart emulation from that point
State Definition Language (SDL)	• Allows simple or complex trigger on set of events • Dynamic netlist creation for accurate trigger mechanism without recompilation
Save and Restore	• Save valuable cycle time and restore run from a "save" point. (e.g., OS boot completion)

Ecosystem support

- High-level synthesis with C-to-silicon compiler to further accelerate verification early in the design cycle and enable hardware/software co-development with significantly less effort
- Accelerated VIP and In-Circuit Emulation to enable system-level and application software testing prior to silicon availability. Includes full compatibility with the SpeedBridge hardware adapter product that connects real-world systems with the design being emulated to provide simple and direct integration
- Hybrid environment of hardware and software to have an efficient hardware/software debug, faster boot, and early software/system validation with RTL
- Metric-driven verification acceleration, and Embedded Test Bench (ETB) to enable users to follow a comprehensive plan-to-closure methodology that increases verification predictability, productivity, and quality

Specifications

	Palladium XP II (XL)	Palladium XP II (GXL)
Scalable capacity and I/O	• Capacity: Up to 72 million gates • I/O: Up to 3,072 • CMOS 3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL	• Capacity: Up to 2.3 billion gates • I/O: Up to 147,456 • CMOS 3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL
Default dedicated user memory	Up to 32GB	Up to 2TB
Simultaneous users	From 1 to 8 users	From 1 to 512 users
Architecture	Custom advanced processors (MCMs)	
Design format and language support	• HDL: RTL (VHDL, Verilog, SystemVerilog) and gate-level netlist • HVL: C++, SystemC, Specman '***e***', SystemVerilog, and Universal Verification Methodology (UVM) acceleration • Assertions: System Verilog Assertions (SVA), Property Specification Language (PSL), Incisive Assertion Library, and Open Verilog Library (OVL)	
Memory transformation and Memory Model Portfolio (MMP)	• Options for memory placement, compaction, squeezing, read port splitting, and merging • Comprehensive portfolio supports most industry-standard memory models	
Hardware/software interfaces, connecting to third-party tools/IP/ environment	• Various standards: SCE-MI 2.X and TLM support • Most comprehensive SpeedBridge and Accelerated VIP portfolio for standard protocols supporting most market segments • Application-specific interfaces: C/C++, PLI, VPI, SystemVerilog DPI, DPI-SystemC, VHPI, etc. and support for third-party interfaces to the standalone UXE model	
Fast compile	Up to 75 million gates per hour with a single workstation for RTL	
Performance	Up to 4MHz, with built-in profiler that tunes performance for acceleration	
Advanced debug and low-power verification	FullVision, Infinitrace, Dynamic Probes, continuous waveform upload, SimVision, SDL, Dynamic Power Analysis, etc.	
Flexible clocking	Supports a very large number of synchronous, asynchronous, and gated clocks	

Supported Workstations and Operating Systems*

- X86 instruction set architecture workstations
- OS type: Linux
  - RHEL 5 (32-bit and 64-bit), RHEL 6 (32-bit and 64-bit)
  - SuSE 11 (64-bit)

** Please check with your Cadence representative for the latest information and additional details as they are subject to change without notice.*

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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