SpeedBridge Adapter for PCI Express 3.0

System emulation under real-world operating conditions

The Cadence® SpeedBridge® adapter for PCI Express® (PCIe®) 3.0 provides efficient driver and application-level testing. Designed for pre-silicon RTL and integration of PCIe-based ASICs and systems on chip (SoC), the solution can reproduce post-silicon bugs, as the design runs in the actual target system. The solution verifies emulated PCIe 3.0 designs with the actual ASIC/SoC software/hardware, driver development, and application development, and runs with existing software and software test programs.

Addressing Verification and Integration in PCIe Devices

PCIe is a high-bandwidth, low-pin-count serial interconnect technology that also maintains software compatibility with older PCI infrastructure. It's uniquely positioned as the logical interconnect technology for today's products.

With the SpeedBridge adapter, you can address the verification and integration needs for your PCIe devices. The solution consists of an interface card and emulator-resident Verilog wrapper that transparently convert a standard PCIe interface into an emulation-speed PCIe interface (see Figures 1 and 2). The plug-and-play card is compatible with standard PCs, workstations, and most embedded PCIe platforms without requiring modification. It performs rate adaptation so the emulated PCIe device can connect to a full-speed PCIe device. For example, an emulated root complex can connect to the full-speed endpoint cards.

The SpeedBridge adapter connects directly to a Cadence Palladium® emulator through standard emulation cables and adaptors. It is designed to be functionally transparent to both the PCIe 3.0 host or device. As a result, most software applications and device drivers developed for the device under test (DUT) can be used without modification in the PCIe test environment. Given the high speed of in-circuit emulation, you can co-verify hardware and software together with software drivers before the real silicon. Due to the billions of cycles that it consumes, software debug with RTL simulation is not practical. Cadence emulators provide the advanced hardware/software debug capabilities needed for ease of use, ease of debug, and high speed—without sacrificing quality. The solution also supports quick system bring-up, allowing application-based traffic running in a short span of time.

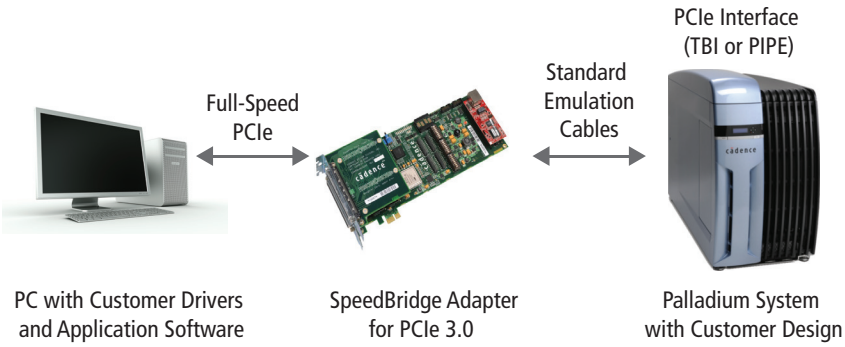

Figure 1: System components for endpoint emulation

Benefits

- Enables rapid emulation deployment
- Enables verification IP reuse
  - Works from one project to another
  - No need for every user to create custom solutions
  - Improves productivity to get to the first test by leveraging existing applications, third-party software tools, and more
  - Eliminates the need to set up a complex FPGA-based environment

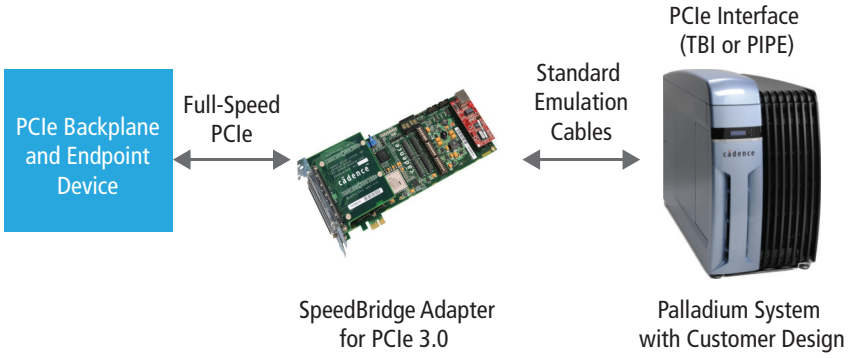

Figure 2: System components for root complex

- Ensures quality
  - Mature technology, tested and verified by Cadence and many other user designs
  - Verifies designs quickly and efficiently
  - Provides a single-card solution
- Reduces system risk
  - Checks PCIe protocol and integrity errors (CRC)
  - Verifies the PCIe design in a real environment and the future system platform
  - Boots OS system
  - Runs real system software/drivers
  - Increases confidence in PCIe device quality
  - Reduces time to market

Features

- Compliant with PCIe Base Specification V3.0
- Enables emulation of root complex, endpoint, switch, and bridge devices
- Compatible with non-SSC/SSC (spread spectrum clock) PCIe 3.0 platforms
- Supports link-speed negotiation of 2.5Gbps, 5.0Gbps, or 8.0Gbps with the emulated PCIe 3.0-capable designs
- Supports SR-IOV
- Supports power management states:
  - L0—Normal mode
  - L0s—Link suspended
  - L1 and L1 substates with CLKREQ#—low-power state
- Multiple lanes
  - Support for 1x, 2x, 4x, 8x, and 16x lanes
- Works with emulation speed of up to 12MHz
- Backward compatible with PCIe 2.0, 1.1, and 1.0a-based designs
- Connects an emulated PCIe 3.0 device to a full-speed (2.5Gbps) PCIe interface
- Functionally transparent to most software driver or operating systems
- Real PCIe driver environment
  - Installs in PCIe host platforms or backplanes when emulating an endpoint device
- Enables early debug with first silicon and first software
  - Concurrent software development and hardware/software co-verification
- Debug capabilities
  - Fully static implementation supports key emulation debug features
  - Support for logic analyzer debug capabilities
- Includes SpeedBridge Configuration Manager software, which runs on your PC to remotely monitor the PCIe interface status
- For detailed information, email cva_support@cadence.com

Specifications

The SpeedBridge adapter supports:

- Memory, I/O, configuration, and message transactions
- Requests and completions
- Complete PHY-level link initialization including TX equalization
- System-driven, credit-based flow control
- PCIe PHY-level 10-bit and 20-bit interfaces as well as standard PIPE in either 8-bit, 16-bit, or 32-bit mode
- One virtual channel (VC) and one traffic class (TC)
- Payloads from 128-byte to 4096-byte
- Legacy and non-legacy devices
- Lane reversal and polarity inversion
- Extended configuration space
- Transaction ordering driven by host platform
- Multiple read completion

Requirements

- One SpeedBridge adapter for PCIe 3.0 for each emulated PCIe interface
- A PC or workstation with one or more PCIe slots—one slot for each SpeedBridge solution used for emulation endpoint devices
- A PCIe backplane for emulation of root complex devices
- System using Cadence Incisive® and Palladium series solutions
- Device drivers and/or application software required by the emulated ASIC/SoC
- Emulator-resident verilog wrapper for SpeedBridge adapter for PCIe 3.0
- One Ethernet CAT5 cable for connecting SCM
- Requires 1 HDDC

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. **www.cadence.com**

© 2015 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, Incisive, Palladium, and the Cadence logo are registered trademarks and SpeedBridge is a trademark of Cadence Design Systems, Inc. in the United States and other countries. PCI-SIG, PCI Express, and PCIe are registered trademarks and/or service marks of PCI-SIG. All other trademarks are the property of their respective owners. 4146 03/15 SA/DM/PDF