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Protium S1 FPGA-Based Prototyping Platform

The fastest way to prototype your ASIC

The Cadence® Protium™ S1 FPGA-Based Prototyping Platform is an advanced FPGA-based prototyping solution enabling early software development, throughput regressions, and high-performance system validation. It combines high-capacity FPGA boards, based on the latest generation of FPGAs, with a complete implementation and debug software flow, providing ultra-fast design bring-up and unprecedented ease of use. Compatible with Cadence's Palladium® platforms and SpeedBridge® adapters, it allows for the quick and smooth transition of the system-on-chip (SoC) design from an existing emulation environment into a high-performance FPGA-based prototype.

Early Software Development

Successfully completing today's and tomorrow's challenging SoC designs, with their ever-increasing software contents, on time and on budget, requires starting the software-development process as early as possible. FPGA-based prototyping has long been a key technology to achieve that goal. However, growing complexities and shrinking time-to-market windows are making the bring-up of such a prototyping system increasingly painful and time consuming.

The Protium S1 platform addresses and solves these challenges by providing a comprehensive and productive solution to reduce the prototype bring-up from months to weeks. This speed-up is achieved by combining a hardware platform—a family of FPGA boards—with a software platform, providing a fully integrated implementation flow as well as advanced debug capabilities.

System Validation

With their high speed, small form factor, and external system connections, FPGA-based prototyping systems are a productive solution to allow design teams to validate their IP and SoC designs within the actual system environment. With its fast design bring-up and compatibility with the SpeedBridge portfolio, the Protium S1 platform offers distinct advantages over in-house-developed and other FPGA-based solutions.

Throughput Regressions

Using the Protium S1 platform, you can improve your product quality by running exhaustive regression tests on a high-performance, cost-effective platform.

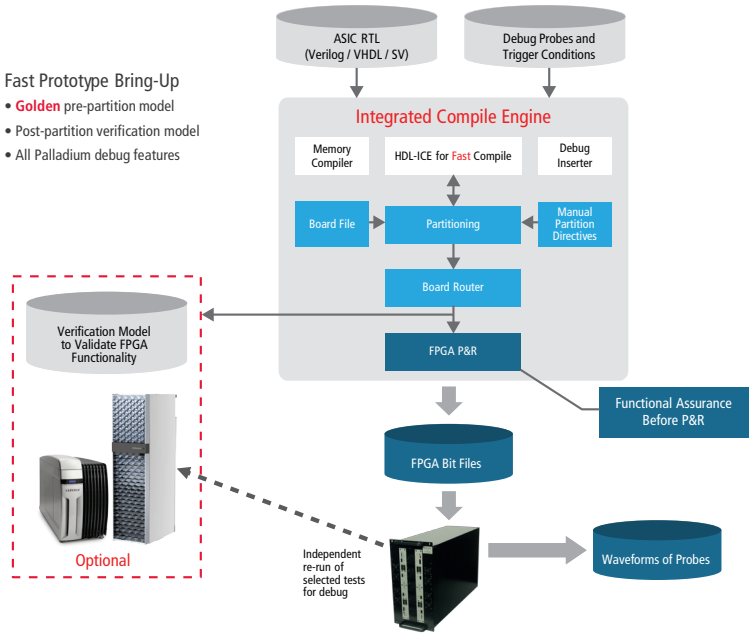

Figure 1: Protium S1 flow

When the majority of hardware defects in the design have been removed, users must be able to run regressions quickly, while preserving the integrity of the design under test (DUT) and the verification environment. To optimize the throughput of regression speed within budget, pair the Palladium XP Verification Computing Platform and the Palladium Z1 Enterprise Emulation Platform—including a common compile flow, identical language coverage, and the ability to re-use the Palladium verification environment—with the Protium S1 platform. This approach allows users to maximize throughput regressions, which requires less interactive hardware debugging.

The Protium S1 platform further extends the innovation within the Cadence Verification Suite—comprised of best-in-class core engines, verification fabric technologies and solutions that increase design quality and throughput—fulfilling verification requirements for a wide variety of applications and vertical segments.

Benefits

Fastest prototype bring-up

- Reuse of the existing Palladium emulation environment
- Automatic multi-FPGA partitioning
- Automatic memory conversion and modeling
- Support for unlimited number of design clocks

Highest model accuracy

- Support for complex, ASIC-style clocking
- Palladium platform-compatible clocking
- Automatic generation of a post-partitioning verification database for fast model validation

Unparalleled debug

- Waveform capture and storage for off-line debug and analysis
- Signal force and release for interactive debug and design configuration
- Memory upload/download to quickly update design boot image and memory content
- Full clock control including start/stop and run “n” cycles, enabling advanced verification use modes and automation
- Palladium platform compatibility for interactive debug and root-cause analysis

Unsurpassed flexibility

- Boards are equipped with the most common, standard interfaces
- Expansion connectors for custom and off-the-shelf daughtercards
- Compatible with SpeedBridge adapters
- Support for end-to-end encryption (e.g., to protect third-party IP)

Features

Complete FPGA-based prototyping system with all required hardware and software components.

Design input

- Synthesizable RTL (Verilog, VHDL, System Verilog)
- Synthesizable gate-level netlist
- Full support and compatibility with the Palladium language set (synthesizable constructs only)

Scripting and setup

- Compatibility with Palladium script files
- Compatibility with Palladium clock definition files
- Automatic ASIC-to-FPGA memory conversion

Multi-FPGA partitioning

- Fully automatic with FPGA interconnect optimization and FPGA utilization balancing
- User-guided performance optimization
- Black-box support for high-speed design modules and interfaces
- Automatic clock tree transformation (gated clocks, multiplexed clocks, latches, etc.)
- Automatic pin-multiplexing insertion

Post-partitioning Palladium model

- Generated automatically
- For fast FPGA model validation
- Accurate representation of the multi-FPGA implementation including clock remapping, converted memories, pin-multiplexing, probing, and triggering logic, etc.

FPGA place and route

- Fully automatic setup
- Support for parallel place and route
- Fully integrated Xilinx Vivado Place and Route software

Integrated Compile Engine

Taking an ASIC design (RTL) and mapping it into a set of FPGAs is without any doubt the biggest challenge and the most time-consuming task when getting an FPGA-based prototype up and running. Unlike other solutions, the Integrated Compile Engine in the Protium S1 platform provides everything needed to take an existing RTL design, compile it, partition it into multiple FPGAs, and generate the individual bit files to configure each FPGA. This can be done fully automatically with minimal or no modifications to the original ASIC-RTL code. Various levels of specific user guidance and interaction allow further optimization, specifically to achieve higher speed.

To provide visibility into the design and interactive debug capabilities during runtime, the user can select the to-be-observed signals before compilation and define the trigger conditions to start a data capture. During runtime, the selected signals are captured and stored for off-line viewing and analysis.

In addition, several unique debug capabilities are at the user’s disposal, ranging from back-door memory upload/download over the ability to force signals into “1” or “0” to being able to start/stop the clock or run “n” cycles.

Protium S1 Hardware

To cover a wide range of design sizes and accommodate different interface requirements, multiple hardware configurations are available, ranging from two FPGAs per system to eight FPGAs per system. All FPGAs are Xilinx Virtex-Ultrascale XCVU440 devices providing up to 25M ASIC gates capacity (design dependent) and up to 88Mb of embedded memory per FPGA. The boards are mounted in a custom chassis with power supply, cooling, and all necessary interfaces and cabling included.

In addition to being equipped with a variety of on-board interfaces, the Protium S1 platform is complemented by a comprehensive portfolio of daughtercards. The Protium S1 platform is also fully compatible with Cadence's family of SpeedBridge adapters, enabling a smooth transition from an emulation environment to an FPGA-based prototyping environment.

Requirements

For compile

- Linux operating system (Refer to Platform Matrix for Cadence Applications)
- Minimum of 64GB of RAM
- Minimum of 500GB of free disk space

For control and configuration

- Linux workstation (32-bit or 64-bit, Red Hat or SUSE)
- 64GB of RAM
- 45GB of disk space
- 1 Ethernet port
- 1 USB 2/3 port
- Multiple Protium S1 Platforms can be controlled from one workstation

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/training

Protium S1 FPGA-Based Prototyping Platform — Hardware Configurations

	39RX811K (Board Only)	39RX812K	39RX814K	39RX828K
FPGAs	1X Virtex Ultrascale XU440	2X Virtex UltraScale XU440	4X Virtex UltraScale XU440	8X Virtex UltraScale XU440
FPGA boards	1	1	1	2
Approx. total capacity (design dependent)	Up to 25M ASIC gates	Up to 50M ASIC gates	Up to 100M ASIC gates	Up to 200M ASIC gates
FPGA-internal memory	88Mb	176Mb	352Mb	704Mb
On-board memory (optional)	Up to 32GB	Up to 64GB	Up to 128GB	Up to 256GB
Front-panel interfaces	PCI Express® (PCIe®) Gen3 (X8) iPass, USB Host, FPGA JTAG, CPU Ethernet, CPU Serial, CPU Device, JTAG • 1X 4-lane PCIe Gen3 • 8X SFP+ • 2X QSFP+	• 2X 4-lane PCIe Gen3 • 8X SFP+ • 2X QSFP+	• 1X 4-lane PCIe Gen3 • 8X SFP+ • 3X QSFP+	• 2X 4-lane PCIe Gen3 • 16X SFP+ • 6X QSFP+
Back-panel Interfaces	• 1X 4-lane PCIe Gen3 • 8X SFP+ • 2X QSFP+	PCIe Gen3 (X8) iPASS, USB Host, FPGA JTAG, CPU Ethernet, CPU Serial, CPU Device, JTAG, UART		
On-board interfaces	• 2X SATA II (1X Device/1X Host) • 1X JTAG (14-pin) • 1X RS232	• 8X SFP+ • 2X QSFP+ • 4X SATA II (2X Device/2X Host) • 1X JTAG (14-pin) • 1X RS232	• 8X SFP+ • 2X QSFP+ • 8X SATA II (4X Device/4X Host) • 1X JTAG (14-pin) • 1X RS232	• 16X SFP+ • 4X QSFP+ • 16X SATA II (8X Device/8X Host) • 2X JTAG (14-pin) • 2X RS232

Protium S1 FPGA-Based Prototyping Platform — Hardware Configurations (Continued)				
	39RX811K (Board Only)	39RX812K	39RX814K	39RX828K
GTH expansion connector	• 1X GTH connector • 16 SerDes (16Gbps) Each GTH connector supports: 16-lane PCIe (Gen1/Gen2/Gen3) • 2X 4-channel Ethernet, XAUI, Infiniband • 16X SFP+ 10GbE et. al. • 4X QSFP+ 4 channels 10 GbE or single-channel 40 GbE • 16X USB3.0/2.0 A, AB, B 16X Serial ATA II (SATA II) 16X SMA	• 2X GTH connectors (1X GTH connector per FPGA) • 16X SerDes (16Gbps) per FPGA Each GTH connector supports: 16-lane PCIe (Gen1/Gen2/Gen3) • 2X 4-channel Ethernet, XAUI, Infiniband • 16X SFP+ 10GbE et. al. • 4X QSFP+ 4 channels 10 GbE or single-channel 40 GbE • 16X USB3.0/2.0 A, AB, B • 16X Serial ATA II (SATA II) • 16X SMA	4X GTH connectors (1X GTH connector per FPGA) 16X SerDes (16Gbps) per FPGA Each GTH connector supports: 16-lane PCIe (Gen1/Gen2/Gen3) • 2X 4-channel Ethernet, XAUI, Infiniband • 16X SFP+ 10GbE et. al. • 4X QSFP+ 4 channels 10 GbE or single-channel 40 GbE • 16X USB3.0/2.0 A, AB, B • 16X Serial ATA II (SATA II) • 16X SMA	• 8X GTH connectors (1X GTH connector per FPGA) 16X SerDes (16Gbps) per FPGA Each GTH connector supports: 16-lane PCIe (Gen1/Gen2/Gen3) • 2X 4-channel Ethernet, XAUI, Infiniband • 16X SFP+ 10GbE et. al. • 4X QSFP+ 4 channels 10 GbE or single-channel 40 GbE • 16X USB3.0/2.0 A, AB, B • 16X Serial ATA II (SATA II) • 16X SMA
Clock generators	5 programmable synthesizers (2KHz – 945MHz)			10 programmable synthesizers (2KHz – 945MHz)
Samtec SEAM series connector	24 connectors: Each connector connects to 52 I/Os that can be configured as 24 LVDS + 4 single-ended signals or 52 single-ended signals	36 connectors (18X connectors per FPGA) Each connector connects to 52 I/Os that can be configured as 24 LVDS + 4 single-ended signals or 52 single-ended signals	48 connectors (12X connectors per FPGA) Each connector connects to 52 I/Os that can be configured as 24 LVDS + 4 single-ended signals or 52 single-ended signals	96 connectors (12X connectors per FPGA) Each connector connects to 52 I/Os that can be configured as 24 LVDS + 4 single-ended signals or 52 single-ended signals
User I/Os	576 LVDS pairs or 1,248 single-ended signals	864 LVDS pairs or 1,872 single-ended signals	1,152 LVDS pairs or 2,496 single-ended signals	2,304 LVDS pairs or 4,992 single-ended signals
Board configuration	Ethernet, USB			
Power requirements	500W, ATX 24-pin connector P1, 12V/36A, 5V/2A, 3.3V/15A	110-240VAC, 50-60Hz, 500W	110-240VAC, 50-60Hz, 750W	110-240VAC, 50-60Hz, 1,500W
Dimensions	381mm x 32mm x 446mm (width x height x depth)	445mm x 254mm x 762mm (width x height x depth); 19" standard rack mountable, 7u height		

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