

Cadence SpeedBridge Adapter for ARM Logic Tiles

High-performance emulation and HW/SW co-verification

The Cadence® SpeedBridge® Adapter for ARM® Logic Tiles allows a design emulated in a Cadence Palladium® series system to interface with a full-speed ARM Logic Tile. It enables hardware/software co-verification, early verification of embedded software (prior to hardware prototype), and IP reuse, helping engineers boost their productivity while reducing system risk.

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ARM emulation solution

As SoC designs continue to increase in size and complexity, verification becomes increasingly time-consuming. Acceleration and emulation enable more comprehensive validation of a design than simulation alone, and they allow you to develop software before final silicon availability. The introduction of the ARM Logic Tile offers developers of firmware, software, and hardware a scalable SoC prototyping solution integrated with the ARM Integrator family of development boards.

Building SoC prototypes with ARM Integrator boards eliminates the need for you to design your own FPGA prototyping boards for each project. The Integrator Logic Tile product helps designers deliver secure FPGA prototypes of SoC and platform designs through encryption of the FPGA configuration information.

Developers will benefit from the scalability of the tile design, where FPGA capacity can be increased by

simply adding another Logic Tile product without the need for swapping FPGA or re-designing the board.

Powerful in-circuit verification

The Cadence SpeedBridge Adapter for ARM Logic Tiles connects a Palladium series acceleration/emulation system, such as the Palladium XP Verification Computing Platform, to an ARM Logic Tile (LT). The ARM LT is configured for the ARM-synthesizable CPU core that the design is using. After the design is downloaded into a Palladium XP, you can connect a software debugger via JTAG, which connects through a special API.

With the high speed of in-circuit emulation, you can co-verify hardware and software (HW/SW) with application software running using an ARM LT. You can have both HW/SW debug tools you need for ease of use, ease of debug, and high speed, so you don't have to sacrifice quality. Cadence provides leading-edge HW/SW debug technology and methodology.

Benefits

Improved productivity

- Offers a high-performance emulation solution for ARM processor cores
- Enables HW/SW co-verification with software running on the ARM processor

Rapid emulation deployment

- Delivers an off-the-shelf SoC platform verification solution
- Seamlessly integrates ARM cores with Palladium in-circuit emulation capabilities

Early HW/SW integration

- Enables verification of embedded software with hardware model of ARM core as soon as RTL is available

IP reuse

- Delivers a solution that works from one project to another
- Saves time and reduces complexity by eliminating the need for every user to re-invent the solution

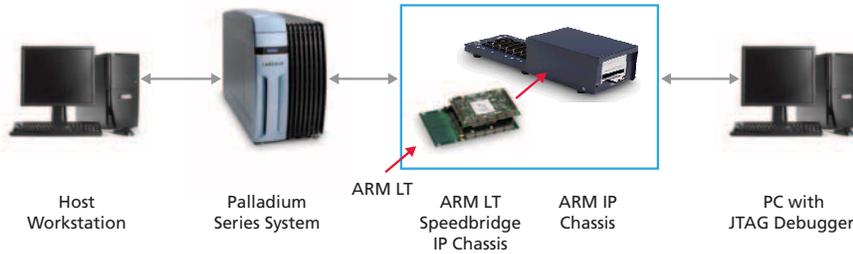


Figure 1: The SpeedBridge Adapter for ARM Logic Tiles helps you connect the Palladium XP Verification Computing Platform to an ARM Logic Tile and software debugger

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

Advanced debugging

- Supports interactive JTAG-based debugging tools familiar to software engineers
- Leverages advanced Palladium debugging capabilities

Improved quality

- Delivers a solution that is tested and verified by Cadence-based designs as well as many other user designs

Reduced system risk

- Runs system software/drivers/firmware
- Validates software stack
- Verifies embedded system software prior to hardware prototype
- Enables collaboration among HW/SW engineers for efficient debugging with respective views

Specifications

Supported ARM logic tiles

- ARM7TDMI
- ARM9EJS
- ARM1136JFS
- ARM1156T2S
- ARM1176JZFS
- ARM CORTEX A8
- ARM CORTEX R4F

For Newer versions or to make a request please contact the Cadence Product Marketing Team.

Other required components

- Palladium series acceleration/emulation system and 4 High Density Data Cables (HDDC)
- Software debugger* with JTAG interface
- Connectors and cables

* Several industry-standard software debuggers are supported, such as ARM Multi-ICE and Lauterbach. Please check with the Cadence Product Marketing team for more details.



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