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Protium FPGA-Based Prototyping Platform
FPGA-based prototyping solution

The Cadence® Protium™ FPGA-Based Prototyping Platform is an advanced FPGA-based prototyping solution enabling early software development, throughput regressions, and high-performance system validation. It combines high-capacity FPGA boards, based on the latest generation of FPGAs, with a complete implementation and debug software flow, providing an unprecedented quick design bring-up and ease of use. Compatible with Cadence's Palladium® Verification Computing Platform and SpeedBridge® adapters, it allows for the quick and smooth transition of the system-on-chip (SoC) design from an existing emulation environment into the high-performance fpga-based prototype.

Early Software Development

Successfully completing today's and tomorrow's challenging SoC designs, with their ever-increasing software contents, on time and on budget, requires starting the software-development process as early as possible. FPGA-based prototyping has long been a key technology to achieve that goal. However, growing complexities and shrinking time-to-market windows are making the bring-up of such a prototyping system increasingly painful and time consuming.

The Protium platform addresses and solves these challenges by providing a comprehensive and productive solution to reduce the prototype bring-up from months to weeks. This speed-up is achieved by combining a hardware platform—a family of FPGA boards—with a software platform, providing a fully integrated implementation flow as well as comprehensive debug capabilities.

System Validation

With their higher speed, smaller form factor, and external system connections, FPGA-based prototyping systems are a productive solution to
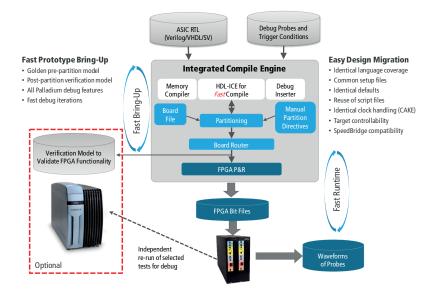

Figure 1: Protium flow

allow design teams to validate their hardware/software developments within the actual system environment. With its fast design bring-up and compatibility with the SpeedBridge portfolio, the Protium platform offers distinct advantages over in-house-developed and competitive FPGA-based solutions.

Throughput Regressions

As part of their efforts to achieve a "shift left" for software development, hardware verification, and hardware/software integration, users are adopting a continuum of development engines from virtual prototyping through RTL simulation, acceleration, and emulation to FPGA-based prototyping. The different engines are used both individually and in hybrid

combinations. Their compatibility with Palladium emulation, including the bring-up flow, combines with the ability to re-use the Palladium verification environment. The Protium platform is an ideal vehicle for the project phases in which the majority of hardware defects in the design already have been removed and users need to optimize the throughput of regressions at optimized speed and cost points, requiring less inter-active hardware debug.

Benefits

Fastest prototype bring-up

- Reuse of the existing Palladium emulation environment
- Automatic multi-FPGA partitioning
- Automatic memory conversion and modeling
- Support for unlimited number of design clocks

Highest model accuracy

- Support for complex, ASIC-style clocking
- Palladium-compatible clocking definitions
- Automatic generation of a post-partitioning Palladium database for fast model validation

Unparalleled debug

- Waveform capture and storage for off-line debug and analysis
- Signal force and release for interactive debug and design configuration
- Memory upload/download to quickly update design boot image and memory content
- Full clock control including start/stop and run "n" cycles, enabling advanced verification use modes and automation
- Palladium compatibility for interactive debug and root cause analysis

Unsurpassed flexibility

- Most common interfaces standard on board
- Expansion connectors for custom and off-the-shelf daughtercards

- Compatible with Cadence's emulation SpeedBridge adapters

Features

Complete, FPGA-based rapid prototyping system with all required hardware and software components.

Design input

- Synthesizable RTL (Verilog, VHDL, SystemVerilog).
- Synthesizable gate-level netlist
- Full support and compatibility with the Palladium language set (synthesizable constructs only)

Scripting and setup

- Compatibility with Palladium script files
- Compatibility with Palladium clock definition files
- Automatic ASIC-to-FPGA memory conversion

Multi-FPGA partitioning

- Fully automatic with FPGA interconnect optimization and FPGA utilization balancing
- Optional user guidance
- Optional black-box support for high-speed design modules and interfaces
- Automatic clock tree transformation (gated clocks, multiplexed clocks, latches, etc.)
- Automatic pin-multiplexing insertion

Post-partitioning Palladium model

- Generated automatically
- For fast FPGA model validation
- Accurate representation of the multi-FPGA implementation including clock remapping, memory conversion, pin-multiplexing, probing and triggering logic, etc.

FPGA place and route

- Fully automatic setup
- Support for parallel place and route
- Automatic timing closure, eliminating any setup and hold-time violations

Integrated Compile Engine

Taking an ASIC design (RTL) and mapping it into a set of FPGAs is without any doubt the biggest challenge and the most time-consuming task when getting a FPGA-based prototype up and running. Unlike other solutions, the Integrated Compile Engine in the Protium platform provides everything needed to take an existing RTL design, compile it, partition it into multiple FPGAs, and generate the individual bit files to configure each FPGA. This can be done fully automatically with minimal or no modifications to the original ASIC-RTL code. Various levels of specific user guidance and interaction allow further optimization, specifically to achieve higher speed.

To provide visibility into the design and interactive debug capabilities during runtime, the user can select the to-be-observed signals before compilation and define the trigger conditions to start a data capture. During runtime the selected signals are captured and stored for off-line viewing and analysis.

In addition, several unique debug capabilities are at the user's disposal, ranging from back-door memory upload/download over the ability to force signals into "1" or "0" to being able to start/stop the clock or run "n" cycles.

Protium Hardware

To cover a wide range of design sizes and also different interface requirements, multiple hardware configurations are available, ranging from two FPGAs per system to eight FPGAs per system. All FPGAs are Xilinx Virtex-7 2000T devices providing up to 12M ASIC gates capacity (design dependent) and up to 68Mb of embedded memory per FPGA. The boards are mounted in a custom chassis with power supply, cooling, and all necessary interfaces and cabling included.

In addition to being equipped with a variety of on-board interfaces, the Protium systems are also fully compatible with Cadence's family of SpeedBridge adapters, enabling a smooth transition from an emulation environment to a fpga-based prototyping environment.

Requirements

For compile

- Linux operating system (Refer to Platform Matrix for Cadence applications)
- 64GB of RAM
- 500GB of disk space

For control and configuration

- Linux workstation (32-bit or 64-bit; Red Hat or SUSE)
- 64GB of RAM
- 45GB of disk space
- 1 Ethernet port
- 1 USB 2/3 port
- Multiple Protium systems can be controlled from one workstation

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/support-and-training

Protium FPGA-Based Prototyping Platform—Hardware Configurations				
	39RX712	39RX714	39RX726	39RX728
FPGAs	2 Virtex-7 XC7V2000T	4 Virtex-7 XC7V2000T	6 Virtex-7 XC7V2000T	8 Virtex-7 XC7V2000T
FPGA boards	1	1	2	2
Approx. total capacity (design dependent)	Up to 25M ASIC gates	Up to 50M ASIC gates	Up to 75M ASIC gates	Up to 100M ASIC gates
FPGA-internal memory	136Mb	272Mb	408Mb	544Mb
On-board memory (optional)	Up to 32GB	Up to 64GB	Up to 96GB	Up to 128GB
Front panel interfaces	2x 4-lane PCI Express® (PCIe®) Gen2 3X SFP+ 1X QSFP+ 1X USB 3.0	1x 4-lane PCIe Gen2 4X SFP+ 2X QSFP+	3x 4-lane PCIe Gen2 7X SFP+ 3X QSFP+ 1X USB 3.0	2x 4-lane PCIe Gen2 8X SFP+ 4X QSFP+
On-board interfaces	PCIe (Gen1/2), SATA, USB 3.0, Ethernet, XAUI, Infiniband			
Clock generators	5 programmable synthesizers (2kHz – 945MHz)	5 programmable synthesizers (2kHz – 945MHz)	10 programmable synthesizers (2kHz – 945MHz)	10 programmable synthesizers (2kHz – 945MHz)
Mictor connectors	2	N/A	2	N/A
Expansion connectors	4	8	8	8
User I/Os	288 LVDS pairs or 584 single-ended	576 LVDS pairs or 1,168 single-ended	576 LVDS pairs or 1,168 single-ended	576 LVDS pairs or 1,168 single-ended
Board configuration	Ethernet, USB, PCIe			
Dimensions	480mm x 230mm x 673mm (width x height x depth); rack mountable, 5U height			

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