Protium S1 Single-FPGA Board

The most efficient way to validate your IP and subsystem

Part of the Cadence® Protium™ S1 FPGA-Based Prototyping Platform, the Protium S1 Single-FPGA Board is an affordable and high-performance solution for IP validation and early software development. It is fully compatible with the multi-FPGA Protium S1 product family and its comprehensive set of accessories and daughtercards. Being part of Cadence's System Development Suite ensures tight integration with other Cadence verification solutions and tools.

Early Software Development

Successfully completing today's and tomorrow's challenging IP and system-on-chip (SoC) designs, with their ever-increasing software contents, on time and on budget, requires starting the software-development process as early as possible. FPGA-based prototyping has long been a key technology to achieve that goal. However, growing complexities and shrinking time-to-market windows are making the bring-up of such a prototyping system increasingly painful and time consuming.

The Protium S1 FPGA-Based Prototyping Platform provides an efficient and affordable solution for early software/firmware development for a wide range of applications, including, but not limited to:

- IP validation
- Mixed-signal designs: big digital (D) and small analog (A)
- Medical
- Automotive
- IoT

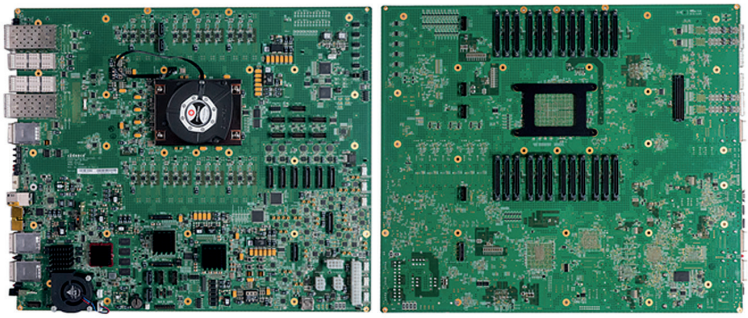

Figure 1: Protium S1 Single-FPGA Board (front and back views)

Figure 2: Enclosure option for Protium S1 Single-FPGA Board (enclosure front and back views)

With its high speed, small form factor, and extensive set of external interfaces, the Protium S1 Single-FPGA Board is a productive solution allowing design teams to validate their IP and SoC designs within the actual system environment.

Expandability

- Daughtercards
  - Cadence provided
  - Third party (e.g., FMC daughtercards through FMC adapter)
  - Custom
- Cadence SpeedBridge® adapters

Protium S1 Single-FPGA Board — Hardware Configuration	
39RX811K (Board Only)	
FPGAs	1X Virtex Ultrascale XU440
FPGA boards	1
Approx. total capacity (design dependent)	Up to 25M ASIC gates
FPGA-internal memory	88Mb
On-board memory (optional)	Up to 32GB
Front-panel interfaces	PCI Express® (PCIe®) Gen3 (X8) iPass, USB host, FPGA JTAG, CPU Ethernet, CPU serial, CPU device, JTAG 1X 4-lane PCIe Gen3 8X SFP+ 2X QSFP+
Back-panel Interfaces	1X 4-lane PCIe Gen3 8X SFP+ 2X QSFP+
On-board interfaces	2X SATA II (1X device/1XHost) 1X JTAG (14-pin) 1X RS232
GTH expansion connector	1X GTH connector 16 SerDes (16Gbps) Each GTH connector supports: 16-lane PCIe (Gen1/Gen2/Gen3) 2X CX4-channel Ethernet, XAUI, Infiniband 16X SFP+ 10GbE et al 4X QSFP+ 4 channels 10GbE or single-channel 40GbE 16X USB3.0/2.0 A, AB, B 16X Serial ATA II (SATA II) 16X SMA
Clock generators	5 programmable synthesizers (2KHz – 945MHz)
Samtec SEAM series connector	24 connectors: Each connector connects to 52 I/Os that can be configured as 24 LVDS + 4 single-ended signals or 52 single-ended signals
User I/Os	576 LVDS pairs or 1,248 single-ended
Board configuration	Ethernet, USB
Power requirements	500W, ATX 24-pin connector P1, 12V/36A, 5V/2A, 3.3V/15A
Dimensions	381mm x 32mm x 446mm (width x height x depth)

Optional Cadence Prototyping Compile and Debug Software Suite

The Protium S1 FPGA-Based Prototyping Platform is fully compatible with standard FPGA design and synthesis tools like Xilinx's Vivado, ensuring re-use of any exiting custom flow.

As part of the Cadence System Development Suite, the Protium S1 FPGA-Based Prototyping Platform is also fully supported by Cadence's unique and highly productive prototyping implementation and debug software suite. Using this software suite to compile and map a design into the Protium S1 Single-FPGA Board unlocks these additional capabilities and benefits:

Fastest prototype bring-up

- Congruency with and reuse of an existing Cadence Palladium® emulation environment
- Automatic memory conversion and modeling
- Support for an unlimited number of design clocks and clocking styles

Highest model accuracy

- Support for complex, ASIC-style clocking
- Reuse of emulation/simulation clocking definitions
- Automatic generation of a post-partitioning netlist for fast, pre-place-and-route model validation

Advanced debug

- Waveform capture and storage for off-line debug and analysis
- Signal force and release for interactive debug and design configuration
- Memory upload/download to quickly update design boot image and memory content
- Full clock control including start/stop and run "n" cycles, enabling advanced verification use modes and automation

Requirements

For compile

- Linux operating system (Refer to Platform Matrix for Cadence Applications)
- 64GB of RAM
- 500GB of disk space

For control and configuration

- Linux workstation (32-bit or 64-bit, Red Hat or SUSE)
- 64GB of RAM
- 45GB of disk space
- 1 Ethernet port
- 1 USB 2/3 port
- Multiple Protium S1 platforms can be controlled from one workstation

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training

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