cadence®

Encounter Conformal ECO Designer

ECO automation for greater predictability and design convergence

Cadence® Encounter® Conformal® ECO Designer enables designers to implement RTL engineering change orders (ECOs) for pre- and post-mask layout, and offers early ECO prototyping capabilities for driving critical Yes/No project decisions. Cadence ECO solutions combine automatic ECO analysis, logic optimization, and design netlist modification with world-class equivalence checking to provide superior performance, productivity, and predictability, helping you achieve convergence on your design goals.

Engineering Change Orders

Engineering change orders (ECOs) have a wide variety of implementations that range from adding or removing logic in a design to more subtle changes such as cleaning up routing for signal integrity. All ECOs are focused on delivering products to market as fast as possible with minimal risk to correctness and schedule. ECOs can be a time of high stress, long work hours, and uncertainty. Even if the logic change is implemented in the netlist, there might not be enough spare gates on the mask to implement the change.

Available flows for processing ECOs may remove some of the uncertainty of whether the product will work, but they are still a manual process that typically requires many cycles to achieve correct implementation. If the ECO were implemented with only metal-layer changes, the cost would be greatly reduced. Having this early knowledge of implementability, a design team can change plans and target workable solutions rather than wasting time in failed attempts and extended schedules.

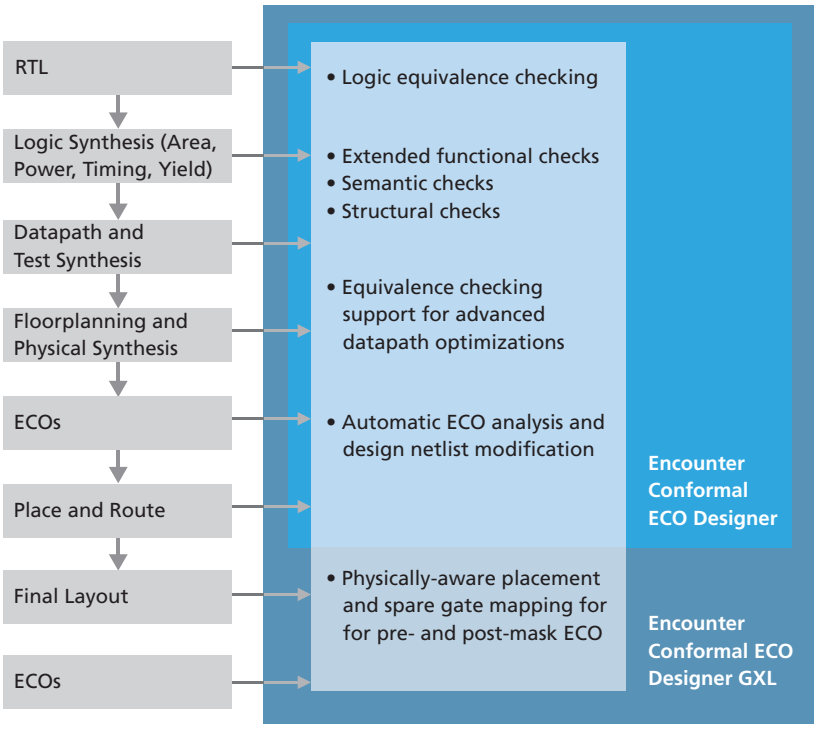

Figure 1: Encounter Conformal ECO Designer offers automatic ECO analysis and design netlist modification

Encounter Conformal ECO Designer

Cadence offers the most complete ECO solution that spans from RTL to GDS. This solution consists of Encounter Conformal ECO Designer for ECO automation for RTL-level functional changes, Encounter RTL Compiler for logic synthesis and ECO logic optimization, and Encounter Design Implementation System for physical implementation of the ECO changes. This combined solution brings automation and predictability to the ECO process.

Conformal ECO Designer is a unique technology that offers functional ECO analysis, optimization, and generation capability. It combines proven equivalence checking and functional checks, and uses formal techniques to analyze, abstract, and implement the functional ECO.

Conformal ECO Designer is available in two configurations: an XL offering, which targets primarily the pre-mask ECO flow; and a GXL offering, which targets the pre-mask and post-mask ECO flow with metal-only layers and spare gates. The GXL configuration leverages physical database knowledge to generate ECO placement guidance for downstream place-and-route tools.

Benefits

- Provides faster turnaround time by minimizing manual intervention and eliminating time-consuming iterations
- Generates early estimates on ECO feasibility by quantifying designer intent
- Implements complex ECOs that are typically not attempted manually
- Enables front-end designers in fabless semiconductor companies earlier netlist handoff to ASIC vendors
- Improves designer productivity and offers flexibility to do ECO with metal-only layers, thus reducing manufacturing costs and driving faster design convergence toward tapeout
- Reduces verification time significantly by using abstraction techniques to verify multi-million–gate designs much faster than traditional gate-level simulation

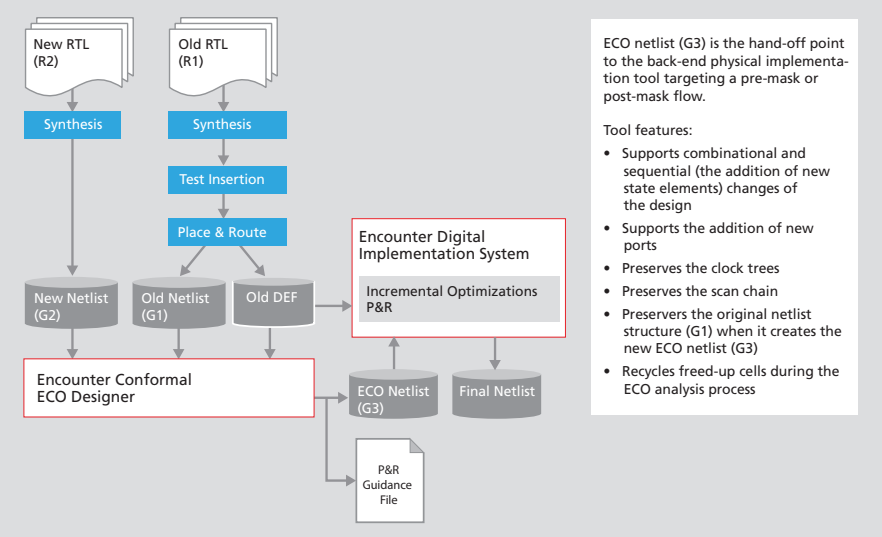

Figure 2: The Encounter Conformal ECO Designer implementation flow

- Decreases the risk of missing critical bugs through independent verification technology

Features

Conformal ECO Designer combines logic equivalence checking (for the most complex SoC and datapath-intensive designs) with functional ECO analysis, design netlist modification, and logic optimization.

Equivalence checking for ECOs

During development, a design undergoes numerous iterations prior to final layout, and each step in this process has the potential to introduce logical bugs. Conformal ECO Designer checks the functional equivalence of different versions of a design at these various stages and enables designers to identify and correct errors as soon as they are introduced, ensuring initial intent remains intact.

Equivalence checking also plays an important role in the ECO implementation process. It helps the ECO analysis tool identify which modules and logic cones in the design require change to implement the ECO. For instance, in Figure 2, the original netlist is compared against the new netlist to determine what has changed. Equivalence checking is also used at the tail end of the process to make sure the ECO implementation was successful both for front-end and back-end signoff.

Functional ECO analysis

Conformal ECO Designer has a built-in ECO analysis engine that can identify the differences between the original design netlist and the new design netlist. Users can perform ECO analysis on the entire design or on specific modules within the design hierarchy, which is typically more efficient. Once the ECO analysis step is completed and the logic change optimized, Conformal ECO Designer performs the necessary netlist modifications to achieve the new function in the original design netlist. The output is the ECO netlist. Alternately, Conformal ECO Designer can write out an ECO script that can be used to make direct changes to the place-and-route database.

Physically-aware pre-mask ECOs

Conformal ECO Designer (GXL) has the ability to read the DEF layout database corresponding to the original place-and-route design netlist, LEF, Liberty synthesis libraries, and SDC timing constraints to optimize changes, estimate routing, and legally place the generated ECO logic into the design floorplan. The output of Conformal ECO Designer is the ECO netlist and the corresponding placement DEF file. This flow can reduce timing closure itera-

tions during place-and-route, especially in late-state pre-mask ECO situations, to drive design convergence.

Spare gate mapping for post-mask ECOs

Conformal ECO Designer (GXL) can also read the DEF layout database corresponding to the original design netlist, LEF, Liberty synthesis libraries, and SDC to optimally map ECO logic to standard cell and gate-array spare gates. The mapping engine is timing and spare cell location-aware. This capability enables the designer to get an early estimate of the ECO feasibility and drive convergence in the back-end implementation flow.

Conformal ECO Designer (GXL) can also recycle freed-up cells in the ECO mapping process. The output is the ECO netlist and a spare gate mapping file, which instructs the place-and-route tool how to map the newly added ECO logic to specific spare logic resources in the layout.

Integrated environment

An intuitive GUI is provided for setup and debugging, allowing the user to work more productively and quickly pinpoint the cause of equivalence mismatches. Included are:

- Graphical debugging via an integrated schematic viewer that shows logic values for each error vector
- Full cross-highlighting between RTL model and circuit
- Automatic error candidate identification with assigned and weighted percentages
- Logic-cone pruning to focus debugging on relevant information

Smart setup and diagnosis

Conformal ECO Designer includes a set of intelligent analysis commands to ease setup and diagnosis. Smart setup investigates the current environment and automatically remedies common setup issues sometimes experienced by new users. In tandem, non-equivalent analysis can be invoked if non-equivalences are encountered and can present concise root cause information for quicker debug. For hierarchical designs, Conformal ECO Designer includes smart technology for accelerating setup requirements through boundary conditions profiling

Encounter Conformal Technology

To shorten overall design-cycle times and minimize silicon re-spins, designers need production-proven validation. Encounter Conformal verification technologies offer the most comprehensive and trusted solutions for equivalence checking, timing constraints management, asynchronous clock-domain-crossing synchronization checks, functional ECO analysis and generation, and low-power design verification.

The Encounter Conformal technology family consists of Conformal Constraint Designer, Conformal Equivalence Checker, Conformal Low Power, and Conformal ECO Designer.

Platforms

- Linux (32-bit, 64-bit)
- Sun Solaris (64-bit)
- IBM AIX (64-bit)

Language Support

- Verilog (1995, 2001, 2005)
- SystemVerilog
- VHDL (87, 93)
- SPICE (traditional, LVS)
- EDIF
- Liberty
- Mixed languages

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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