cādence®

Cadence SpeedBridge Adapter for PCI Express
In-circuit emulation under real-world operating conditions

The Cadence® SpeedBridge® Adapter for PCI Express is an in-circuit emulation solution designed specifically for system-level testing and integration of PCI Express-based device ASICs. It verifies emulated designs with the actual ASIC software/hardware and does not require modification, increasing productivity and reducing system risk. As a result, designers are assured of PCI Express device quality and get their products to market faster.

Cadence SpeedBridge Adapter for PCI Express

PCI Express is a high-bandwidth, low pin-count, serial interconnect technology that also maintains software compatibility with existing PCI infrastructure, and is uniquely positioned as the logical interconnect technology for products being developed today. As the computing platform of the future, PCI Express architecture provides industry-leading price and performance. To address the verification and integration needs for PCI Express devices, Cadence offers an off-the shelf in-circuit emulation solution for PCI Express design.

The Cadence SpeedBridge Adapter for PCI Express consists of an adapter card and encrypted emulator-resident RTL wrappers that together convert a standard PCI Express interface into an emulation-speed PCI Express interface (See Figure 1.1 & 1.2). It interfaces with most existing PCI Express-capable hosts without requiring modification.
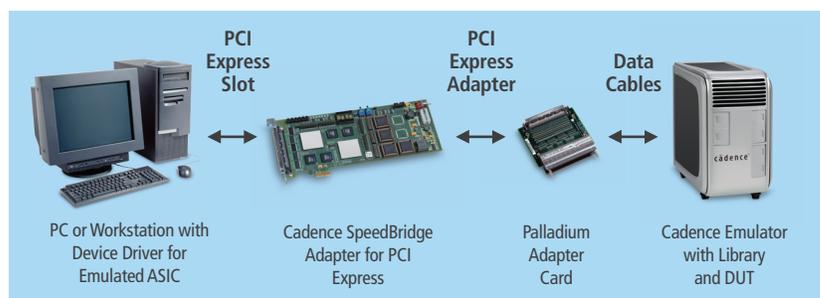

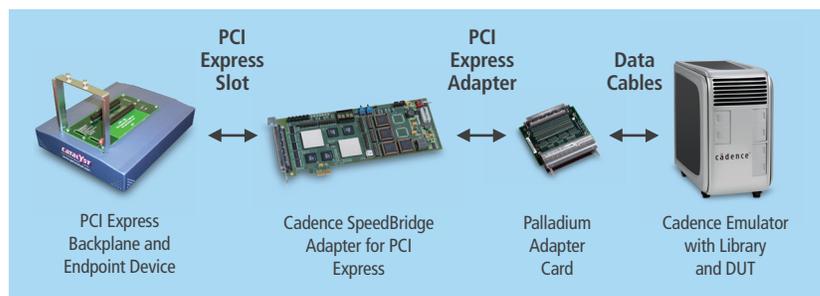*Figure 1.1: Cadence Speed Bridge Adapter for PCI Express—System Components for Endpoint Emulation*

Figure 1.2: Cadence Speed Bridge Adapter for PCI Express—System Components for Root Complex Emulation

It performs rate adaptation so that 1) emulated endpoint designs can connect to a host platform (PC, server, backplane) without slowing down the host or system device to emulation speed, and 2) emulated root complex designs can connect to full-speed endpoint cards.

The SpeedBridge Adapter for PCI Express connects directly to a Cadence Incisive® Palladium® emulator through standard emulation cables. It is designed to be functionally transparent to both the PCI Express host and the emulated devices. With the high speed of in-circuit emulation, you can co-verify hardware and software together with software drivers without the real silicon. Cadence emulators provide the advanced hardware/software debug capabilities you need for ease of use, ease of debug, and high speed—so you don't have to sacrifice quality.

Benefits

- Enables rapid emulation deployment

- Enables verification IP reuse
  - Works from one project to another
  - No need for every user to re-invent the solution
  - Improves productivity to get to the first test by eliminating environment setup and debug time

- Ensures quality
  - Tested and verified by Cadence and many other user designs
  - Verifies your design quickly and efficiently
  - Provides a single-card solution

- Reduces system risk
  - Checks PCI Express protocol and integrity errors (CRC)
  - Verifies the PCI Express design in a real environment
  - Boots OS system
  - Runs real system software/drivers
  - Increases confidence in PCI Express device quality
  - Reduces time to market

Features

- Enables emulation of root complex, endpoint, switch and bridge devices

- Compatible with non-SSC (spread spectrum clock) PCI Express host platforms

- Multiple lanes
  - Supports 1x, 4x, 8x, 16x lanes

- Emulation speeds
  - Connects an emulated PCI Express device to a full-speed PCI Express device and works with emulation speed up to 1.5MHz

- Fully transparent to software driver or system software

- Real PCI Express driver environment
  - Installs in the PCI Express host platform

- Early debug with first silicon and first software
  - Allows concurrent software development and HW/SW co-verification

- Debug capabilities
  - Fully static implementation supports key emulation debug features
  - Supports Logic Analyzer debug capabilities

- For detailed information, email incisive_info@cadence.com

Specifications

- Compliant with PCI Express base specification v1.0a

- Memory, IO, configuration, and message transaction support

- Requests and completions support

- Credit base flow control

- Full PHY-level link initialization

- PCI Express PHY-level 10b interface as well as standard PIPE in either 8-bit or 16-bit mode support

- One virtual channel (VC) and one traffic class (TC) support

- Payload of 128-byte to 4096-byte support

- Legacy and non-Legacy device support

- Lane reversal and polarity inversion support

- Extended configuration space support

- Transaction ordering driven by host platform support

- Multiple read completion support

Requirements

- A PC or workstation with one or more PCI Express slots: one slot for each adapter used for emulation of a PCI Express endpoint

- A PCI Express backplane for emulation of a PCI Express root complex

- One adapter for each emulated PCI Express interface to be connected to the host system

- Motherboard must be able to turn off spread spectrum clock (SSC)

- Incisive Palladium system

- PCI Express cable adapter board

- One 200-pin PCI Express adapter cable

- One motherboard reset cable

- Emulator-resident RTL wrappers

- Device driver and/or application software required by the emulated ASIC

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training

- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom

- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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