cadence®

RocketSim Parallel Simulation Engine

Delivering revolutionary parallel logic simulation speed-up

Cadence® RocketSim™ parallel simulation engine eliminates functional verification bottlenecks by complementing compiled-code simulators with revolutionary parallel simulation technology that speeds up simulation using standard multi-core servers. It is proven for register-transfer level (RTL) system on chip (SoC), gate-level functional simulation, and gate-level design for test (DFT) simulation in numerous marquee systems and semiconductor companies in the mobile, server, and graphics domains.

Overview

Functional verification is a severe bottleneck in chip design projects. The ever-growing chip density and complexity impacts the time it takes simulators to complete each run. When each simulation takes days to complete, either the project's time to market is delayed or, in some cases, teams tape out early with less confidence.

RocketSim parallel simulation engine solves the bottleneck common in existing compiled-code simulators by offloading the time-consuming calculations to an ultrafast multicore engine. This enables the engine to achieve performance gains over compiled-code simulators of up to 6X for RTL SoC, up to 10X for gate-level functional simulation, and up to 30X for gate-level DFT simulation. Complex simulations like these often need SystemVerilog Assertions (SVA) and X-propagation support, which is provided by the engine. It also complements hardware-based accelerators by executing full four-state, bit-precise logic (0, 1, X, Z), and works from within the familiar simulator environment.

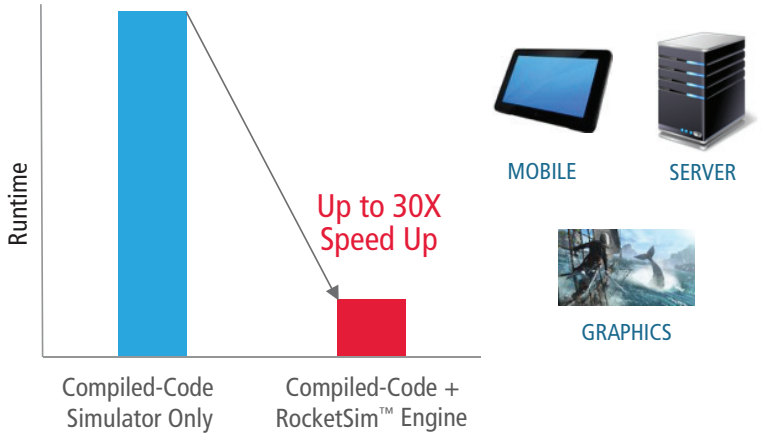

Figure 1: The RocketSim engine delivers ultrafast multicore simulation

During compilation, the RocketSim engine's compiler runs on the host machine, separating the design from the testbench. During runtime, a large portion of the logic is offloaded to the RocketSim parallel simulation engine, running on standard multicore servers, while the testbench runs on the host simulator. Programming language interface (PLI) is used during simulation execution to maintain the state synchronization between the compiled-code simulator running the testbench and the RocketSim engine running the design.

With the RocketSim parallel simulation engine, you get support for large and complex designs (over one billion gates), along with full visibility of your design, including debug access. This expands the role of simulation to include larger designs and more complex tests.

The RocketSim engine works seamlessly with Cadence® Incisive® Enterprise Simulator, accelerating the simulation process without the need to modify designs or testbenches.

Key Features

RocketSim parallel simulation engine:

- Runs on standard multi-core servers
- Scales to available cores for performance
- Speeds up leading compiled-code simulators
- Provides over one billion logic gate capacity
- Complies with IEEE 1364 Verilog, 1800 SystemVerilog (including SVA), 1076 VHDL
- Executes full support for four-state logic (0, 1, X, Z)
- Executes X-propagation support
- Runs alongside the testbench
- Supports UVM, OVM, eRM, and VMM testbenches
- Supports PLI/VPI compliant interface
- Provides full debug visibility
- Enables direct dump of FSDB/SST2 waveforms
- Enables quick ramp-up

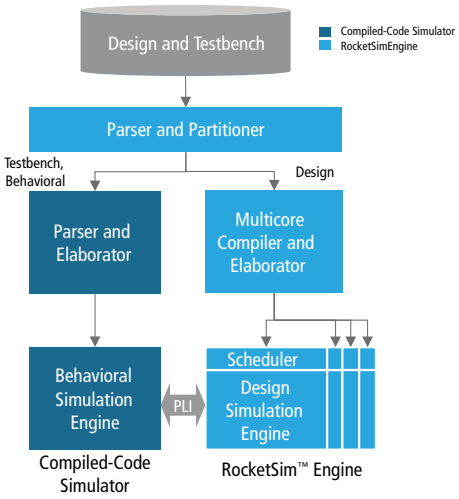

Figure 2: Integration of RocketSim engine and compiled code simulation

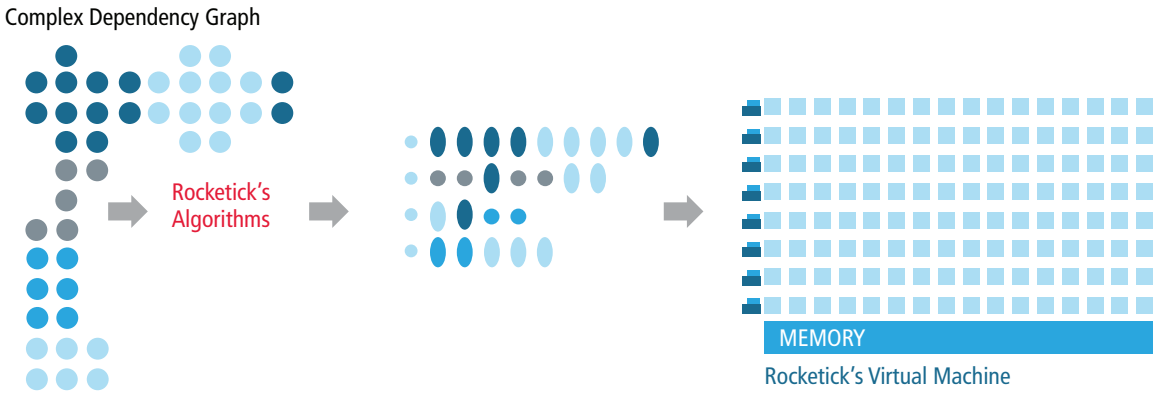

Figure 3: Revolutionary parallel simulation algorithms