Emulation Development Kit for Palladium Series

Full system verification solution

The Cadence® Emulation Development Kit (EDK) is a pre-configured off-the-shelf solution that allows users to validate their systems and co-verify hardware and software in a pre-silicon environment. This solution provides modeling accuracy, high performance, and remote access, simplifying the engineering task and dramatically improving verification productivity.

Overview

The Cadence Emulation Development Kit (EDK) is a pre-configured off-the-shelf, rack-mountable solution for system-level validation that provides modeling accuracy, high performance, and remote access using the Cadence Palladium® series. It enables rapid deployment of a high-performance system-level validation platform, and makes it possible to co-verify hardware and software with applications running on an industry-standard operating system (OS) using the standard software stack, dramatically improving verification productivity.

The Cadence EDK is pre-configured for protocol-specific interfaces so that device software engineers can easily develop and validate application software and device drivers for standard operating systems over device hardware interfaces such as PCI Express® and USB.

Figure 1: Emulation Development Kit with Palladium Series

Pre-Configured Solution for Full-System Validation

The rise in hardware and software complexity is making system validation increasingly difficult. To ensure completeness of verification, it is essential to run production-level system software in a pre-silicon environment to account for all corner cases that are very difficult to model in a testbench-driven environment.

Cadence EDK is a pre-configured solution enabling users to quickly bring up a real-time system environment that can aid in developing and testing drivers, operating systems, test suites, etc. on a pre-silicon design under test (DUT). It facilitates a flexible but high-

fidelity pre-silicon verification platform allowing for easier integration of system hardware and software.

Unlike virtual channels that have to share a single connection channel for each additional port, the Cadence EDK offers full-speed performance for any number of ports in the design under test. This ensures full scalability and bandwidth for fast system verification.

Remote Accessibility

Cadence EDK offers a fully secure, cloud computing setup with remote accessibility, ensuring that teams distributed across different geographical locations can easily access and complete their system verification tasks through a Palladium series verification platform that is hosted at a data center location. This can be achieved without compromising the accuracy of traffic through the DUT or runtime performance.

Benefits

Highest productivity with high fidelity

- Offers higher verification performance than other verification methods without abstracting out critical portions of the design, while running in a real system environment that will be used in post-silicon validation
- Full-speed performance and scalable with multi-interface designs or multiple interconnect technologies

Offers rapid verification deployment

- Provides a pre-validated emulation interface fully compatible with the Palladium series
- Enables rapid creation of system-level environments using the same hardware and software that the real silicon will use

Enables reuse

- Built around standards-compliant interfaces such as PCIe® and USB, and can be reused for other projects
- Improves productivity by getting the design running quickly without weeks or months of specialized test environment creation
- Allows use of standard third-party protocol analysis tools, driver development suites, and traffic-generation utilities

Ensures quality

- Tested and verified by Cadence against independent verification IP and other user designs
- Cadence-provided solution lets you verify your design quickly and efficiently to ensure high product quality

Reduces system emulation bringup risk

- Performs interface testing at the physical level
- Runs full system enumeration connected to a real server chipset running a real OS with a full software stack
  - Does not abstract away low system-level connection issues that arise with real chipsets
  - Does not abstract away the real enumeration sequence of different OSs
- Runs entire system-level real tests, just as the design silicon will have to do when it is deployed
  - Directed random testing is a vital and necessary part of modern system verification, but it is not sufficient
- Allows interaction with multiple system-level interconnects such as PCIe and USB, all in the same verification environment and without impacting performance

Features

- Remotely configure, use, and monitor using IP network
- Supports remote protocol and traffic monitors
- Supports Windows 7, Windows 10, and Linux OSs
- Supports PCI Express Gen3 protocol interface with up to 16 lanes and L1 power management
- Supports USB3.0 device interface with U0, U1, U2, and U3 power management

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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