Improving the Breakdown Voltage for 100nm GaAs pHEMTs by the Support of Device Simulations

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Abstract

In this work we discuss for a 100nm gate length GaAs pHEMT transistor with a transconductance of gmax=760mS/mm and an input capacitance of cin=740fF/mm the influence of the distance between the channel and super lattice on the drain leakage current Id and the breakdown voltage Vbds and the relation between both parameters. The understanding of this relation was possible by the help of device simulations. An improvement of 20% in the breakdown voltage Vbds was possible by optimizing the distance between channel and super lattice while the other process parameters were kept the same.

INTRODUCTION

The demand for devices operating above 100GHz results in a reduction of the gate length below the subquarter-micrometer range. To get a better understanding of the short channel effects and the interpretation of the measured electrical parameters like leakage currents and breakdown voltage the technological development of a single recess 100nm pHFET was accompanied by device simulations. The parameter set used for these device simulations is based on parameters used for the simulation of our standard PH25 pHEMT process.

DEVICE SIMULATIONS AND MEASUREMENTS

For the measurement and simulation of the drain and gate leakage current a constant voltage is applied on the drain and the source is grounded. While sweeping the gate voltage the drain and gate leakage currents are recorded.

When reducing the gate length in the 100nm range both measurements and device simulations show an increased drain leakage current in the sub-threshold range. Fig. 1 shows the measured drain and gate leakage currents for transistors with a gate length of 100nm and different distances between the Schottky contact and the channel.

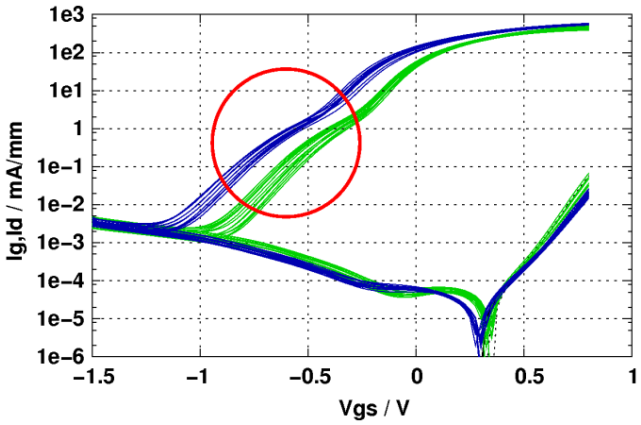

Figure1: Measurement: drain and gate leakage current for 100nm gate length transistors with two different distances between Schottky contact and channel

The different distances between Schottky contact and channel are the reason for the horizontal shift in the two sets of drain leakage curves. The gate leakage current is about the same. In the encircled area of Fig. 1 the drop of the drain leakage current is reduced with decreasing gate voltage. The same effect of a reduce drop in the drain leakage is observed in results obtained from device simulations, as can be seen in the encircled area of Fig. 2.

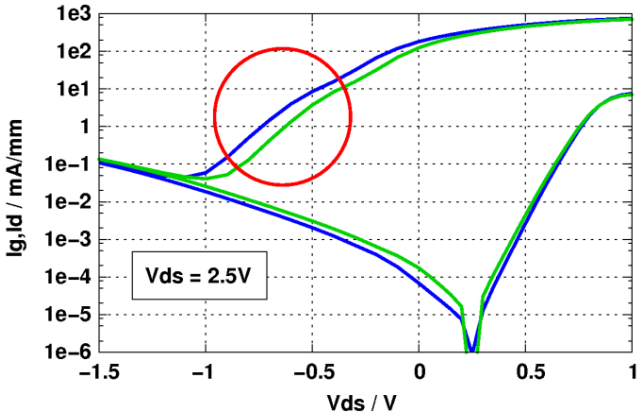

Figure 2: Device simulation: drain and gate leakage currents for 100nm gate length HEMTs with different distances between Schottky contact and channel

These simulations were also performed for two different distances between Schottky contact and channel. For transistors with gate lengths in the subquarter-micrometer range like for the PH25 process the drain leakage current does not show this reduced drop.

As both, measurement and device simulation, show the same effect device simulations were performed to get a better understanding of the root cause of the increased drain leakage current when going to smaller gate lengths. For these simulations the gate length Lg was varied in the range from 220nm down to 60nm. The other parameters like epitaxy stack, doping concentration and geometry were kept the same.

The result of the device simulations shows a significant increase in the drain leakage current when reducing the gate length, as can be seen in Fig. 3.

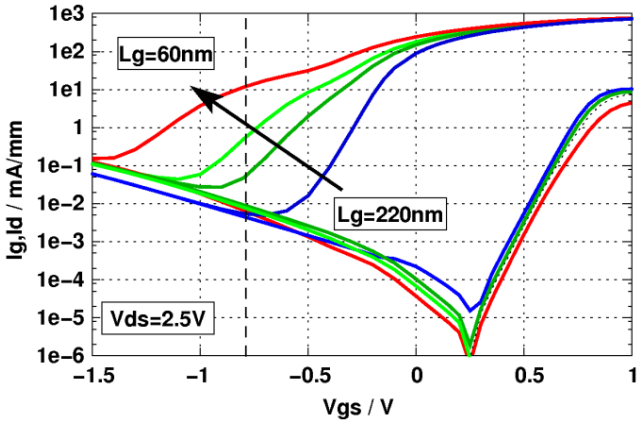

Figure 3: Device simulation: drain and gate leakage current for different gate lengths

Device simulations also show that an increased drain leakage current is directly reflected by a reduced transistor breakdown voltage. This relation will be explained later on.

Understanding the Drain Leakage Current

To identify the origin of this increased drain leakage current device simulations were used to visualize the current flow for Vds=2.5V and Vgs=-0.8V. In Fig. 3 the dashed line indicates this bias point. For this biasing the drain leakage current differs significantly between a transistor with a gate length of 220nm and 60nm. For a transistor with a gate length of 220nm the complete drain current flows into the gate. Gate and drain leakage currents are about the same as can be seen in Fig. 3. But looking at the current flow for a transistor with a gate length of 100nm the drain current bypasses the channel in the direction of the super lattice, see Fig 4.

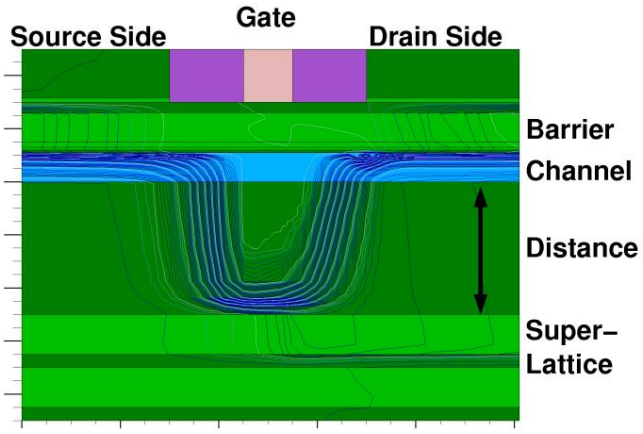

Figure 4: Device simulation: current flow lines for Lg=100nm, Vds=2.5V and Vg=-0.8V

The hetero barrier of the first super lattice behaves as a parasitic channel below the normal channel. With decreasing gate length more and more drain current bypasses the channel in the direction of the super lattice at pinch off. This is the reason for the increased drain leakage current for reduced gate lengths.

Optimizing the Epitaxial Stack

Identifying the origin of the increased drain leakage current and the related reduction in the breakdown voltage various device simulations focusing on the area between super lattice and channel were performed to hinder the drain current bypassing the channel. From device simulations resulted that one mean to reduce the leakage current and increase the transistor breakdown voltage Vbds is the reduction of the distance between the ternary AlGaAs/GaAs super lattice and the channel. The simulation showed that the other important electrical parameters like transconductance and input capacitance are not affected by this modification.

Fig. 5 shows results of device simulations when reducing the distance between channel and supper lattice for a transistor with a gate length of 100nm.

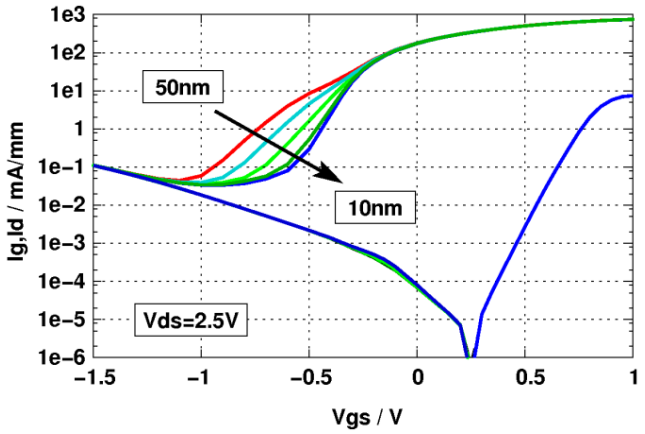

Figure 5: Device simulation: gate and drain leakage current with different distances between channel and super lattice

The drain leakage current can be drastically reduced by reducing the distance between channel and super lattice. While the gate leakage current is not influenced by this modification. The gate leakage current is mainly influenced by the properties of the Schottky contact between the gate metalization and the barrier and surface states along the recess.

This decreasing drain leakage current is directly reflected by an increasing breakdown voltage in the simulation as can be seen in Fig. 6.

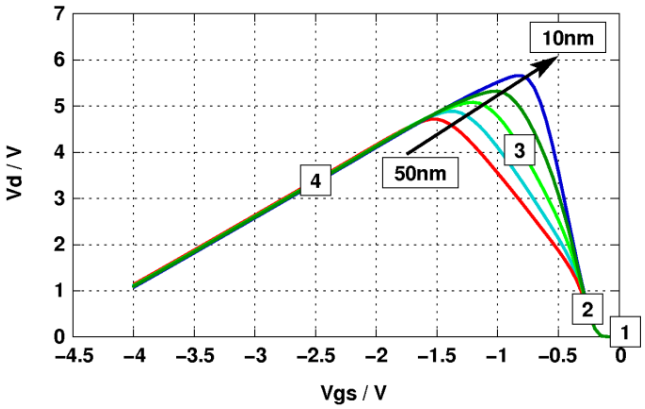

Figure 6: Device Simulation: influence of the distance between channel and super lattice and breakdown voltage

For these breakdown simulations Idss/100 is applied to the drain, the gate voltage is reduced starting at Vgs=0V and the drain voltage is recorded. The maximum of the drain voltage is the breakdown voltage Vbds [1].

In Fig. 6 four different areas are indicated by numbers. In the first area the channel is open and a low drain voltage is sufficient for the applied current. By reducing the gate voltage the transistor starts to pinch and an increased drain voltage is needed to maintain Idss/100. In the third area the drain voltage starts to differ between the different variations. The simulation with a distance of 50nm between channel and super lattice shows the lowest increase of the drain voltage Vd with decreasing gate voltage Vgs. For this simulation significant current bypasses the channel in the direction of the super lattice and a low drain voltage Vd is needed for maintaining the current. Reducing this distance the slope of the drain voltage increases more and more as a result of a more confined current in the channel and less current bypassing towards the super lattice. After reaching the maximum of the drain voltage all five curves coincide in the fourth area. This indicates the same diode breakdown behavior of the gate drain diode for all simulations. The diode is not influenced by the distance between channel and super lattice.

Realized Epitaxial Stacks

To verify the device simulation results wafers were grown by MBE with distances of 50nm (Buffer 1), 25nm (Buffer 2), and 10nm (Buffer 3) between the super lattice and the channel. The other layers and the doping concentration were kept the same. All wafers were processed in the same lot using the same process parameters.

As predicted by device simulations the drain leakage current is reduced by reducing the distance between channel and super lattice. Fig. 7 shows the measured improvement of the breakdown voltage Vbds for transistors with a gate length of 100nm.

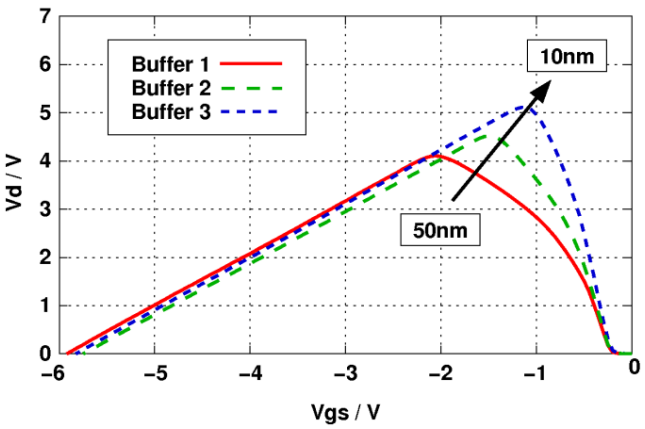

Figure 7: Measurement: breakdown voltage for three different distances between channel and super lattice and a gate length of 100nm

The measurements are in good agreement with the device simulations. The gate drain diode for the measured transistors behave about the same as can be seen in the coincidence of the three curves for gate voltages below -2V where the gate drain diode determines the shape of the curves with a slope of about one. Buffer 1 with a distance of 50nm between channel and super lattice shows the lowest breakdown voltage with Vbds=4V. By reducing the distance down to 25nm (Buffer 2) and 10nm (Buffer 3) the breakdown voltage increases up to 5V.

CONCLUSIONS

By the use of device simulations the first hetero barrier of the super lattice was identified as a parasitic channel for a 100nm gate length pHEMT. This channel influences the drain leakage current Id in the sub-threshold range and the breakdown voltage Vbds. By reducing the distance between channel and super lattice from 50nm down to 10nm the influence of the parasitic channel on the drain leakage current was drastically reduced and the breakdown voltage was improved from Vbds=4V to 5V with no other modifications in the process. The other electrical parameters were not influenced by this modification.

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REFERENCES

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ACRONYMS

pHEMT: Pseudomorphic High Electron Mobility Transistor
MBE: Molecular Beam Epitaxy
Vg: Gate voltage
Vds: Drain source voltage
Idss: Drain current at Vds=2.5V and Vgs=0V
Vbds: Transistor breakdown
Id: Drain current
Ig: Gate Current