Influence of the Epitaxy on the Sub-Threshold Drain Leakage Current and the Breakdown Voltage for GaAs pHEMTs

P. Abele, F. Bourgeois, J. Splettstoesser, and D. Behammer

United Monolithic Semiconductors GmbH, Wilhelm-Runge-Strasse 11, D-89081 Ulm, Germany

Phone: +49-731-505-3093, FAX: +49-731-505-3005, E-mail: abele@ums-ulm.de

Keywords: GaAs, pHEMT, sub-threshold, breakdown, buffer, epitaxy

Abstract

In this work we present the influence of the buffer on the drain leakage current and breakdown voltage of $Al_{0.25}Ga_{0.75}As/In_{0.20}Ga_{0.80}As/Al_{0.25}Ga_{0.75}As$ double recessed pHEMTs. Three different types of buffers were investigated: a 50 nm thick $In_{0.52}Ga_{0.48}P$ layer, a binary AlAs/GaAs super lattice, and a ternary $Al_{0.60}Ga_{0.40}As$/GaAs super lattice. For the latter the thickness of the first $Al_{0.60}Ga_{0.40}As$ layer was also varied. The measurements of the drain leakage current and breakdown voltage are presented and discussed.

Introduction

Double recessed pHEMT GaAs transistors are widely used for power applications. For these applications high breakdown voltages are mandatory. The properties of the surface determined by surface states and charges show significant influence on the breakdown voltage. All the wafers presented here are processed in the same way, so the surface properties of all wafers are comparable. In this work we concentrate on the buffer below the channel and show its influence on the drain leakage current and breakdown voltage.

After introducing the technology for the double recess pHEMT transistors and the measurement conditions for determining the drain and gate leakage currents and the breakdown voltage these electrical parameters of the transistors are presented and discussed for each buffer variation. To get a better understanding of the measurement results device simulations using Silvaco were performed.

Experimental

All transistors presented have seen the same process flow and have the same epitaxy stack except the buffer. The wafers were grown by MBE (Molecular Beam Epitaxy) with a Si δ-doping on both sides of the channel. A schematic cross section is shown in Fig. 1.

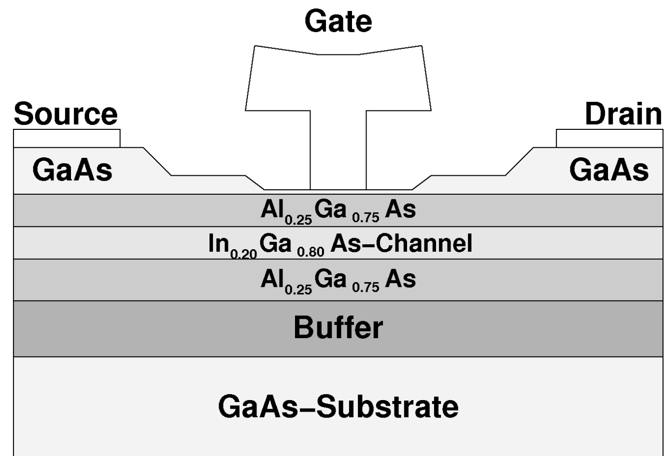

Figure 1: Schematic cross section of the double recessed pHEMT

First the source and drain contacts are defined by a lift off process. After double recess formation by wet chemical etching using an AlAs stop layer for a well defined recess geometry, a dielectric assisted Al-T-gate is defined by lift off and the transistor is finally passivated using a nitride. The gate length for these transistors is L_G=230 nm. Below the channel a 20 nm thick $Al_{0.25}Ga_{0.75}As$ layer separates the buffer.

For the measurements presented in this work single finger transistors are used with a gate width of 100 µm.

The gate and drain leakage currents were measured by applying at the drain V_{DS}=2.5 V and sweeping the gate voltage V_{GS} between –3 V and +0.5 V while the source is grounded. The gate and drain currents are recorded. The drain current at V_{GS}=0 V and V_{DS}=2.5 V is defined as I_{DSS}. For determining the breakdown voltage V_{BDS} a drain current of I_{DSS}/100 is applied and the gate voltage V_{GS} is reduced starting at 0 V. When the channel starts to pinch the drain voltage increases up to a maximum. The maximum is V_{BDS} [1].

BUFFER: ALAS/GAAS

For these wafers the buffer consists of a binary AlAs/GaAs super lattice. Fig. 2 shows the leakage currents of two transistors (Tr1 and Tr2) from two wafers grown at different times but processed in the same lot.

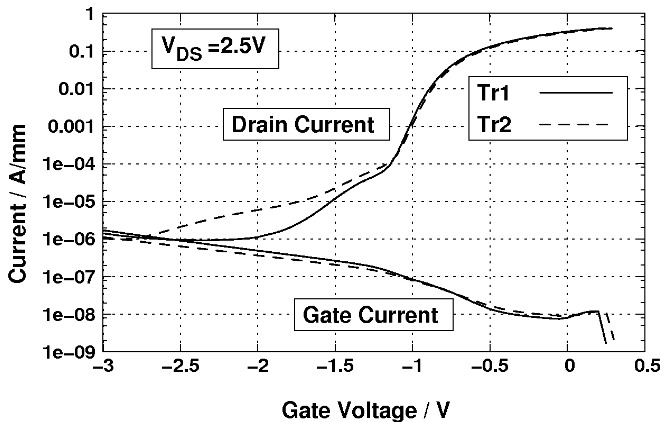

Figure 2: Drain and gate leakage current from transistors from different wafers using the same AlAs/GaAs buffer

While the gate currents for both transistors are similar over the whole measurement range from –3 V up to +0.5 V the drain currents deviate at gate voltages below -1.2 V significantly. Transistor Tr2 shows a much higher drain leakage current indicating a worse control of the current below the gate. At V_{GS}=-2 V transistor Tr1 shows nearly one decade more drain current. On the same transistors the breakdown voltage was measured, see Fig. 3.

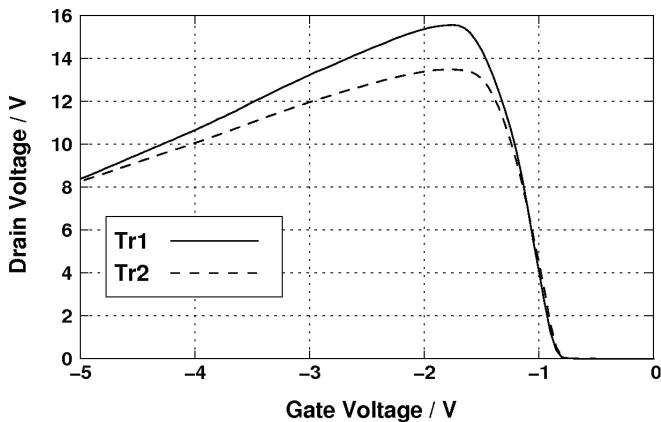

Figure 3: Breakdown voltage of transistors with different drain leakage currents

The high drain leakage current is directly reflected by a low breakdown voltage. Transistor Tr1 shows a breakdown voltage of V_{BDS}=15.5 V and transistor Tr2 V_{BDS}=13.5 V both at a gate voltage of V_{GS}=-1.75 V.

To verify this observation a correlation between the breakdown voltage and the drain leakage current at V_{DS}=2.5V and V_{GS}=-2V was performed on several lots with 20 transistors measured on each wafer. This confirmed the observation.

As both transistors use the same super lattice for the buffer and have a similar δ-doping as can be seen in Fig. 2, where the drain leakage current curves of both transistors show no vertical shift above V_{GS}=-1.2V to each other, device simulations were performed to get an understanding of the deviation in the leakage current. These simulations show an influence of the background doping of the super lattice on the drain leakage current. Simulations with an acceptor background concentration below 5E14/cm³ show a clear increase in the drain leakage current and a reduction in the breakdown voltage. Using a background doping of more than 2E15/cm³, the simulations showed a drastic reduction of the drain leakage current.

BUFFER: INGAP

For this experiment as buffer a 50 nm thick $Ga_{0.52}In_{0.48}P$ layer was used. Using this buffer the discontinuity in the conduction band to the $Al_{0.25}Ga_{0.75}As$ layer is very low [2]. Device simulations show at a gate voltage of V_{GS}=-1.8 V where the transistor should be pinched off a significant current flow below the buffer in the GaAs substrate. This causes an increase of the drain current. These device simulation results are verified by measurements on transistors as can be seen in Fig. 4.

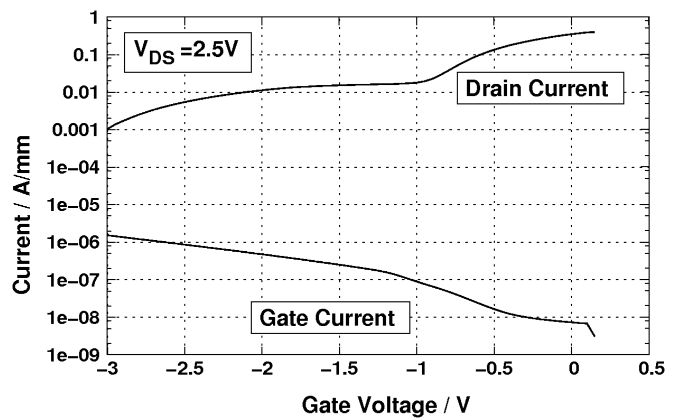

Figure 4: Drain and gate leakage currents for a transistor with $Ga_{0.52}In_{0.48}P$ buffer

For the transistors using a $Ga_{0.52}In_{0.48}P$ buffer the gate leakage current is comparable to the one shown in Fig. 2. This indicates that the Schottky diode build by the gate metalization and the semiconductor behaves the same for these transistors. The characteristics of this diode is mostly influenced by the treatment of the surface during the

processing which is the same for all presented transistors. A significant difference can be seen in the drain leakage current. Compared to the previous drain current curves for this buffer the current decreases much more slowly with decreasing gate voltage. For a gate voltage between -2.5V and -1.5V the deviation is three decades compared to the transistors using an AlAs/GaAs buffer. Even at a gate voltage of –3 V the drain current is more than two decades higher compared to the gate current. So there is still a significant current flow under the gate. This bad pinch off behavior is directly reflected by the breakdown voltage, see Fig. 5.

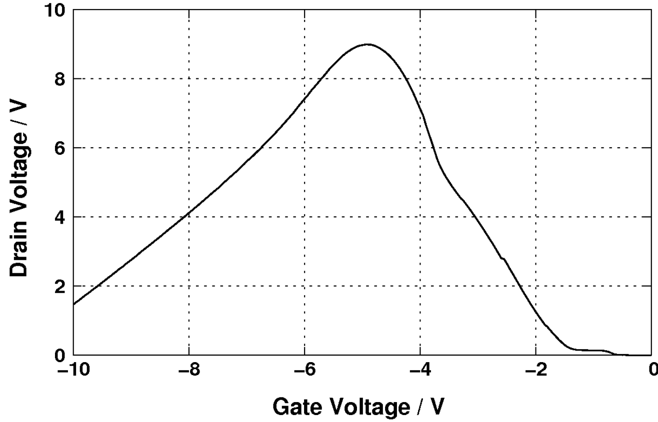

Figure 5: Breakdown voltage of a transistor with $Ga_{0.52}In_{0.48}P$ buffer

The breakdown voltage for this transistor is with V_{BDS}=9 V much lower compared to the one presented before. Also the gate voltage for this breakdown voltage shifts to a much more negative value of V_{GS}=-4.9 V. This indicates the bad pinch off behavior of this transistor.

These measurements and the simulation results show that the buffer plays also a significant role in preventing charges from flowing below the channel in the substrate which contribute significantly to the drain leakage current and influence this way the breakdown voltage.

Buffer: AlGaAs/GaAs

For this experiment three variations of a ternary $Al_{0.60}Ga_{0.40}As$ /GaAs buffer were grown. Each consists of an $Al_{0.60}Ga_{0.40}As$/GaAs super lattice but differs in the thickness of the first $Al_{0.60}Ga_{0.40}As$ layer next to the $Al_{0.25}Ga_{0.75}As$ layer, see Fig. 1. The thickness of the first layer varies between 3.0 nm and 18.5 nm. Table 1 summarizes the three buffer variations.

Table 1: Variations of the ternary $Al_{0.60}Ga_{0.40}As$/GaAs buffer

Buffer	B1	B2	B3
$Al_{0.60}Ga_{0.40}As$	3.0nm	10.0nm	18.5nm
GaAs	4.0nm	4.0nm	4.0nm
$Al_{0.60}Ga_{0.40}As$ 3nm GaAs 4nm	x 14	x 14	x 14

The motivation in this variation is to block the electrons from moving into the super lattice or even the GaAs substrate. A thicker layer of $Al_{0.60}Ga_{0.40}As$ is intended to cause a better blocking compared to a thinner first layer. This expectation is verified by measurements of the drain leakage, as can be seen in Fig. 6.

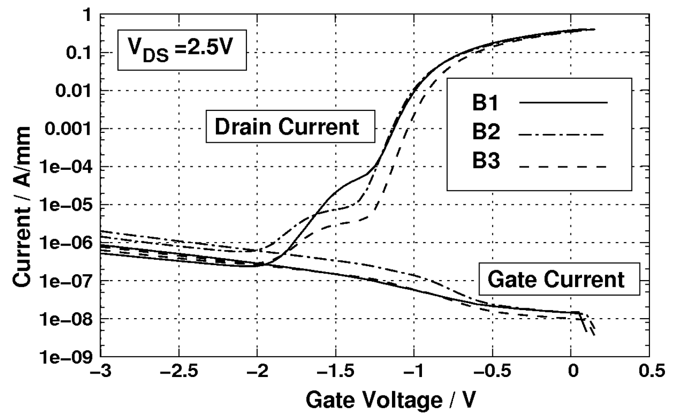

Figure 6: Drain and gate leakage of the three variations of the ternary $Al_{0.60}Ga_{0.40}As$ buffers

The correlation between the thickness of the first hetero barrier of the super lattice and the drain leakage current can be clearly seen. The buffer B1 with the lowest thickness of the first layer shows the highest drain leakage current for gate voltages below V_{GS}=-1.25 V. With increasing barrier thickness the drain leakage current decreases. This shows the importance of the first hetero barrier in reducing the leakage current.

The wafer using the buffer B3 shows additionally a horizontal shift. This is caused by a lower δ-doping compared to the others as the different layer stacks are grown in different epitaxy runs. This shift is about 0.1 V and causes also a reduction in I_{DSS} of 10%.

A comparison of the breakdown voltage V_{BDS} for this buffer variation is difficult as besides the buffer also the δ-doping is not the same on the different wafers. Therefore the relative high breakdown voltage of V_{BDS}= 17.5 V for the transistor using buffer B3 is attributed to the lower doping. The other two wafers show a breakdown voltage of about V_{BDS}=16 V.

Summary

Measurements of leakage currents and breakdown voltages of double recessed pHEMTs with different types of buffers were presented.
Two transistors using a binary AlAs/GaAs buffer grown at different times showed significant differences in the drain sub-threshold leakage currents. The transistors with the higher drain leakage current also showed a lower breakdown voltage of V_{BDS}=13.5 V compared to 15.5 V. As a result of device simulations this variation can be caused by a different background doping of the buffer.
To underline the correlation between the drain leakage current and breakdown voltage a transistor using a GaInP buffer was characterized. The $Ga_{0.52}In_{0.48}P$ shows to $Al_{0.25}Ga_{0.75}As$ a low discontinuity in the conduction band. For this transistor a significant drain leakage current was measured and the breakdown voltage is just V_{BDS}=9 V. Device simulations showed a significant current flow in the GaAs substrate at pinch off for this type of buffer.
For a ternary $Al_{0.60}Ga_{0.40}As$/GaAs buffer the first $Al_{0.60}Ga_{0.40}As$ layer was varied in its thickness. This variation showed that a thicker first hetero barrier results in a lower drain leakage currents at sub-threshold.

Acknowledgments

The authors would like to thank M. Schaefer from CADwalk (www.cadwalk.de) and Dr. G. Zandler from Silvaco (www.silvaco.de) for performing and supporting the device simulations.

References

[1] S.R. Bahl and J.A. del Alamo, “A new drain-current injection technique for the measurement of the breakdown voltage in FETs”, IEEE Trans. Electron Devices, vol. 40, pp. 1558-1560, Aug. 1993.

[2] V. Palankovski, “Analyses and Simulation of Heterostructure Devices”, Springer-Verlag, ISBN 3-211-40537-2

Acronyms

pHEMT: Pseudomorphic High Electron Mobility Transistor
MBE: Molecular Beam Epitaxy