Dual N-Channel JFET Switch

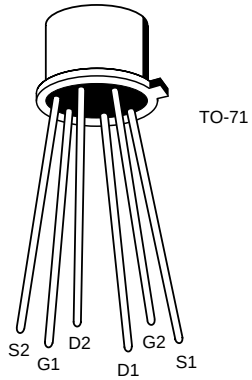
calogic
LLC

U401 – U406

FEATURES

- **Minimum System Error and Calibration**
- **Low Drift With Temperature**
- **Operates From Low Power Supply Voltages**
- **High Output Impedance**

PIN CONFIGURATION



CJ2

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

Gate-Drain or Gate-Source Voltage 50V
Gate Current (Note 1) 10mA
Storage Temperature Range . . . . . -65°C to +200°C
Operating Temperature Range . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

	One Side	Both Sides
Power Dissipation (T_A = 85°C)	300mW	500mW
Derate above 25°C	2.6mW/°C	5mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
U401-6	Hermetic TO-71	-55°C to +150°C
XU401-6	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	U401		U402		U403		U404		U405		U406		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1µA	
I_{GSS}	Gate Reverse Current (Note 2)		-25		-25		-25		-25		-25		-25	pA	V_{DS} = 0, V_{GS} = -30V	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-.5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	V	V_{DS} = 15V, I_D = 1nA	
$V_{GS(on)}$	Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3		V_{DG} = 15V, I_D = 200µA	
I_{DSS}	Saturation Drain Current (Note 3)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10V, V_{GS} = 0	
I_G	Operating Gate Current (Note 2)		-15		-15		-15		-15		-15		-15	pA	V_{DG} = 15V, I_D = 200µA	
			-10		-10		-10		-10		-10		-10	nA		T_A = 125°C
BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1µA	
g_{fs}	Common-Source Forward Transconductance (Note 3)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	µS	V_{DS} = 10V, V_{GS} = 0	f = 1kHz
g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
g_{fs}	Common-Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000		V_{DG} = 15V, I_D = 200µA	f = 1kHz
g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
C_{iss}	Common-Source Input Capacitance (Note 6)		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 6)		3.0		3.0		3.0		3.0		3.0		3.0			
e_n	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15V, V_{GS} = 0	f = 10Hz (Note 6)
CMRR	Common-Mode Rejection Ratio	95		95		95		95		90				dB	V_{DG} = 10 to 20V, I_D = 200µA (Note 5, 6)	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10V, I_D = 200µA	
$\frac{\lvert \Delta V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	µV/°C	V_{DG} = 10V, I_D = 200µA	T_A = -55°C, T_B = +25°C, T_C = +125°C

NOTES: **1.** Per transistor.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300µs; duty cycle ≤3%.
4. Measured at end points T_A, T_B, T_C.
5. CMRR = $20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS_1} - V_{GS_2} \rvert} \right]$, ΔV_{DD} = 10V.
6. For design reference only, not 100% tested.