PULSONIX

Advanced Technology Option

Users Guide

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Chapter 1. Micro-via Technology

Feature Summary

The features described below are available in the Advanced Technology suite and are available as a cost option.

The Micro-via and Layer Span features enable advanced support for Micro-vias, layer spans, composite vias for stacked Micro-vias and Board/Area spans including Cutouts.

To use Micro-vias or Board/Areas on layer spans, there is an order in which items must be created to enable subsequent processes.

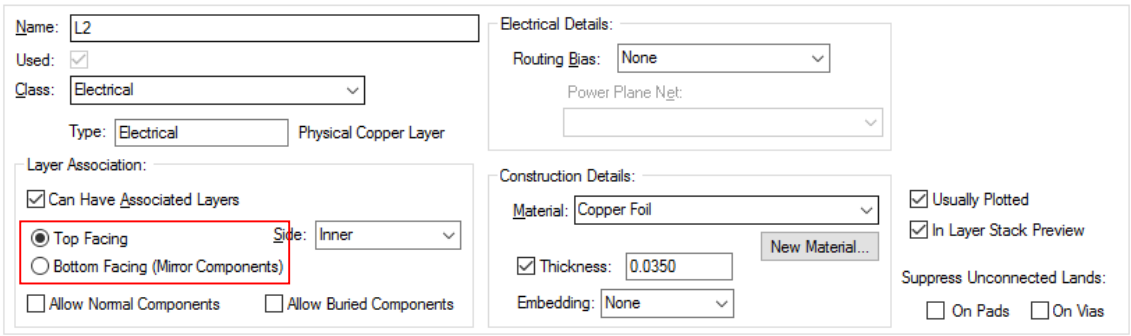
Micro-vias

For Micro-vias to be created, the individual facets must be created in the correct order and certain information defined.

Mainly, you must have two suitable layers defined that have **Can Have Associated Layers** enabled and the same facing directions (**Top Facing**, **Bottom Facing** etc.). Once in the **Layer Spans** dialog, this will now produce the correct type of layer span when created.

Micro-via Layer 'Facing' Switch

The **Top** or **Bottom Facing** switch in the **Layers** dialog (**Technology**, **Layers**) with **Can Have Associated Layers** checked, is used to define a Micro-via layer. For a Via Span to be a Micro-via type, it must have two 'same' facing sides. So for example, L2 and L3 must both be defined as facing the same way (Top or Bottom Facing). These must be defined before it can be considered as a Micro-via when creating your Layer Spans.



When using Micro-vias, the 'Facing' direction must also be defined if the layer is to be used as a **Stop layer** in the layer span definition, Stop pads are described a bit further on.

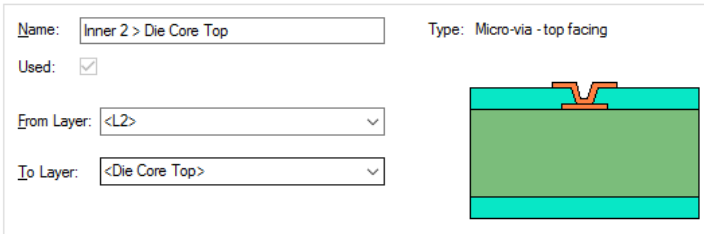
Layer Spans

For Micro-vias, once at least two layers have been defined using the same **Facing** switch, then the Layer Span can be created. **Layer Spans** are defined in the **Layer Spans** dialog from within the **Technology**. It is from here you can define layer spans to use for Vias, Micro-vias, Board Outlines, Areas and Components.

A layer span becomes a **Micro-via** type by having the same **Facing** side on its Top and bottom **Layers** as we said already. To use a micro-via technology you should define the span between **same facing layers**.

	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	T - L2	<Top Side>	<Layer 2>	Micro-via - top facing
Y	L2 - Core Top	<Die Top Cor	<Layer 2>	Micro-via - top facing
Y	Core Top - Core Bottom	<Die Top Cor	<Die Bot Core>	Buried
Y	Core Bottom - L3	<Layer 3>	<Die Bot Core>	Micro-via - bottom facing
Y	L3 - Bottom	<Layer 3>	<Bottom Side>	Micro-via - bottom facing

Layer Spans are created as you would normally using the **Layer Span** option from the **Technology** dialog. When a pair of layers are selected which have the same facing layers, the **Type:** is automatically changed to a **Micro-via**, this also shows the via 'drill' direction.



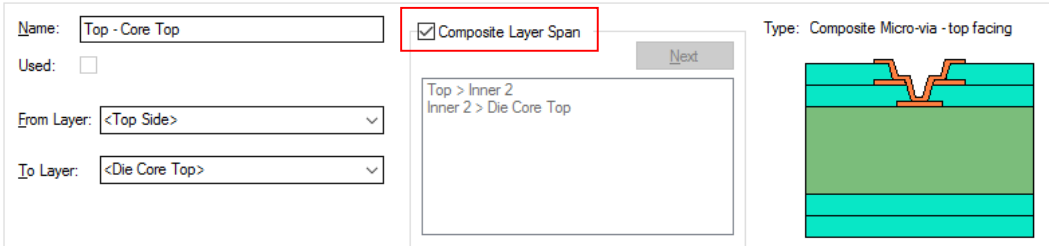
Composite Micro-via Layer Spans

Composite Spans are used for connecting multiple layer spans together. So for example, you could span Top to L2 and L2 to L3 using two individual vias. Because Micro-vias would require these to have the same coincident 'drill' points for laser or plasma drilling, the most effective method of moving these would be as a set moving as one unit. A composite span will allow this to happen but it must be defined for use.

A **Composite Layer Span** can be defined using a combination of **Micro-via** and **normal spans**. It is specifically used for creating a via 'stack', or more correctly, a Micro-via stack. That is, a stack of vias which together complete the span and which move together as one unit, this will usually involve a set of Micro-vias and sometimes includes a buried via.

Defining the Composite Spans

To do this, you must first define each span within the composite. Once created, define the **Composite Layer Span** by selecting layers from **From Layer:** and **To Layer:** using the drop down list. If these are legal layers which can create a composite span. The **Composite Layer Span** check box will be available.

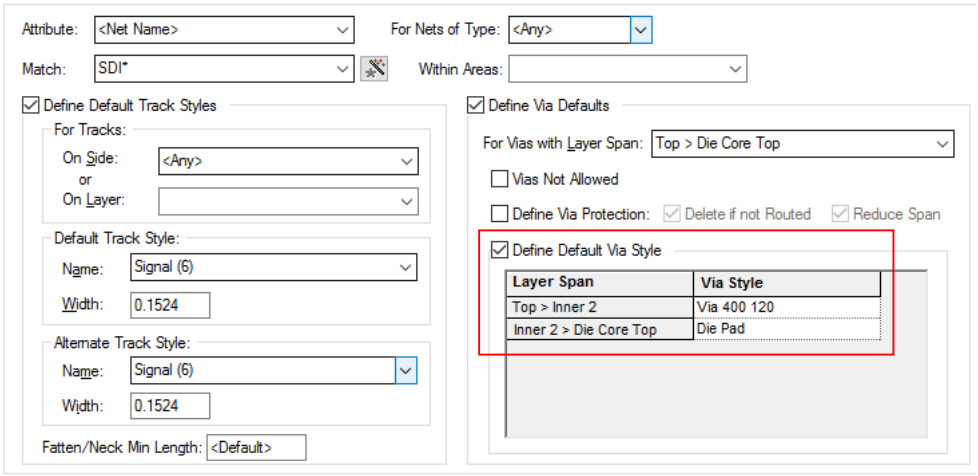


The dialog will offer each possible combination of spans which will cover this composite overall span (if there is more than one, press **Next** to cycle through each one). You can change a composite back to a normal span by unchecking the **Composite Layer Span** check box.

Once you have a composite span defined, you must then define the **Pad Style** (this will be your via) to use on each via in the stack. Only nets which have composite styles defined in the **Net Styles** dialog can use the composite span to create stacked vias.

Defining a Composite Via Span in Net Styles

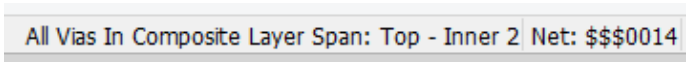
To use a **Micro-via layer span** or **Composite layer span**, you will require an entry in the **Net Styles** for a net within your **Technology**. When composite spans are used it causes a via stack to be added rather than a single via, each via in the stack using the pad style defined in the net styles entry.



Using Composite Layer Spans

Composite via stacks can be added using **Insert Via**, or added automatically by changing layers of tracks. If using Insert Via, then the same restrictions to the function will apply as when using **Insert Multiple** e.g. no finish markers, test point or design clearance etc.

Selecting a via selects all the vias in that stack, and the status bar informs you of this and the layers it spans.



This is so the stack can be moved as one, but the individual vias in the stack can still be selected using the **Select Next** option. Once a via has been moved away from the rest in the stack, the stack is no longer complete and will not be selected as one item (as a composite).

Composite span stacks can be shown in the **Layer Stack Preview**, and in the **3D Viewer**.

Stacked and Tapered Micro-vias

By defining a **Layer Span** between **two same facing layers**, vias using this span are defined as a **Micro-via**. To add extra detail to your Micro-vias, you can define the via (in **Pad Styles**) as having an **Entry Pad** and/or **Stop Pad**.

Entry Pads and Stop Pads

There are two special **Pad Style** exceptions (defined in the **Technology**) for **Micro-via Entry Pad** and **Micro-via Stop Pad**. These define the pad sizes used on the entry and stop layers when the style is used for a Micro-via (unless there is an explicit exception for that layer, which will be used instead). These provide a simple method of defining specific Entry and Stop pad sizes, **they are not mandatory for Micro-vias**.

This pad definition is used for creating 'tapered' Micro-vias, where the Entry and Stop pads are different diameters to match the 'taper' effect caused by the laser drilling.

A Micro-via showing a tapered hole

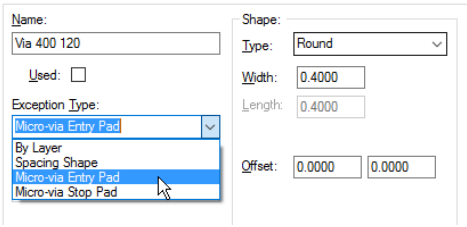
It is also possible to create a set of 'stacked' Micro-vias using a **Composite Layer Span**. Without Stop pads, the laser will simply 'cut' to a depth or until it reaches a Stop pad. Multiple 'tapered' via spans are also possible using **Composite Layer Spans** using different **Via Pad Styles**.

Two examples of Stacked Micro-vias (Composite)

Creating Entry and Stop Pads

▶ To create entry and stop pads

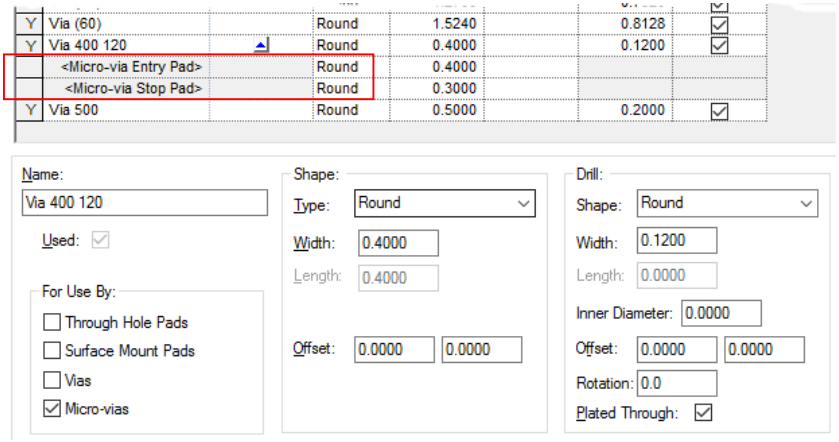
1. In the **Technology** and from within **Pad Styles**, use the **By Layer** option for a selected pad. Select the pad that requires the entry and stop pad definition.
2. For **Type:** select **Micro-via Entry** from the drop down list.
3. The **Layer:** box will now be greyed out as un-selectable.
4. Type a value for **Width:** if it needs to be different to the default stack value and then press **OK** to exit and save the exception.



5. Normally, you would also do the same for the **Stop Pad** so the laser knows where to enter and where to stop drilling, although this isn't mandatory for some processes.

6. The Stop pad is displayed as a solid pad even though the default pad stack is defined with a drill hole. The Entry pad is displayed with a drill hole shown (this is controlled on the Layer Class settings).

7. The **Pad Style** entry for that pad would then look like this for example (shown for **Via 400 120**):



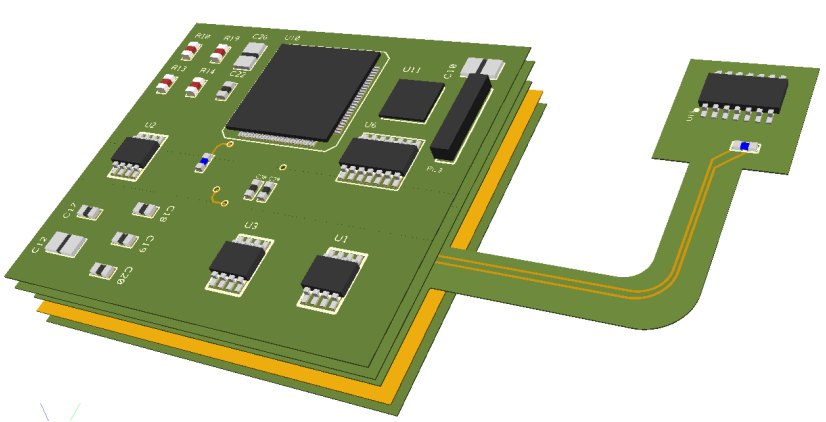
Outputs for drilling Micro-vias

Micro-vias are ‘drilled’ (using a laser or plasma ‘drilling’ machine), an output is exported from Pulsonix using the standard **Excellon NC Drill** format. Special customised reports can be generated using the **Report Maker** option on the **Outputs** menu if required. All pad styles on any layers and the drill position can be output if required, there are special Report Maker commands to allow this.

Chapter 2. Flexi-rigid Board Technology

Feature Summary

In Pulsonix, a flexi-rigid board setup is a combination of rigid and flexi boards. The flexi board is achieved by placing a different board outline on a layer span, that spans a subset of layers of the rigid board structure, representing the top and bottom flexi layers of the design. Where the flexi board outline is outside of the main board outlines, this represents the exposed flexi portion of the design.



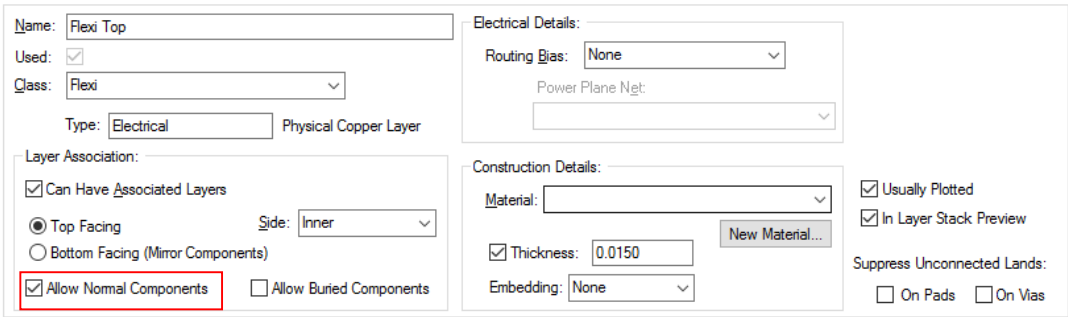
Both board outlines and board area cutouts can be assigned a layer span to support this.

Through Hole and Surface Mounted components can be placed onto exposed flex board outer layers. This is done by changing their layer to the inner layer that they will sit on. To be able to move the component onto an inner layer span, you must create a suitable **Layer Span.**

Board Spans

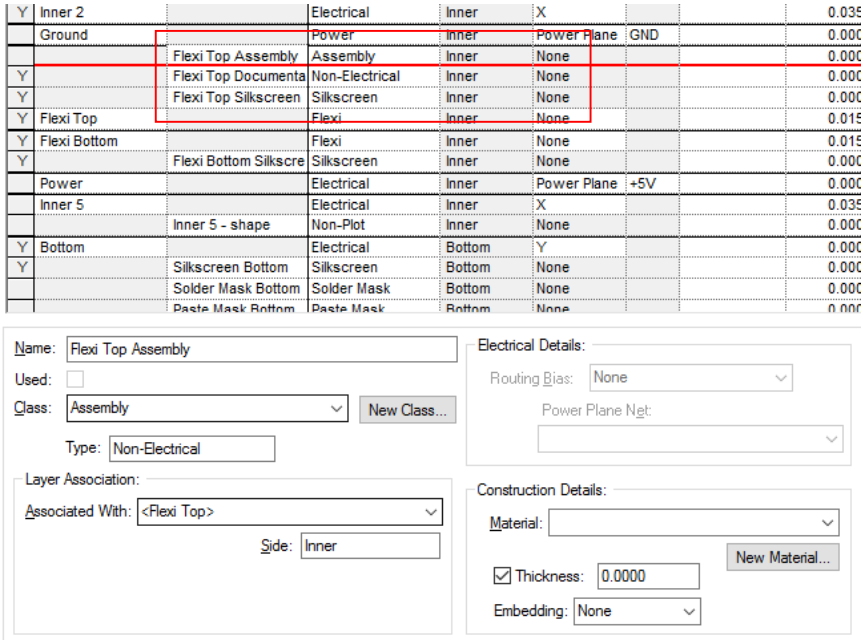
Defining Layers

Inner layers used for the outer sides of flexi boards are defined as normal layers with no special requirements other than if the flex is to contain components on that side. If they are, they must have the **Allow Normal Components** check box selected. This rule applies if you intend placing both Through Hole and Surface Mounted components.

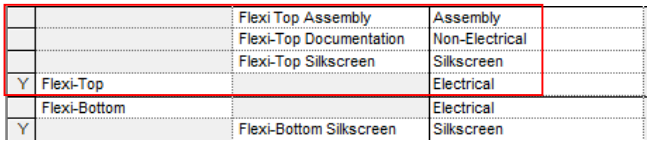


Where a component is to be placed on a flexi layer, you should ensure that all associated layers required for manufacturing are also defined for that inner flexi layer. For example, you may require a Flexi Top Silkscreen, Flexi Top Assembly and Flexi Top Documentation layers.

Where layer sets are required, the **Can Have Associated Layers** check box must be selected for the 'host' electrical layer (Flexi Top). When the associated layers are then defined, the **Associated With:** drop down selection will be available. Choose the host layer to be associated with. The **Side:** option will be pre-selected for you depending on your association choice.



Each of the associated layers can be positioned around the host layer depending on how you wish them to be viewed in the layer stack.



Defining Layer Spans

For a normal PCB design, you would have one board outline that is used for all layers, with a flexi-rigid board, you would need to define a board exception. That is, a board outline that is used on a different span of layers. A **Board** on a layer span redefines the outline for that span. For example, it is possible to define a flexi-board on an inner layer span, which overhangs the outer board outline. It is possible to add normal components to the 'overhangs'. For normal boards, the board outline would remain on <Through-board> layers.

For the creation of layers to be used for flexi boards, you need to specifically define a layer span in the **Layer Span** dialog. You will use these Layer spans to add **Board Outlines**, **Board Area Cutouts** and **Areas** onto.

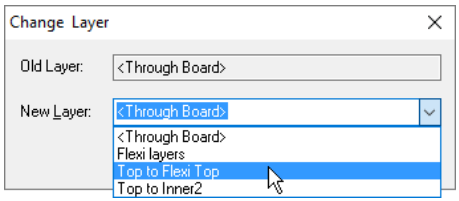
In addition, to place components on a flexi layer, you must have a **Layer Span** defined in your **Technology**. For our example, this would be **Flexi Layers** spanning the <**Flexi Top**> and <**Flexi Bottom**> layers.

	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	Flexi	<Flexi-Top>	<Flexi-Bottom>	Buried
Y	Top to Flexi top	<Top Side>	<Flexi-Top>	Micro-via - top facing
Y	Top to Inner 2	<Top Side>	<Inner 2>	Composite Blind from Top

This means you must already also have a pair of flexi layers defined in the **Layers** dialog to be spanned. In our example below, **Flexi Top** and **Flexi Bottom**.

		Flexi Top Assembly	Assembly	Inner	None
		Flexi-Top Documentation	Non-Electrical	Inner	None
		Flexi-Top Silkscreen	Silkscreen	Inner	None
Y	Flexi-Top		Electrical	Inner	None
Y	Flexi-Bottom		Electrical	Inner	None
Y		Flexi-Bottom Silkscreen	Silkscreen	Inner	None

If selecting a **Board Outline**, **Area** or **Board Outline Cutout**, use **Change Layers** to change to a Layer Span selected from the drop down list, a list created from the legal Layers Spans available. The board outline will now appear on the layer spans selected.



Component Spans

In addition, to place components on a flexi layer, you must have a **Layer Span** defined in your **Technology**. For our example, this would be **Flexi Layers** spanning the <**Flexi Top**> and <**Flexi Bottom**> layers.

	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	Flexi Layers	<Flexi-Top>	<Flexi-Bottom>	Buried
Y	Top to Flexi Top	<Top Side>	<Flexi-Top>	Micro-via - top facing
Y	Top to Inner 2	<Top Side>	<Inner 2>	Micro-via - top facing

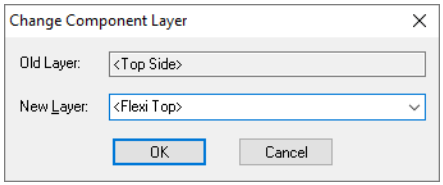
This means you must already also have a pair of flexi layers defined in the **Layers** dialog to be spanned. In our example below, **Flexi Top** and **Flexi Bottom**.

		Flexi Top Assembly	Assembly	Inner	None
		Flexi-Top Documentation	Non-Electrical	Inner	None
		Flexi-Top Silkscreen	Silkscreen	Inner	None
Y	Flexi-Top		Electrical	Inner	None
Y	Flexi-Bottom		Electrical	Inner	None
		Flexi-Bottom Silkscreen	Silkscreen	Inner	None

Placing Components on to Flexi Board layers

To move a component to a layer span

To move a component onto the new Layer Span required, select the component and from the context menu, select **Change Layer**. Select your span choice from the drop down list.



Only layer spans that start or end on layers that can have components will be available.

A **Mirror Component** check box will be available to say which side of the span the component will be placed on.

The **Design Rules Check** (DRC) option will check that pads, mounting holes etc. will fit the span defined.

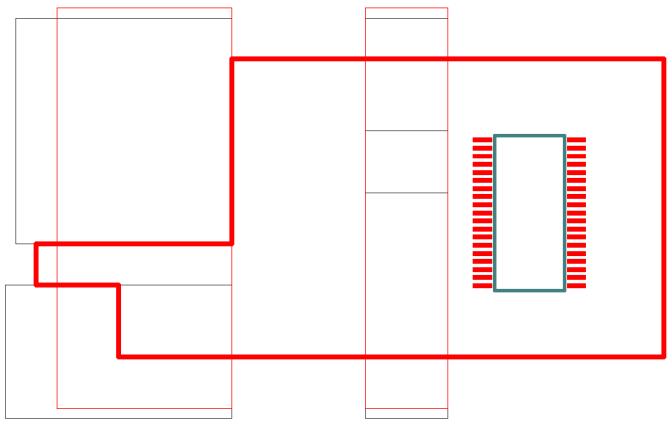
Mounting Holes in a PCB design can be assigned to a **Layer Span**. This allows you to place construction holes into the flexi board without having to use a via.

Components which are to be used on any other layer span other than conventional <Through Hole> do not need any special set up requirements but you should be aware of any supporting layers which may or may not be subsequently required, for example Silkscreen layers. You should also make provision for any supporting or associated layers which may be required once the component is on the new layers.

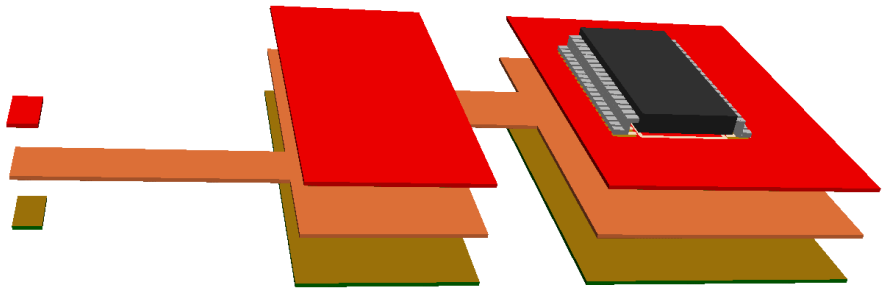
Alternative Method of producing Flexi-rigid boards using cutouts

The method of applying cutouts to spans also supports another methodology of producing flexi-rigid boards. This is where **Board Area Cutouts** are used on the flexi layers so that when the main board outline is profiled (milled or routed), it produces a flexi-rigid solution.

The picture below shows the PCB design in Pulsonix. You can see the **Board Area Cutouts** on their spanned layer and the main **Board Outline** used to create the overall design shape.



When viewed in the 3D Viewer, the design looks like this:



Chapter 3. Board Cavities

Feature Summary

You can create cavities (a cutout) in a board for a number of uses. For example, you may wish to use an Open cavity, one which exposes an inner layer to the surface. This may simply be a cavity for thermal properties or other uses. You may also drop a component into this cavity, a bare die which is connected to an outer layer using bond pads and wires, and then sealed using a bonding material. You may also use internal cavities to create a cutout within two internal layers of the board. This may be used for inserting a thinned die or semiconductor into. Generally, the internal cutout wouldn't be left void without anything actually filling it.

Using Cavities

Pulsonix allows you to create cavities in boards using **Board Area Cutouts**.

Board Area Cutouts are defined as cavities through the use of **Layer Spans** in the **Technology** dialog, the same as **Board** outlines and **Areas**. Where a cavity is to be created in a board, this is simply a **Board Area Cutout** spanning the required layer span.

Cavities can be added directly to a design or can be added to a footprint, both use the same principles for addition of the **Board Area Cutouts.**

Defining Layer Spans

A cavity must span two **electrical** layers. These layers are defined in the **Layers** dialog of the **Technology**.

	Top		Electrical	Top	None
	Prepreg		Construction		None
Y	Layer 2		Electrical	Inner	None
		Glue spots ECP L2	Glue spots ECP	Inner	None
		Cavity ECP L2	Cavity ECP	Inner	None
		Assembly ECP L2	Assembly ECP	Inner	None
Y	Die Top Core		ECP DIE Pads	Inner	No Tracks
	Core		Construction		None
Y	Die Bottom Core		ECP DIE Pads	Inner	No Tracks
		Glue spots ECP L3	Glue spots ECP	Inner	None
		Cavity ECP L3	Cavity ECP	Inner	None
		Assembly ECP L3	Assembly ECP	Inner	None
Y	Layer 3		Electrical	Inner	None
	Prepreg 2		Construction		None
	Bottom		Electrical	Bottom	None

Once suitable Layers have been created, use the **Layer Span** dialog in the **Technology** to create a 'pair' of layers to span.

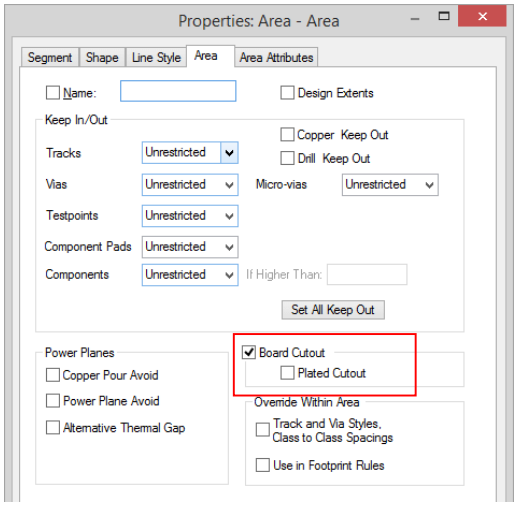
	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	T - L2	<Top Side>	<Layer 2>	Micro-via - top facing
Y	L2 - Core Top	<Die Top Cor	<Layer 2>	Micro-via - top facing
Y	Core Top - Core Bottom	<Die Top Cor	<Die Bot Core>	Buried
Y	Core Bottom - L3	<Layer 3>	<Die Bot Core>	Micro-via - bottom facing
Y	L3 - Bottom	<Layer 3>	<Bottom Side>	Micro-via - bottom facing

Board Area Cutouts

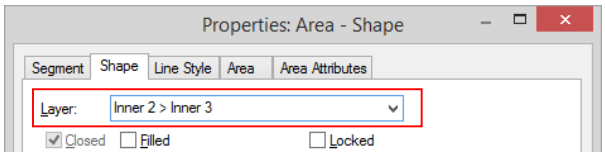
You can define cavities using a **Board Area Cutout**. These can be created in the design using **Areas** or within a Footprint. Components can be placed within cavities in the design (using the **Advanced Technology** option). If the footprint has been created with a **Board Area Cutout**, it will be self-contained with its own cavity.

Components in cavities are discussed below in the *chapter on Embedded Components.*

Once an **Area** has been added, use **Properties** of the selected area to change it usage. To be used as a cavity, the **Board Cutout** check box must be selected on the **Area** tab.



From the **Shape** tab within the **Properties** dialog, change the **Layer:** using the drop down list to span the layer span previously created.



Component creation and Areas

When creating components, Areas spanning layers can be defined up-front for use when a component is to be dropped into a cavity in the design. These are created as **Areas** and with the **Board Cutout** check box selected. Obviously, the Area needs to be defined to span the appropriate layers within the design. You should be using the same **Technology** as your design when creating components which will sit in cavities, using the same Technology becomes more essential.

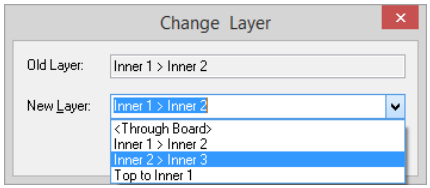
For further information about embedded components and components in cavities, please refer to the next chapter, *Embedded Component Technology*.

Placing Components into Internal Cavities

You can place components into internal and open cavities in the board, this is fully discussed in the following chapter on Embedded Components. Below is a quick summary:

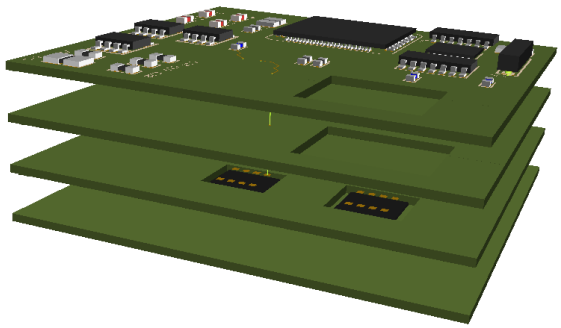
▶ To insert a component into a cavity

1. The **Layer Span** selected must have been first defined in the **Layer Span** dialog of the **Technology**.
2. Use the **Change Layer** option on the selected component. This will only be required if the footprint has been created for use on other layers.



3. You can only choose layers or layer sets for which the component was created.
4. Choose the span which the component will fit across. For example, a component might span Layer 3 to Layer 4 but sits inside the cavity that spans these layers; a cutout in the Prepreg or other construction layer.

The **3D Viewer** picture below shows two components within a cavity within the board structure. Additional cutouts on the right hand component illustrate a component exposed to the surface through the use of multiple spanned layer areas.



Chapter 4. Embedded Component Technology

Feature Summary

Pulsonix supports embedded component technology (ECT) such as printed and etched resistors, discrete embedded capacitors, buried capacitors, spiral inductors, RF components and embedded thinned die semiconductors.

Some specialist manufacturing processes allow you to place and embed components in the layer stack *within* the board. This technology allows much more efficient use of space, but requires additional features in the CAD system to enable this.

In a conventional PCB design, components can only be added to the Top or Bottom sides of the board in either through-hole or surface mounted forms. A conventional footprint will have a body which is placed above the surface of the board and pads which fit onto or through the board.

For some embedded components, they may not have a *body* like conventional components, the functionality of the component is built into the board. Using copper shapes and perhaps resistive or capacitive materials inside the layers, these make up the component itself and are created during manufacture. There are many different types of embedded component, but they all have common requirements to enable them to be added to a design correctly.

With embedded components you may want to place pads and copper shapes on inner layers and create resist or coating shapes on layers which are embedded in the board stack. When you change the layer of such a component, you would want all the associated shapes to follow the pads. In a similar way to conventional technology, you can create additional non-electrical layers which are associated with an inner electrical layer. You can also define an inner layer to be one on which embedded components are allowed to be placed. For embedded components to work correctly **it is essential to define the design technology correctly before you begin to create the footprints**.

If you are using embedded components, it is likely that you may also want to use Micro-vias as well. *Please refer to the previous Chapter on this subject.*

Overview of the ECT Process

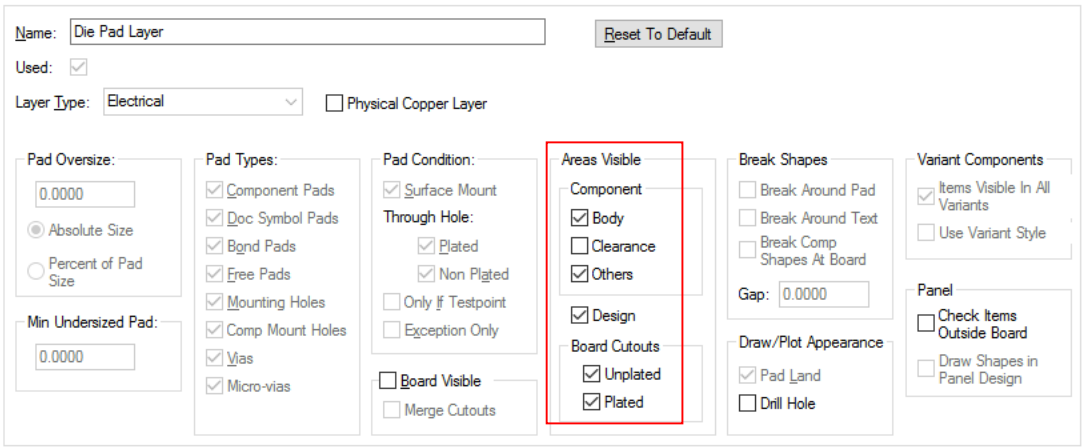
To use embedded components within Pulsonix you must create a technology to support this feature:

- Edit or create the **Technology** file that you wish to use. This will be used for the design and to create the footprint. It should contain suitable Layer Classes, Layers, Materials, Layer Spans, Pad Styles (vias) and Net Styles.
- Add **Layers Classes** and **Layers** to support embedded component technology. For layers that are critical to the final manufacturing process, select the **Essential For Manufacturing** check box in **Layers Classes** dialog.
- Add **Inner Electrical** layers and allow **Associated Layers**. Also enable **Allow Buried Components** for the electrical layer containing the embedded component.
- Add **non-electrical** inner layers to support embedded component manufacturing and documentation processes.
- Create **Layer Spans** to enable you to move your embedded component into.
- Create your footprint and save it using the **Embedded Component** check box on the **Save to Library** dialog.

Layer Classes

Layer Classes must be properly defined when creating embedded component layers or layers which are part of the embedded component itself, such as printed resistors or built-up capacitors.

From this dialog, the more important items to define for embedded technology are **Physical Copper Layer** or **Essential for Manufacturing, Areas** and **Board Cutouts**. All other items define the contents or appearance of that layer when used.



Layer Classes allows build status to be available **Physical Copper Layer** or **Essential for Manufacturing** depending on the Layer type:

Essential for Manufacturing selected – available for **Non-electrical** layers. If a Footprint contains items on an Essential layer, it cannot be added to a design which does not contain a matching layer. This is needed as you should not be able to add a embedded resistor that has its resistive material etch outline defined, on any layer in the design that does not also have an associated layer for the etch outline to live on.

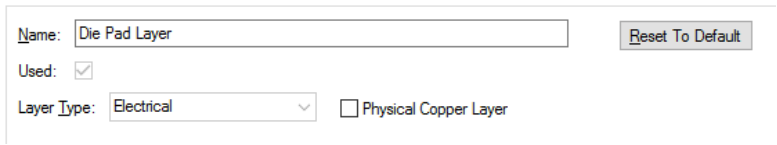
Similarly, items on non-essential layers will not be added to a design without a matching layer, but the Footprint itself can still be added. This can be useful for construction lines, dimensions or alternative outlines.

Typically, associated layers required for the manufacturing process, such as restive layers for a printed resistor would need to have this box checked. Other layers that might use this are Capacitor Dielectric and Capacitor layers.

Physical Copper Layer check box checked. This check box is only shown if the type is **Electrical**. Most electrical layers must have this box checked as they represent a physical copper layer in the construction of the final board. Uncheck it if you need an electrical layer that represents something else, for example an inner layer to display **embedded component die pads** on but not allowing copper tracks etc.

The dialog below shows 'normal' electrical layer class usage:

The dialog below shows electrical layer class usage where the layer only contains die pads:



Areas in the Layer Class dialog

For layers which 'house' the component, these need to have the **Area**, **Component**, **Body** and **Others** check boxes selected. Your selection will depend on what that layer is being used for. For example, you would select Body if the layer is being used to house the component itself. Others (placement outlines) would be used if this layer class also defines the extents of how the component is placed.

Board Cutouts in the Layer Class dialog

Board Cutouts should also be checked if this layer classes is used by the layer for embedded components. Usually cutouts are defined as unplated for internal cavities.

Layers

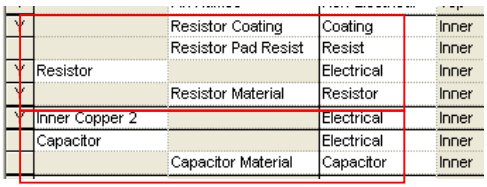
The process of creating **Layers** and **Layer Classes** is usually iterative, you may need to go round this process a couple of times to create a full set of layers required.

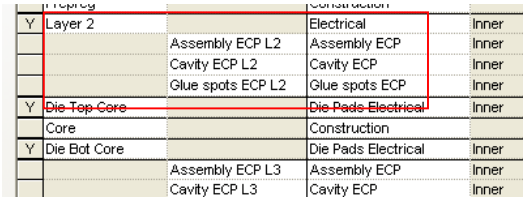
There are a number of distinct layer types required to support various embedded component technologies, these will be created depending on the level of technology you choose.

- Resistor Coating/Material
- Resistor Pad Resist
- Capacitor Dielectric
- Embedded Assembly/Glue Spot
- Die Pad layers

Layer sets

The **Layers** dialog grid allows the support for the addition of inner layer '**sets**'. Pulsonix has **sides** defined for **Top**, **Bottom** and **Inner** layer sets. Unlike conventional technology, for embedded component technology it is normal to add inner layer sets to fully create the technology, as in printed resistors, or embedded semi-conductors for example.

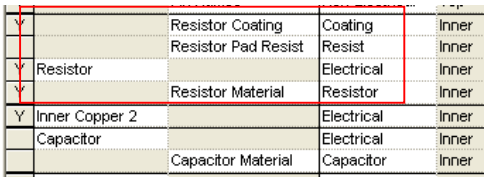




Y	Layer 2		Electrical	Inner
		Assembly ECP L2	Assembly ECP	Inner
		Cavity ECP L2	Cavity ECP	Inner
		Glue spots ECP L2	Glue spots ECP	Inner
Y	Die Top Core		Die Pads Electrical	Inner
	Core		Construction	
Y	Die Bot Core		Die Pads Electrical	Inner
		Assembly ECP L3	Assembly ECP	Inner
		Cavity ECP L3	Cavity ECP	Inner

Editing Layers

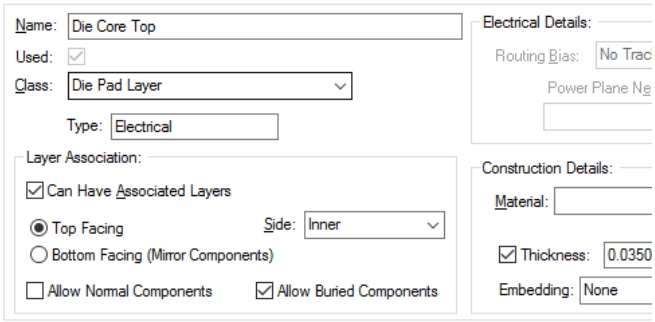
Dark horizontal lines split the rows into groups of layers associated with the same layer set to make them more visible.



Y		Resistor Coating	Coating	Inner
		Resistor Pad Resist	Resist	Inner
Y	Resistor		Electrical	Inner
Y		Resistor Material	Resistor	Inner
Y	Inner Copper 2		Electrical	Inner
	Capacitor		Electrical	Inner
		Capacitor Material	Capacitor	Inner

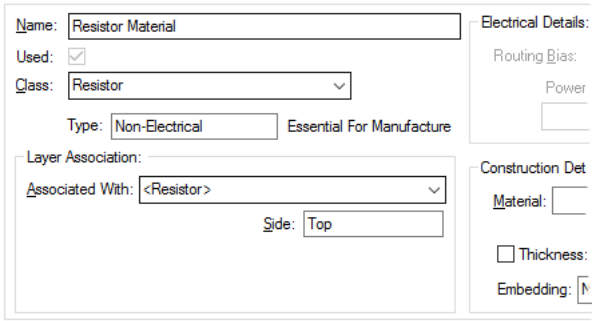
Associated Layers

For more advanced technologies, you may want to associate **Non-Electrical** layers to Inner layers. To do this, edit the inner layer and check the **Can Have Associated Layers** box. Restrictions are imposed to what you can change based on layer type.



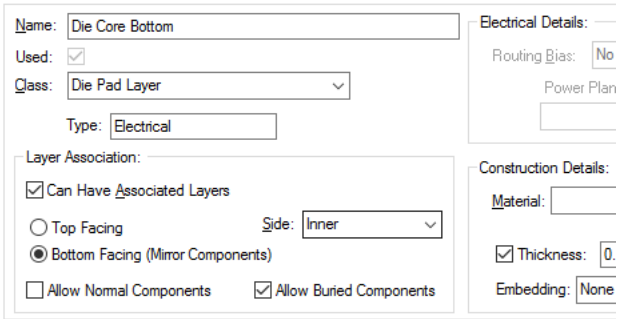
Special technologies such as those using Embedded Components (for example printed resistors) are created by enabling the **Can Have Associated Layers** on an Inner **Electrical** layer. This enables you to associate **Non-Electrical** layers with that inner layer to define the manufacturing processes required.

The inner layer set is the name of the inner electrical layer in angled brackets e.g. <Resistor>.



Facing Side

If you are using a Micro-via technology, you will need to enable **Can Have Associated Layers**, to be able to define if the layer is **Top Facing** or **Bottom Facing**. You can then define a suitable **Layer Span**. A Micro-via is always defined between two top or bottom facing layers.



Side: Top, Bottom or Inner

For more advanced technologies, you may want to associate **Non-Electrical** layers to Inner layers. To do this, select the **Side:** using the drop down list box and check the **Can Have Associated Layers** box.

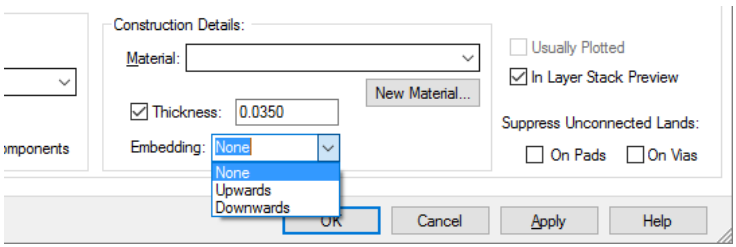
Allow Normal Components and/or Allow Buried Components

Enabling the **Allow Buried Components** option on the Inner layer allows you to add embedded components to that layer. The **Bottom Facing** check box causes components added to this layer to be mirrored.

You can mark which layer sets you can place components on by using a check box on the electrical layer – **Allow Buried Components**. For embedded components, you don't need to select the **Allow NORMAL Components** check box, this is for flexi boards (and normal boards where they are placed on the Top or Bottom sides), you do need to **Allow Buried Components** for the embedded component layer (**Die Bot Core)** though. .

Construction Details – Define Embedding

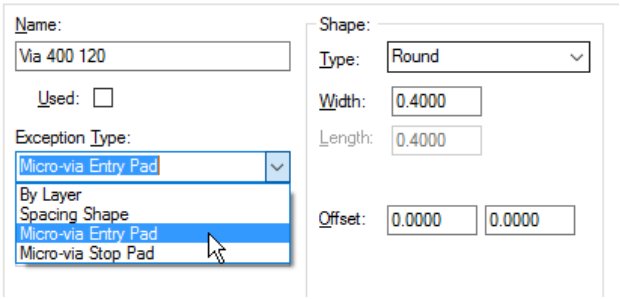
The **Embedding** drop-down allows you to specify the direction of any embedded layers with the layer directly above or below it. This is used during layer thickness calculations in Pulsonix and as a reference for manufacturers.



The **Embedding** direction isn't required for all embedded component technology, only those processes such as 'build-up' technology for Resistors and Capacitors. Soft layers, Prepreg for example, are embedded into a component layer thus eliminating real thickness of the embedded material. The embedding shows the direction the layer will use during manufacturing.

Pad Styles

Special **Pad Styles** usually need to be created to support embedded components. For example, a Pad style suitable for Micro-vias to laser drill down to embedded component layers. These can be standard pad styles or if required, can be defined using the **By Layer** option if you need it tapered or an **Entry** or **Stop** pad defined.



The **Pad Styles** entry for this pad now shows that it has been defined as a Micro-via and its type (Entry or Stop pad).

	Name	Layer	Shape	Width	Length	Drill Hole	Plated
	MicroVia		Round	0.400		0.120	☑
		Micro-via Stop Pad	Round	0.300			
	Mounting Hole		Round	3.750		1.125	☑
Y	Round (1.4)		Round	1.400		0.750	☑
Y	Via (1.25)		Round	1.250		0.650	☑

Layer Spans

Layer Spans must be created to support inner layer components. For Buried Resistors or Capacitors, these would be fairly standard Electrical layers with no special layer span requirements. For embedded semi-conductors or thinned dies that sit in a cavity within a core layer for example, layer spans would be required on which to embed the component. In our example below, this would be **Core Top to Core Bottom**.

	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	T - L2	<Top Side>	<Layer 2>	Micro-via - top facing
Y	L2 - Core Top	<Die Top Cor	<Layer 2>	Micro-via - top facing
Y	Core Top - Core Bottom	<Die Top Cor	<Die Bot Core>	Buried
Y	Core Bottom - L3	<Layer 3>	<Die Bot Core>	Micro-via - bottom facing
Y	L3 - Bottom	<Layer 3>	<Bottom Side>	Micro-via - bottom facing

If we use the following as a sample 4 layer board with 2 layers each side of the embedded core, the Layers dialog would look like this:

	Name	Associated Layer	Class	Side
		Wires Top	Wire Link	Top
Y		Silkscreen Top	Silkscreen	Top
		Solder Mask Top	Solder Mask	Top
		Paste Mask Top	Paste Mask	Top
Y		Pin Names	Non-Electrical	Top
Y	Top		Electrical	Top
	Prepreg		Construction	
Y	Layer 2		Electrical	Inner
		Glue Spots ECP L2	Glue Spots ECP	Inner
		Cavity ECP L2	Cavity ECP	Inner
		Assembly ECP L2	Assembly ECP	Inner
Y	Die Core Top		Die Pad Layer	Inner
	Core		Construction	
Y	Die Core Bottom		Die Pad Layer	Inner
		Glue Spots ECP L3	Glue Spots ECP	Inner
		Cavity ECP L3	Cavity ECP	Inner
		Assembly ECP L3	Assembly ECP	Inner
Y	Layer 3		Electrical	Inner
	Prepreg 2		Construction	
Y	Bottom		Electrical	Bottom
		Silkscreen Bottom	Silkscreen	Bottom
		Solder Mask Bottom	Solder Mask	Bottom
		Paste Mask Bottom	Paste Mask	Bottom
		Wires Bottom	Wire Link	Bottom
Y		Pin Names (Bottom)	Non-Electrical	Bottom
	Construction Lines		Documentation	
	Documentation		Documentation	

Additional layer spans would be created for the following, you would use your own layer names and span names obviously:

- Span **Top Side to Bottom Side** for 'normal' vias, by default this will be **<Through Hole>** created for you by Pulsonix.
- A span is needed between **Die Core Top** and **Die Core Bottom** (to span the cavity), this will be marked as **Buried**
- Span **Top** to **Layer 2** as **Micro-via**
- Span **Layer 2** to **Die Core Top** as **Micro-via**
- Span **Die Core Bottom** to **Layer 3** as **Micro-via**
- Span **Layer 3** to **Bottom** as **Micro-via**

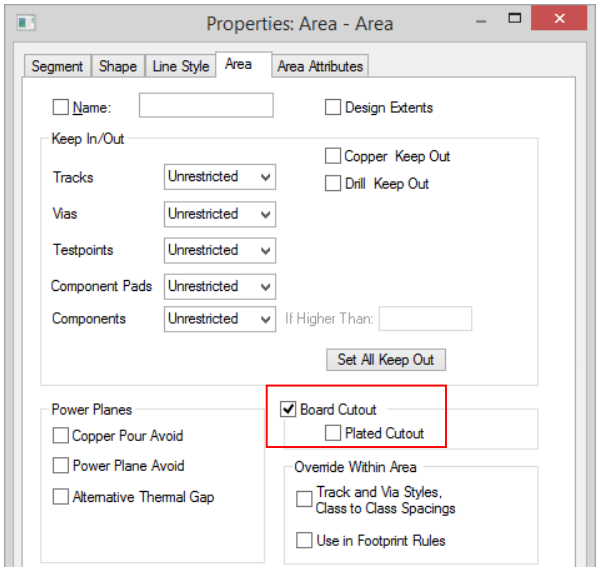
If you require additional drill spans, these can also be added. For example **Composite** layer spans are added by combining existing suitable layer spans.

Footprints for Embedded components

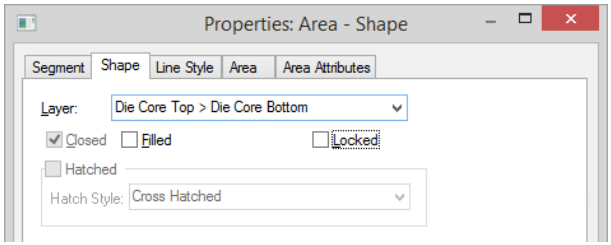
Following the successful creation of your Technology file, you can build the footprint using this file. It is important for embedded components to keep the Technology file used for the footprint in-sync with the master Technology file created. If you failed to create the correct layers in the footprint for example, your embedded footprint wouldn't load into the PCB design.

Areas as Board Cutouts

During footprint creation, we suggest adding the **Cutout Area** for the cavity into the footprint. It needs to be an **Area** defined as **Board Cutout** in the **Properties**.



The **Area body** of the component should live on the bottom layer of the layer span defined for the embedded component, in our example **Die Bot Core**, this being spanned with **Die Top Core**.



The **Layer Span** being defined like this:

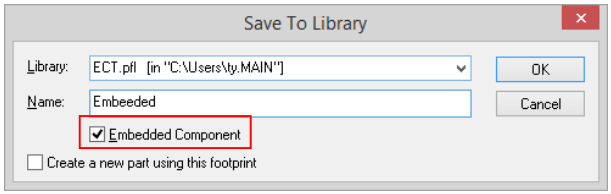
	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	T - L2	<Top Side>	<Layer 2>	Micro-via - top facing
Y	L2 - Core Top	<Die Top Cor	<Layer 2>	Micro-via - top facing
Y	Core Top - Core Bottom	<Die Top Cor	<Die Bot Core>	Buried
Y	Core Bottom - L3	<Layer 3>	<Die Bot Core>	Micro-via - bottom facing
Y	L3 - Bottom	<Layer 3>	<Bottom Side>	Micro-via - bottom facing

Adding pads/vias and areas/shapes onto layer spans

Pads for embedded components should be ‘layered’ and not Through Hole. During the footprint creation, add pads to the required layer.

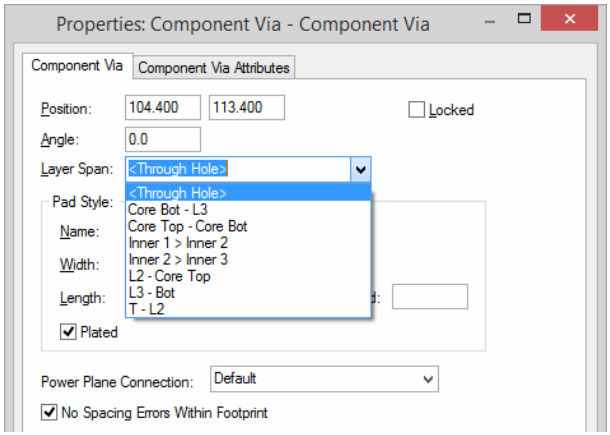
Save To Library

Footprint must be saved as an **Embedded Component** using the check box provided**.** A component should be created for this footprint but there is nothing special about the component definition itself.



Component Vias

You can add **Component Vias** to the footprint. The **Layer Span** can be changed to one selected from the technology file, this could be between an inner layer and the die pads layer. A suitable **Pad Style** for the via should also be selected to connect the inner layer to the die pad. Co



During creation, using the **Properties** for the via, these can be defined using the flag **No spacing check within footprint** set so that they can join two pads without any DRC errors when checked (for a embedded resistor via for example).

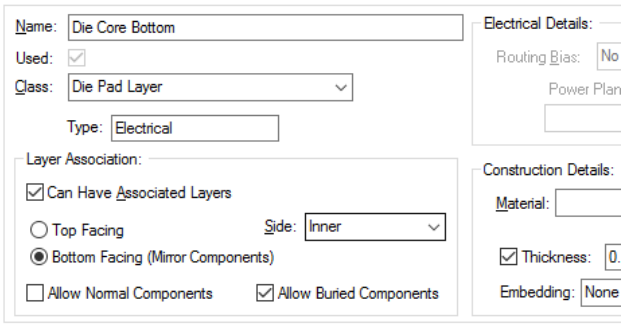
Inserting Embedded Components

When adding an embedded component to a design, it will try to place the device on the top most layer used in the footprint. An embedded component in a PCB design will show its layer on the status bar. If the layers it was defined on do not exist in the design, it will be placed on the top most layer set that contains all the **essential** layers used in it. However, it is better to use the same Technology file for the design and the footprint to avoid layer mismatches.

The process for changing layers of a component is the same for both ‘layer mounted’ and embedded components, except that layered components use a specific layer to live on whereas embedded components are inserted into a layer span containing the cavity.

Using Change Layer

You can select an embedded component and use the **Change Layer** option from the context menu or by pressing the default L key, to set its layer or Layer Span in the design. The **Mirror** option will not be available as a mirror is automatically performed when changing layers to a layer that is marked as an opposite **Facing** side, **Bottom Facing** for example.

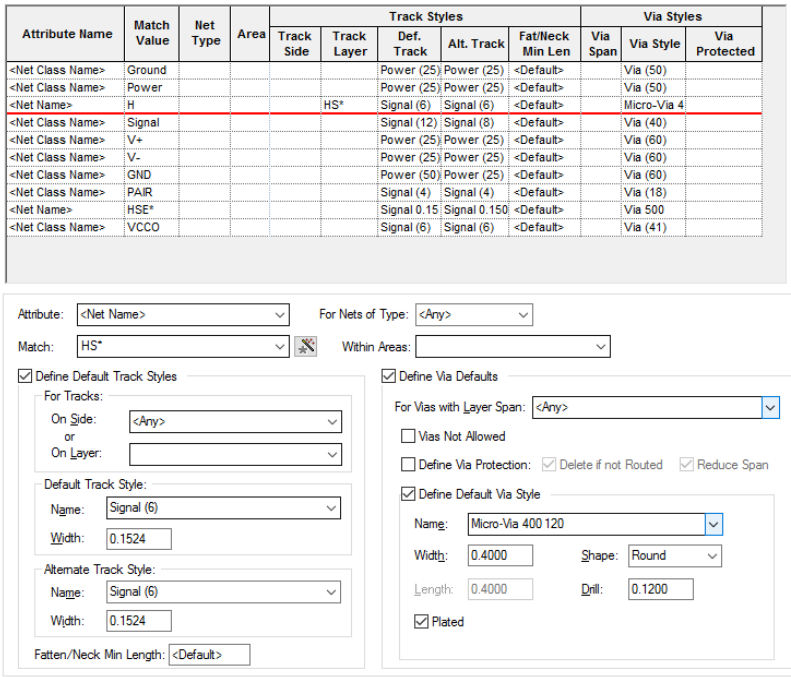


You cannot change an embedded component to a layer set that does not have an associated essential layer to place its critical items on. Copper and Pads are assumed to be essential.

Net Styles

Generally speaking, the advanced technologies will tend to use **Net Styles** to define via and Micro-via definitions for use in the design.

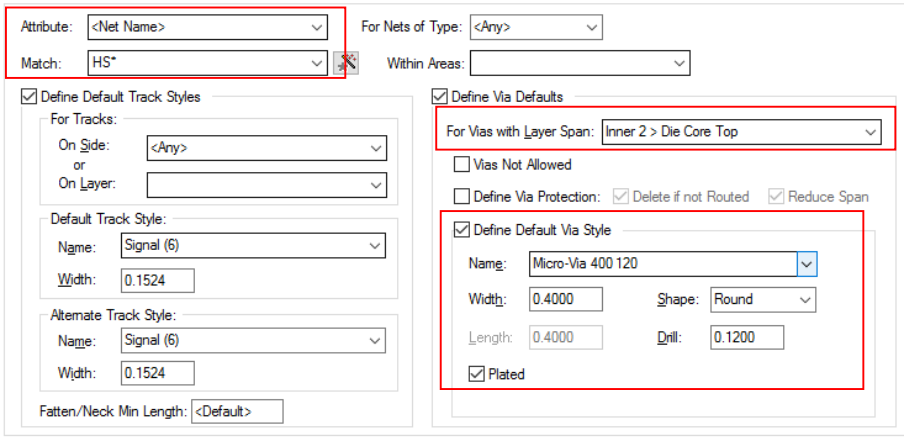
Net Styles appears as a net option on the **Technology** dialog. This will allow you to set up your Micro-vias for net items.



Attribute Name	Match Value	Net Type	Area	Track Styles					Via Styles		
				Track Side	Track Layer	Def. Track	Alt. Track	Fat/Neck Min Len	Via Span	Via Style	Via Protected
<Net Class Name>	Ground					Power (25)	Power (25)	<Default>		Via (50)	
<Net Class Name>	Power					Power (25)	Power (25)	<Default>		Via (50)	
<Net Name>	H				HS*	Signal (6)	Signal (6)	<Default>		Micro-Via 4	
<Net Class Name>	Signal					Signal (12)	Signal (8)	<Default>		Via (40)	
<Net Class Name>	V+					Power (25)	Power (25)	<Default>		Via (60)	
<Net Class Name>	V-					Power (25)	Power (25)	<Default>		Via (60)	
<Net Class Name>	GND					Power (50)	Power (25)	<Default>		Via (60)	
<Net Class Name>	PAIR					Signal (4)	Signal (4)	<Default>		Via (18)	
<Net Name>	HSE*					Signal 0.15	Signal 0.150	<Default>		Via 500	
<Net Class Name>	VCCO					Signal (6)	Signal (6)	<Default>		Via (41)	

Each **Net Style** is defined for a **Net Item** or **Attribute**. You can set multiple rules per net item, these are used for routing and they define the way the routing behaves while being added to the design. You can define the style of a track (that uses this net item) on a particular layer or area for example. Likewise, you can define what Micro-via layer span is used when changing a track from one layer to another.

Using the **Net Styles** dialog, you can define a rule for a net item. In the example below, for a **Via Span** between **L2** and **Core Top**, the **Via** style used will be the **Micro-via** style defined in the **Pad Styles** dialog.

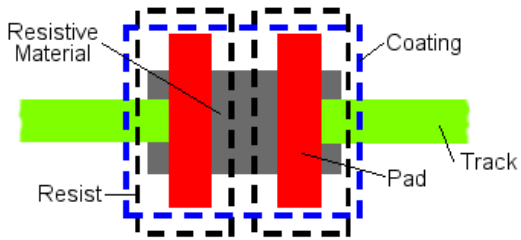


Embedded Resistors

The previous text in this section has discussed general points about setting up your Technology file and design to use embedded components. The following sections specifically detail how to setup designs for use with individual types of embedded components and technology.

Printed Resistor Overview

A printed resistor consists of two (or possibly more) pads, connected by resistive material. Printed embedded resistor pads can be added, the manufacturing process can differ but the layer definitions will be the same. Depending on the build-up manufacturing method, a resist mask or encapsulating coating may also be required. The technology would therefore require an electrical layer with associated non-electrical layers for the resistive material, resist and coating shapes.

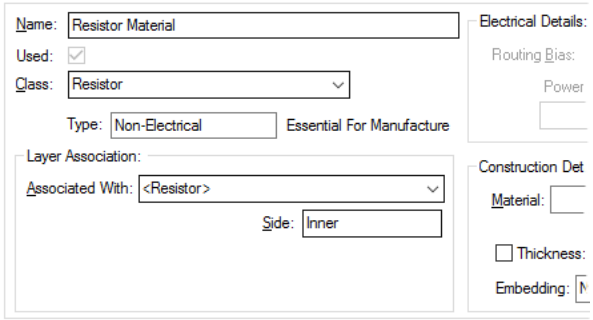


Embedded Resistor Implementation

A printed resistor set would be constructed from one or more layers associated with the master layer.

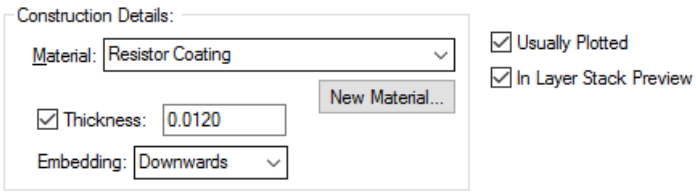
Y		Resistor Coating	Coating	Inner
		Resistor Pad Resist	Resist	Inner
Y	Resistor		Electrical	Inner
Y		Resistor Material	Resistor	Inner
Y	Inner Copper 2		Electrical	Inner
	Capacitor		Electrical	Inner
		Capacitor Material	Capacitor	Inner

If you want to place embedded resistors on an inner electrical layer, you would first define this layer as one which **Can Have Associated Layers** and as one which can **Allow Buried Components**. This is done when creating the **Technology** in the **Layers** dialog.



The appropriate non-electrical layers would then be created, and **Associate** them with the master inner layer. It would be appropriate to define the **Layer Class** for these non-electrical layers as **Essential For Manufacture**, this would prevent the component from being added to electrical layers which do not have these associated layers present.

Also, depending on the pad type chosen, printed or ceramic, you may also need to select **Embedding** and the **Material** name, **Thickness** and direction.

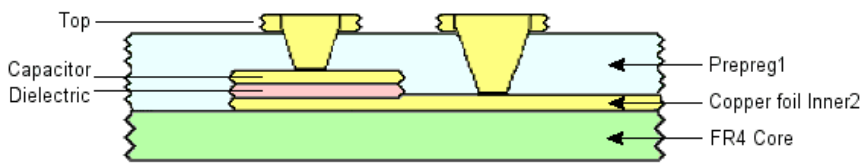


Using this Technology, a footprint can be created with the appropriate shapes. When saving the footprint, on the **Save To Library** dialog, it should be marked as an **Embedded Component**, this tells the system that this footprint can be placed on inner layers.

Embedded Capacitors

Discrete Embedded Capacitors

An embedded capacitor consists of two pads on two individual layers, separated using dielectric material. One of the layers (marked as Capacitor in our example) would be specifically used for 'landing' pads to one side of the capacitor. This would be isolated from the other capacitor pad with a thin dielectric construction layer. The Capacitor and Dielectric layers would be constructed during manufacturing using a 'build-up' technique which would add no significant thickness to the Electrical layer Inner 2. The Capacitor would be a thin copper foil applied to the pad areas where the capacitor is defined.



The **Layers** within the **Technology** would look like this to accommodate the capacitor:

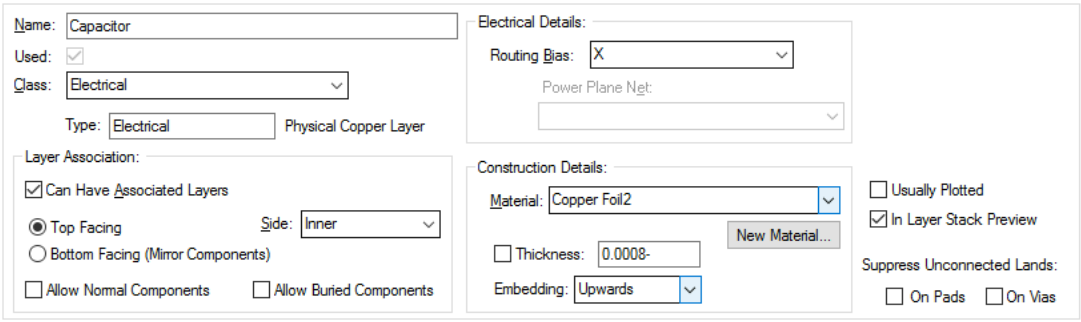
	Top		Electrical	Top	X	Copper Foil
	Prepreg1		Construction		None	Prepreg
Y	Capacitor		Capacitor	Inner	None	Copper Foil
	Dieelectric		Construction		None	Dieelectric
Y	Inner 2		Electrical	Inner	None	Copper Foil
	FR4		Construction		None	FR4
	Inner 3		Electrical	Inner	None	Copper Foil
	Prepreg2		Construction		None	Prepreg
	Bottom		Electrical	Bottom	Y	Copper Foil

The **Layer Spans** used to connect between these layers would look something like this (other layer spans would be included, the ones shown cover the immediate top layers):

	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
	Top - Capacitor	<Top Side>	<Capacitor>	Micro-via - top facing
	Top - Inner 2	<Top Side>	<Inner 2>	Micro-via - top facing

The Capacitor layer has a number of important elements to make it function correctly; the **Layer Class** is predefined with **Physical Copper Layer** unchecked (not selected). This layer will not be plotted and will not allow tracks or other pads. Only the Micro-via layer span will connect to it.

Within the Layer itself, **Can Have Associated Layers** is selected, the layer is **Top Facing** and **Allow Buried Components** is selected. Embedding for this layer is defined as **Upwards**. A Thickness would also be defined but it doesn't affect the overall layer thickness of the Inner 2 layer.

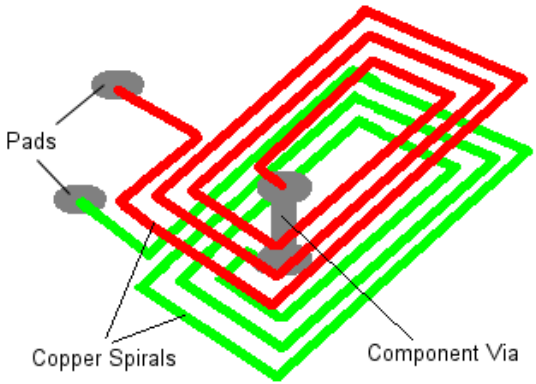


Embedded Capacitor Footprints

Using this Technology, a footprint can be created with the appropriate shapes. When saving the footprint, on the **Save To Library** dialog, it should be marked as an **Embedded Component**, this tells the system that this footprint can be placed on inner layers.

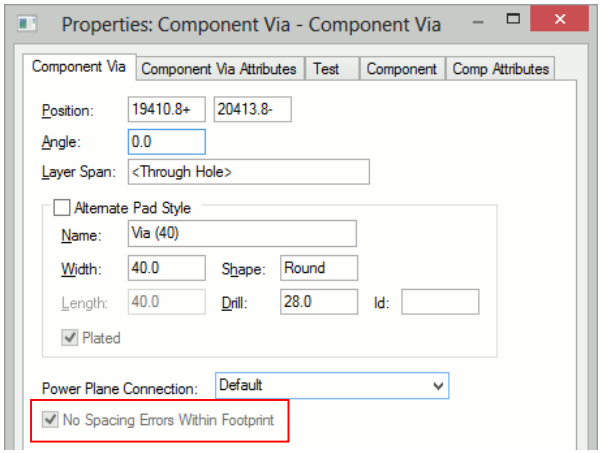
Planar Converter (Planar Transformer)

Planar Converters or **Planar Transformers** are possible using the Advanced Technology option.



This type of component spans any number of layers in the design and may have a physical body applied to the outer layers. However, part of the footprint consists of copper spirals which are connected by a component Via, effectively joining the two footprint pads. Although the pads are joined, we would want to connect them to different nets.

To connect them to different nets, ensure the **Copper spirals** and **Component Via** are not checked when a **Design Rule Check** is run. In **Properties** of the Component's footprint, select the **No Spacing Errors Within Footprint** check box for the **Component Via** entry.



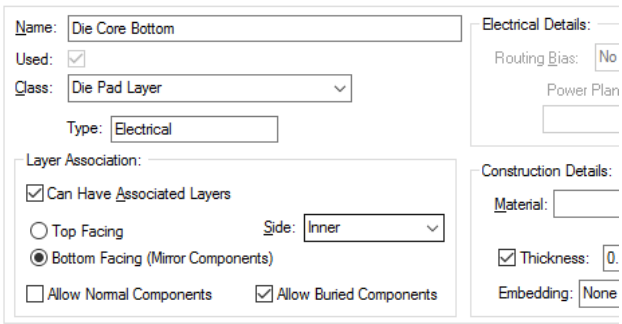
A Component Via is a fixed part of a footprint, but unlike a pad or mounting hole, it exists on a **layer span**, like a normal routing via. When defined, if this footprint is not marked as an Embedded Component, mirroring the component would not swap the inner electrical layers. By defining the footprint as an Embedded Component, you can mirror the component and all the inner layers will swap as expected.

Embedded Semiconductors and Thinned Dies

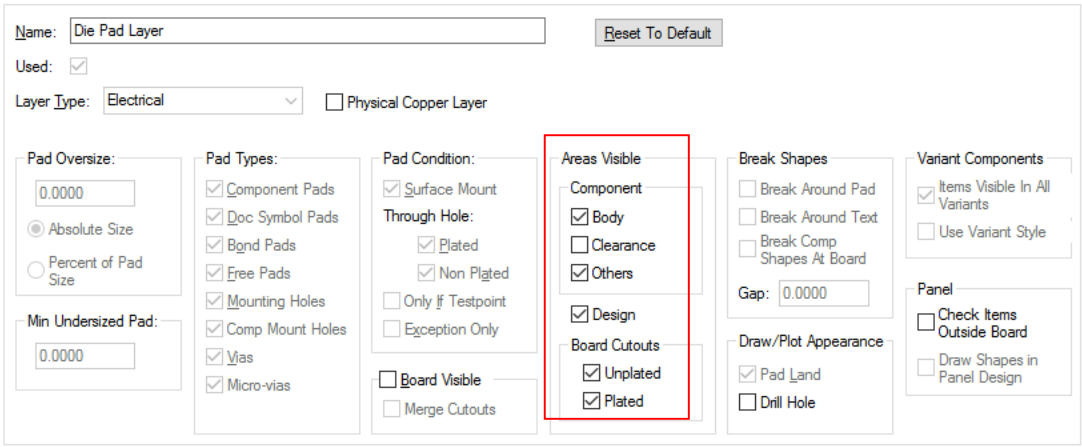
This has been fairly well discussed above. The most important point for embedding thinned dies into a cavity within a board layer is to create pseudo layers (Die Top Core and Die Bot Core in our example), these are not plotted but they do have component pads to 'land' the Micro-vias onto when laser-drilled from electrical layers. These layers are **Electrical** but the **Physical Copper Layer** check box is left unselected. The layer is then automatically marked as **No Tracks**.

	Name	Associated Layer	Class	Side	Bias
		Wires Top	Wire Link	Top	None
Y		Silkscreen Top	Silkscreen	Top	None
		Solder Mask Top	Solder Mask	Top	None
		Paste Mask Top	Paste Mask	Top	None
Y		Pin Names	Non-Electrical	Top	None
Y	Top		Electrical	Top	X
	Prepreg		Construction		None
Y	Layer 2		Electrical	Inner	None
		Glue Spots ECP L2	Glue Spots ECP	Inner	None
		Cavity ECP L2	Cavity ECP	Inner	None
		Assembly ECP L2	Assembly ECP	Inner	None
Y	Die Core Top		Die Pad Layer	Inner	No Tracks
	Core		Construction		None
Y	Die Core Bottom		Die Pad Layer	Inner	No Tracks
		Glue Spots ECP L3	Glue Spots ECP	Inner	None
		Cavity ECP L3	Cavity ECP	Inner	None
		Assembly ECP L3	Assembly ECP	Inner	None
Y	Layer 3		Electrical	Inner	None
	Prepreg 2		Construction		None
Y	Bottom		Electrical	Bottom	Y
		Silkscreen Bottom	Silkscreen	Bottom	None
		Solder Mask Bottom	Solder Mask	Bottom	None
		Paste Mask Bottom	Paste Mask	Bottom	None
		Wires Bottom	Wire Link	Bottom	None
Y		Pin Names (Bottom)	Non-Electrical	Bottom	None
	Construction Lines		Documentation		None
	Documentation		Documentation		None

The **Layer** detail for the die pad layers would look like this:



The **Layer Class** for this layer would look like this. It allows for the component **Body** to sit on this layer, for an **Other** Area of a **Board Cutout** to also exist on this layer.

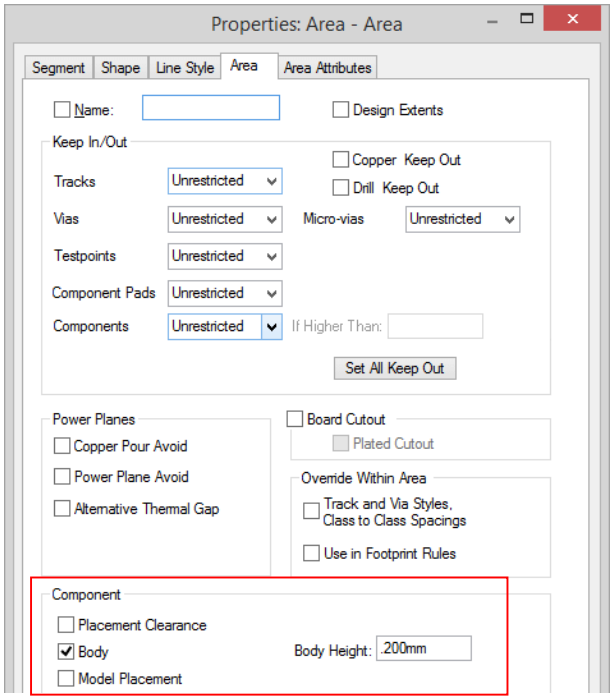


Layer Spans would be created to connect the die layers with the other electrical layers. Suitable **Micro-via** definitions in the **Pad Style** dialog would also be created to support this.

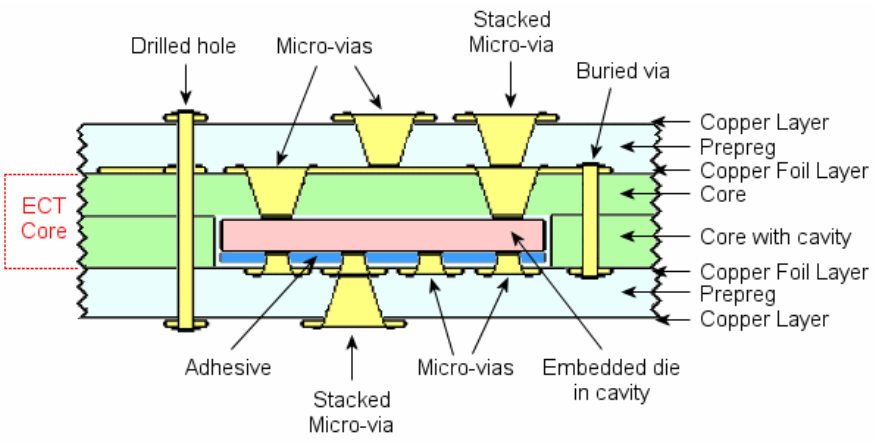
	Name	From Layer	To Layer	Type
Y	<Through Hole>	<Top Side>	<Bottom Side>	Through Hole
Y	T - L2	<Top Side>	<Layer 2>	Micro-via - top facing
Y	L2 - Core Top	<Die Top Cor	<Layer 2>	Micro-via - top facing
Y	Core Top - Core Bottom	<Die Top Cor	<Die Bot Core>	Buried
Y	Core Bottom - L3	<Layer 3>	<Die Bot Core>	Micro-via - bottom facing
Y	L3 - Bottom	<Layer 3>	<Bottom Side>	Micro-via - bottom facing

Embedded Footprints

When creating the footprint for this technology, you must also remember to include a **Body Height** in the **Area** used to define the **component body**. If you do not do this, your component will not be positioned correctly when verifying the design in the **3D Viewer**.



The final layer stack would look like this:



Chapter 5. Chip-On-Board Feature

Chip-On-Board (COB) Technology Overview

The Chip-On-Board functionality within Pulsonix enables the support for single and multiple Chip-On-Board (COB) technology. Chip-On-Board is the use of a bare die directly onto the PCB substrate rather than using the traditional packaging of the device. Attaching a bare die directly to the board enables a large space saving; traditional packaging, even the very small ones still use significantly more 'real estate' than this method.

Feature Summary

Within the Pulsonix Advanced Technology option you have a set of features which enable the creation of Chip-On-Board footprints and subsequent PCB design.

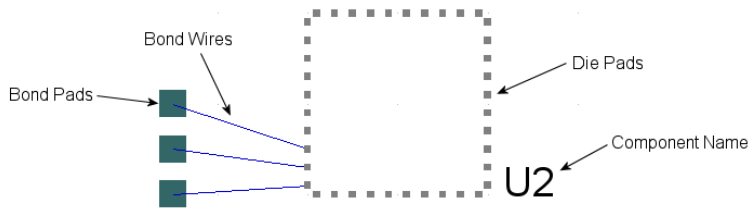
Chip-On-Board technology in Pulsonix is made up of a number of design items:

Bond Pads and **Die Pads** (specific to this product option) and **Wires**, (wires are available generally across the Pulsonix PCB design editor but have special properties and automatic insertion on this option).

Bond pads are specially defined pads. They use Pad Styles and electrical layers defined as you would for any other design but because of the licensing, these pad styles can be added as Bond Pads. Unlike normal component pads, they can be moved independently of other pads in the same component in the PCB design. Bond pads will share the same pad number as the Die pad if they are connected using a wire.

Die pads are also specially defined pads. They use normal Pad Styles as well but once added as Die Pads, they appear on a **Wire** layer. Wire layers use a special **Layer Class** of **Wire**. A **Wire** layer is connected to as a 'pseudo' electrical layer, a layer which can only contain Wire and Die Pads. You can connect to it but do plot its contents with the other electrical items.

Wires connect the Die Pads to the Bond Pads, often called **Bond Wires**. Wires are not the same as connections in the design; they have special properties. Wires appear on the wire layer along with the die pads. When a wire connects the die pad to the bond pad, they take the same net name. Wires are not normally plotted but you can extract a report of the wire start and end positions for use with automatic wire machines.



Chip-On-Board Feature Detail

- Add bond pads using **Insert Bond Pad** and add die pads using **Insert Die Pad.**
- For the Die and Bond pads to be connected together use a **Wire** so that they have the same net name. During **Insert Die Pad**, a bond pad is automatically added with a connecting wire.
- Automatic **rotation** of the bond pads is possible during positioning around the shape or during interactive moving of the bond pads.
- Use the **Properties** dialog to convert from a 'normal' pad to a Die Pad if you haven't used the **Insert Die Pad** option.
- Use **Place Bond Pads** to place bond pads around a user defined shape for specific positioning.
- In the PCB design editor, you can move 'floating' bond pads on components independently of the die component body (normal pads are in fixed positions).
- In the PCB design editor, you can move the die 'body' (that's all the die pads as one unit) on components independently of the bond pads. You may do this following accurate positioning of the bond pads.
- Check Chip-On-Board components within the design for specific rules defined.
- Use the Library Generator toolkit to write an import file for importing components containing Bond pads, Dies pads and connecting Wires.

Where no license is available for this option but the design has used specific Chip-On-Board design items they can be viewed but not manipulated.

Parts created which use PCB Footprints specific to Chip-On-Board technology do not affect the Schematic design editor, they will use normal Schematic Symbols but the translation of the design to the PCB design editor will then utilise the Chip-On-Board features.

Using the Chip-On-Board Feature

Technology Settings

There are a number of Chip-On-Board technology features which can be used in Pulsonix, these are detailed below:

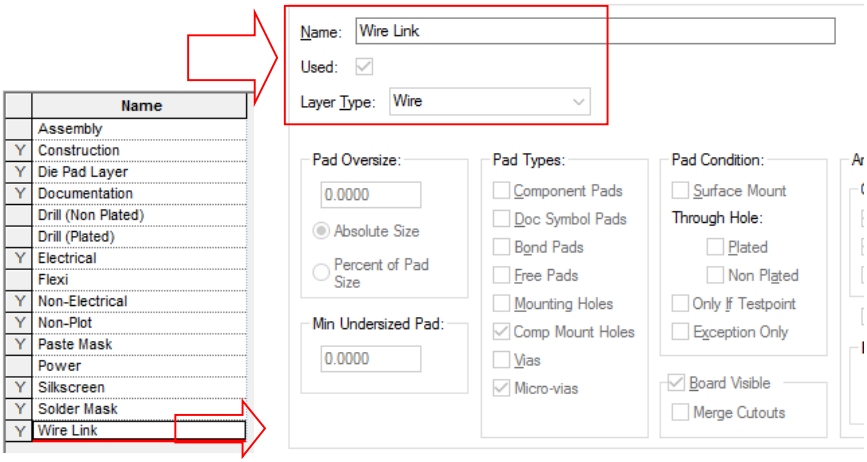
Pad Styles

Although Pad Styles used for this feature are not distinctive until used in the PCB footprint or design, they should be considered during the creation of your technology file. Generally speaking, you will create two types of pad styles to be used for Chip-On-Board technology; Bond Pads and Die Pads. **Die pads** are used to connect the chip 'die' to the 'outside' world and are of a fixed position. These are usually very small, they do not get plotted so are effectively just reference positions on the die. **Bond Pads** are connected to the die pads using wires, these are used to connect the die into the design and are surface mounted, usually rectangular or square.

	Name	Layer	Shape	Width	Length	Drill Hole	Plate
Y	Bond Pad		Rectangle	0.3	0.8	0.0	☑
Y	Die Pad		Square	0.1		0.0	☐

Layer Class

Wires require their own **Layer Class** for addition to the footprint or design. When editing the Layer Class, choose the **Layer Type**: of **Wire** from the drop down list.

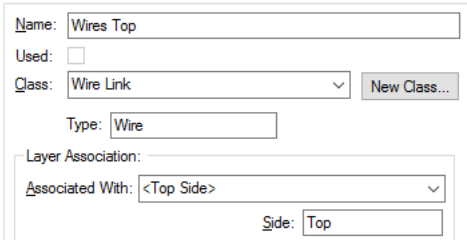


Layers

Wires require their own **Layer** for addition to the footprint or design, this will use the **Wires Layer Class** created.

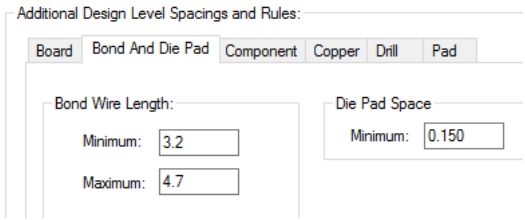
	Name	Associated Layer	Class	Side	Bias
Y		Wires Top	Wire Link	Top	None
		Silkscreen Top	Silkscreen	Top	None
Y	Top		Electrical	Top	X
		Solder Mask Top	Solder Mask	Top	None
		Paste Mask Top	Paste Mask	Top	None
		Pin Names	Non-Electrical	Top	None
	Ground		Power	Inner	Power Plane
	Power		Power	Inner	Power Plane
Y	Bottom		Electrical	Bottom	Y
		Silkscreen Bottom	Silkscreen	Bottom	None
		Solder Mask Bottom	Solder Mask	Bottom	None
		Paste Mask Bottom	Paste Mask	Bottom	None
Y		Wires Bottom	Wire Link	Bottom	None

This layer will be associated with either the <Top Side> or <Bottom Side>. The **Type:** must be **Wire** (defined in the **Layer Class**).



Design Rules

Specific rules exist for use with the Chip-On-Board feature and are used during **Online DRC** or batch **DRC**. You can define the **Minimum** and **Maximum Bond Wire Length** and the **Minimum Die Pad Space** within the **Design Level Rules** of the **Technology** dialog.



Minimum and Maximum Bond Wire Length

These rules are important to ensure the wires are not placed too close to the die and likewise, not too far away. They will be defined according to your manufacturing process or tolerances, or what is physically possible if manually adding wires to the design.

Minimum Die Pad Space

This allows you to override the **Pad to Pad** rule in the **Spacing Rules** dialog and defines the minimum distance between die pads.

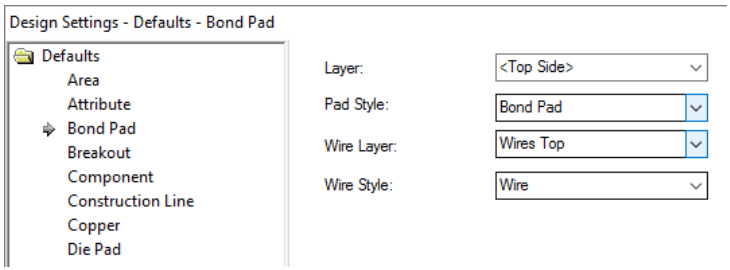
Wire Insulation Rule

The **insulation** property of the Wires can also be defined for each wire, please see below under *Default Design Settings*.

Default Design Setting

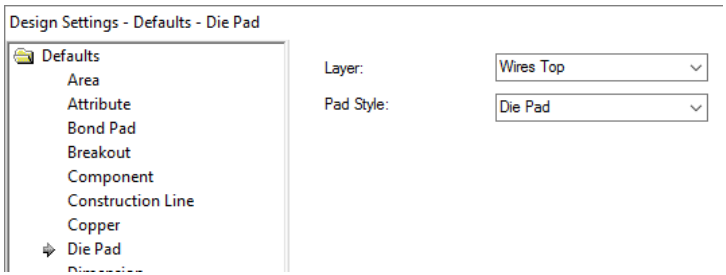
Bond Pads

Within the **footprint editor**, when creating a die with bond and die pads, the **Default** settings for the Chip-On-Board option are defined in the **Design Settings** under **Bond Pad and Die Pad**. There are two specific items to set up; **Bond Pads** and **Die Pads**.



Bond Pad allows you to define the default **Layer** that the bond pad will be added to during **Insert Bond Pad**, its **Pad Style**, **Wire Layer** and **Wire Style**.

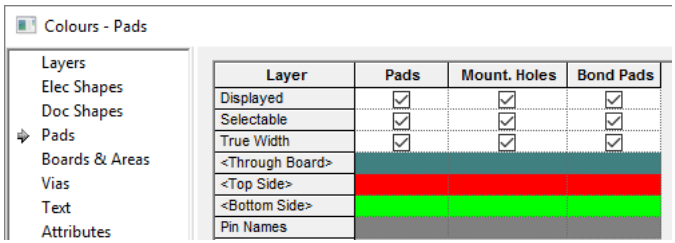
The **Wire Layer** and **Wire Style** are also used when using **Insert Bond Pad**. This option will request that the die pad is selected from which to connect to using the Wire (using this Wire Layer and Style).



Die Pad defines the **Layer** for the die pad and its **Pad Style** used during **Insert Die Pad**.

Colours for use with Chip-On-Board

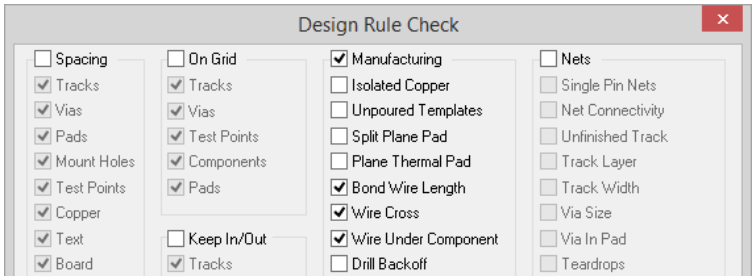
The **Colours** dialog shows items specific for component **Bond Pads** and **Wires**. **Component Bond Pads** are setup on the **Pads** page. You can access the colours dialog from the **Setup** menu.



Wires used for the Chip-On-Board option are displayed on the **Elec Shapes** page as **Comp Wire Links**.

Design Rules Checking Chip-On-Board Designs

The Pulsonix Chip-On-Board feature is provided with a set of design rules, which can be checked using the **on-line DRC** option and **Design Rules Checking** option.



Minimum and maximum **Bond Wire Length** of the bond wires between bond pads and die pads. These rules are defined in the **Technology File** under the **Spacing Rules** tab

Wire Cross, whether they are allowed to cross or not through the support of insulated or un-insulated (bond) wires. The **Wire Cross** check uses the **Insulated** property of a wire. The wire between the die and bond pads (wires are different to normal connections) can be defined **Insulated** or un-insulated. If wires are insulated and cross, no error is reported, if they are not insulated and cross, then an error is flagged.

Wires Under Components is not a Chip-On-Board specific option but is useful for ensuring that no wires have been placed under a component body.

Reporting Wire Positions

In addition to the supplied **Wires** report output (**wire.rff)** which reports the X and Y position of the pads attached to each end of the **Wire** and the **Net Name** of the wire, the **Report Maker** can also create a report for manual and automatic wire machines using the standard commands available and the format scripts.

Creating the Footprint

Adding Die Pads, Bond Pads and Wires

Unlike a normal component, using the Chip-On-Board feature, you can add pads which represent **Bond Pads** and **Die Pads**, connected together using a **Wire**. Other footprint detail such as the **Silkscreen**, **Component Placement Area** and **Body** are the same as normal components.

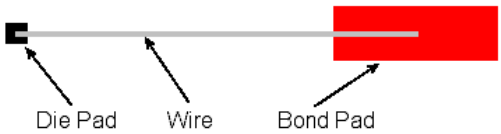
The **Insert Die Pad** and **Insert Bond Pad** options provide you with a mechanism for adding pads directly to the footprint with pre-assigned characteristics (taken from the **Design Settings** options). Die pads have same pad number as their attached Bond Pads (connected with a Wire).

Starting the Footprint creation process

The **Insert Die Pad** option will add a Die pad, Wire and then a Bond Pad to the footprint. **Insert Bond Pad** can also be used but it requires an existing Die pad to attach to (using a Wire).

You should start by using the **Insert Die Pad** option. This will add a die pad to a Wire layer. These pads sit 'above' or 'below' the top or bottom electrical layers but cannot be connected to by any other item such as connection or track, except for a Wire for connectively with the Bond pads.

On selection of the **Insert Die Pad** mode from the **Insert** menu or toolbar, you place the first Die pad which is automatically numbered, you are then given a connected Bond pad on the end of a wire to position.



If you decide to only place Die pads without their respective Bond pads then press the <ESC> button to cancel **Insert Bond Pad** and place the next Die pad. The Die pad number will be incremented to the next number. If you wish to exit completely you must click the ESC key again.

Insert Bond Pad can be used once die pads have already been added to the footprint. On selection of this mode, you are requested to select the die pad to 'pair' with the bond pad. Once selected, a Wire is added to the die pad and you can then place the bond pad. Bond pads cannot be 'converted' from any other type of pad (normal or die pads), they must be added as Bond pads.

You can 'convert' normal pads to die pad using the **Properties** dialog. To do this you must already have a suitable **Wire** layer defined (and **Wire Layer Class**), and a suitable **Pad Style**, although the pad is usually only very small. When the pad layer is changed from <Top>, <Bottom> or <Through-hole> to **Wire Top** or **Wire Bottom**, it is then converted into a **Die Pad**. This is really only used if an existing footprint is to be used as a die.

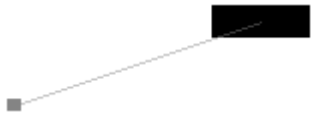
The Wire between the die and bond pads (wires are different to normal connections) can be defined as **Insulated** or un-insulated. This property is used for the **Wire Cross** check when using the **Design Rules Checking** option. If wires are insulated and cross, no error is reported, if they are not insulated and cross, then an error is flagged.

Bond Pad and Wire Alignment

While placing the bond pads you can elect to automatically rotate rectangular pads to be in-line with the Wire. The will be in-line or retain their original pad rotation during move.

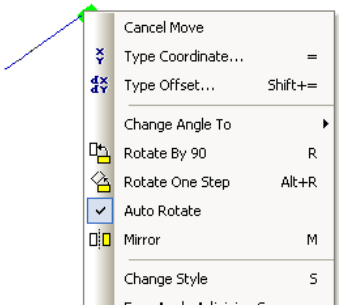
The two pictures below illustrate the effects of auto-rotation on bond pads:

With rotation applied



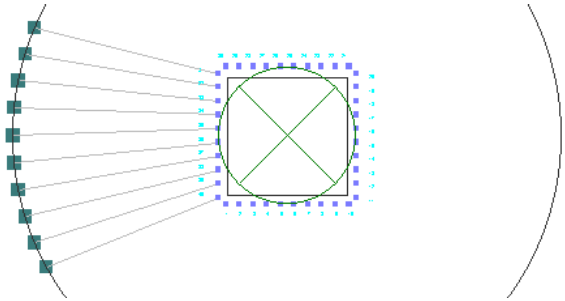
Without rotation applied

The **Auto Rotate** mode is switched on and off from the context menu and is available during **Move**.



Placing Bond Pads Around Shapes

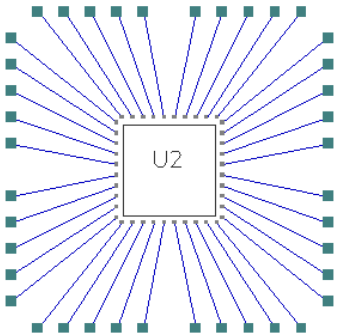
To aid the placement of Bond pads you can use the **Place Bond Pads** option, this is available on the **Tools** menu.



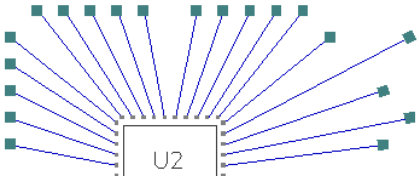
This option is used by selecting the Bond pads to place, then selecting the shape on which to place them around. The pads automatically snap to the shape but may need the placement grid to be corrected to fall exactly on the shape outline. You can use any shape but radial shapes provide the best results.

Adding Chip-On-Board Component to a PCB Design

Footprints for Chip-On-Board use containing Die and Bond pads are saved as normal, using **Save To Library** in the footprint editor. A Part is created in the normal way and the final Component added using the **Insert Component** option. Schematic symbols are also created as you would any standard component. You can only add components containing Die and Bond pads if you have the **Advanced Technology** product option.



Once in the PCB design, and provided you have the **Advanced Technology** product option, the components act differently. Bond pads have the ability to move or 'float' independently of the Die pads or normal pads of the component (Die pads and normal pads are fixed within the footprint).



When attaching connectivity in the design, you cannot connect to a Die pad directly; you can only connect to the Bond pad. This applies to both connections and tracks; they can only connect to Bond pads and not Die pads. However, the Die and Bond pads do have the same pad number.

Placing Bond Pads

The **Place Bond Pads** option (to place bond pads around a shape) is also available in the PCB Design editor but is only available as a command by default as it would normally be used in the footprint editor. If you wish to use this, you will have to use the **Run Command** option from the **Edit** menu and select **Place Bond Pads**, or use the **Customise** option and allocate a shortcut key or toolbar button to this option.

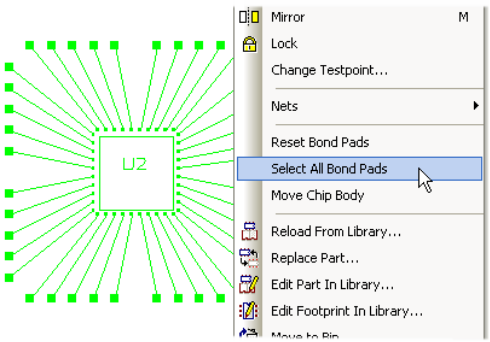
As with the footprint editor, finger pad shapes are supported with **automatic rotation offsetting** on shapes. Again this is available on the context menu while moving the bond pads.

Resetting Bond Pads

The option, **Reset Bond Pads** is available on the context menu for a selected component containing Die and Bond pads. This works on a whole selected component or individually selected Bond pads within a component. This will allow the position of any selected bond pads to be restored to their original position as defined in the footprint.

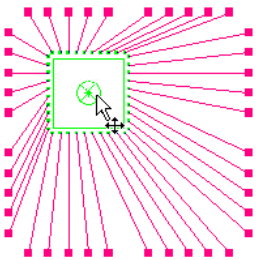
Selecting all Bond Pads on a Component

From the context menu for a selected component, you can use the **Select All Bond Pads** option to select all of the Bond pads. Once all the Bond pads have been selected, this could be used for changing their **Layer** or **Pad Style** for example. This option is only available as part of the Advanced Technology option.



Moving the Chip Body

Once your bond pads have been correctly positioned, you can move the Die independently to reposition the die body, (a Die is considered to be a collection of Die pads within a component). To do this use the **Move Chip Body** option from the context menu of a selected component, this will move the 'chip' body without moving any of the Bond pads. Again, this option is only available as part of the Advanced Technology option.



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