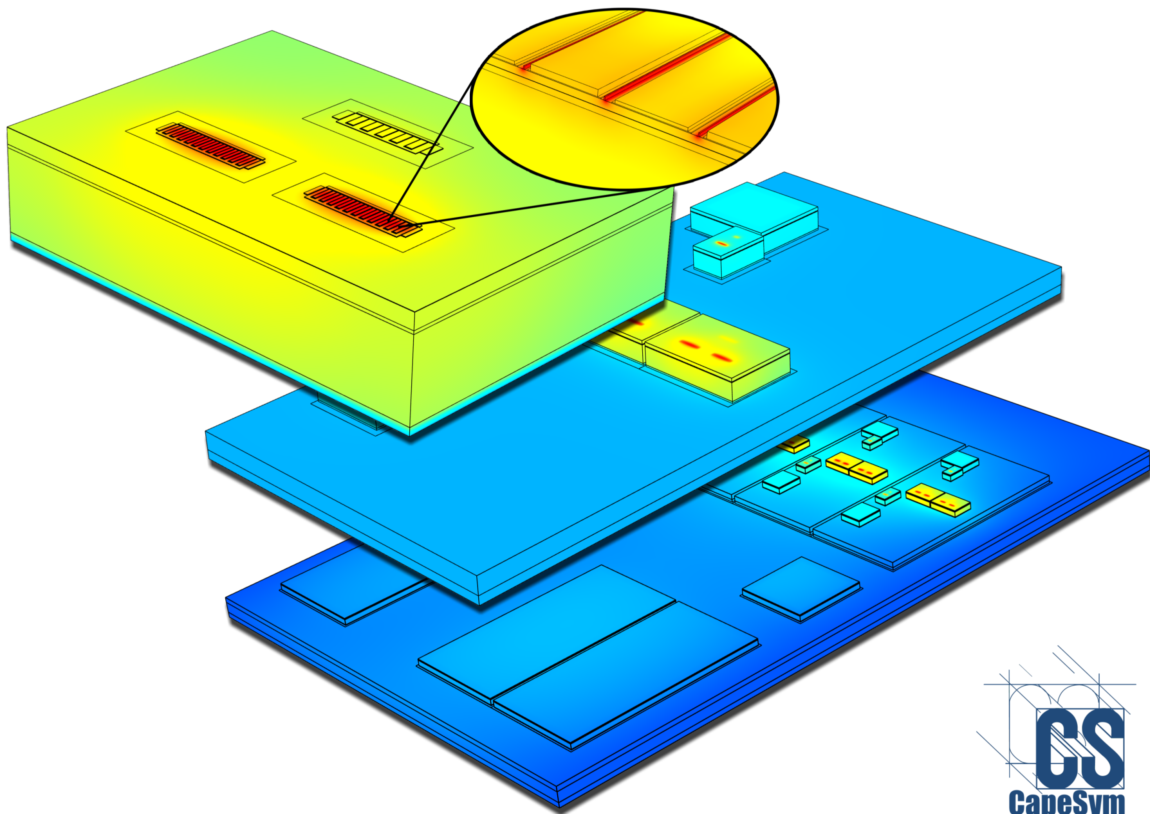
SYMMIC™ Application Note:

Using a FET Template for Thermal Analysis



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Using a FET Template for Thermal Analysis

The **Generic FET Template** provides a more complete thermal model of a field effect transistor than other approaches commonly used for thermal analysis. To demonstrate this, consider the analytical FET model of Darwish et. al. [1]. This model is based on analytical solutions of the heat equation for a FET with uniform gate-to-gate spacing and heating directly under the gate. Only flux in the substrate is considered, and thermal effects of backside layers, epi-layers, and metalization layers are ignored. Darwish et al. estimated thermal resistance and compared the calculated peak temperature with experiments and finite element simulations. A FET template can be reconfigured to quickly perform a higher fidelity thermal analysis.

Configuring the Template

Based on the analytical estimation of the maximum channel temperature under the gate, Darwish et al. compared their analysis to measurements made using liquid crystal techniques [2]. The parameters used for this comparison were:

- gate-to-gate spacing (26 µm)
- gate length (0.5 µm)
- gate width (37.5 µm)
- number of gates (10)
- substrate thickness (100 µm)
- base plate temperature (125 °C)
- power input (0.8 W/mm)

To set up a similar problem, begin with the parameter settings as configured in the default generic FET.xml template. To model a 10-gate FET, set the Number of Gates in the half-FET model to 5. To reduce the finger width, first change the Source Pad Via Width to 19 µm and the Source Via Width to 26 µm. Then in the *Finger/Channel/Gate...* list, set Finger Width to 37.5 µm. Just keep the default values for the rest of the Finger/Channel/Gate parameters because we will set the length of the heat generation segment independently of the gate length. (The channel length is much less significant than gate-to-gate spacing in determining the peak channel temperature in a FET.)

Set the gate-to-gate spacing by specifying the lengths of the sources and drains. In the *Source Lengths...* list, enter 21 µm for all accessible source lengths: the Default Source Length, Source 1 Length, Source 2 Length, and Source 3 Length. Since the default Gate-to-Source spacing is 2 µm and the default Gate Length is 1 µm, this gives a gate-to-gate distance across the source of 26 µm. Likewise, set all the applicable drain lengths in the *Drain Lengths...* list to 15 µm to give a gate-to-gate spacing of 26 µm across the drains. The parameters listed in red are not used in the model – red text indicates a parameter value that is fixed in the present configuration.

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In the theory, only a gallium arsenide (GaAs) substrate is used with no backside metal, solder, or adhesive. To simulate this, open the *Components...* list, and change the material for all layers below the substrate (Backside Adhesive, Metal Shim, Solder) to GaAs. Additionally, change the materials of all the epi-layers and all the vias to GaAs. This includes Epi-layer 1, Epi-layer 2, Epi-layer 3, Source Pad Via Hole, Source Pad Via Metal, Source Via Holes, Source Via Metal, and Source Via in Epi-layers 1-3. It may be helpful to y-slice through the center of the model to see that all via components are correctly filled-in with GaAs.

To produce an equivalent thickness of GaAs beneath the gates, use the *Thicknesses...* parameter list to set Substrate Thickness=84, Solder Thickness=5, Metal Shim Thickness=5, Backside Adhesive Thickness=5. Because these layers and the epi-layers are all now composed of GaAs, this gives a total thickness of 100 µm of GaAs between the power dissipation region and the bottom surface of the device.

The temperature-dependent GaAs conductivity used in the theory is given by:

$$k(T) = 56873\, T^{-1.23} \text{ W/m.K}$$

Open the *Materials...* list and set the material properties for GaAs, changing the thermal conductivities to 51.1e-6 W/µm.K at 300°K, 42.2e-6 W/µm.K at 350°K, 35.8e-6 W/µm.K at 400°K, and 31.1e-6 W/µm.K at 450°K. With the *Isotropic* box checked, only the k_x values need to be entered. Delete the rows for any entries that need to be eliminated. Click the *OK* button to save the material properties, then reopen the material properties dialog for GaAs to verify that the correct numbers were entered.

Set the total dissipated ON Power to 0.8 W/mm in the *Heat Generation...* parameter list. Since Darwish only considers a steady-state solution, only the ON Power is relevant. The default Backside Film Coefficient of 1 essentially holds the bottom surface at a fixed temperature, which we want to be 125°C in this case. So set the Backside Film Temperature to 398.15 K. To simulation heat dissipation in a 0.5µm-long area under the gate, set power Segment 1 Width to 0.5 µm and set Percent Power on Segment 1 to 100%. Set percent power on the other power segments to zero prior to setting segment 1.

Comparing to Analysis and Experiment

Run the simulation by selecting the first item of the Solve menu. This simulation takes less than 2 minutes on an AMD Opteron-based 64-bit system. After the simulation completes, the peak temperature over the device can be read from the temperature scale because the default settings cause the scale range to be set to the range of temperatures in the solution. Select *Temperature scale...* from the Results menu. To change the scale units from Kelvin to Celsius, click on the color scale to open the Temperature Scale Parameters dialog and select Celsius units.

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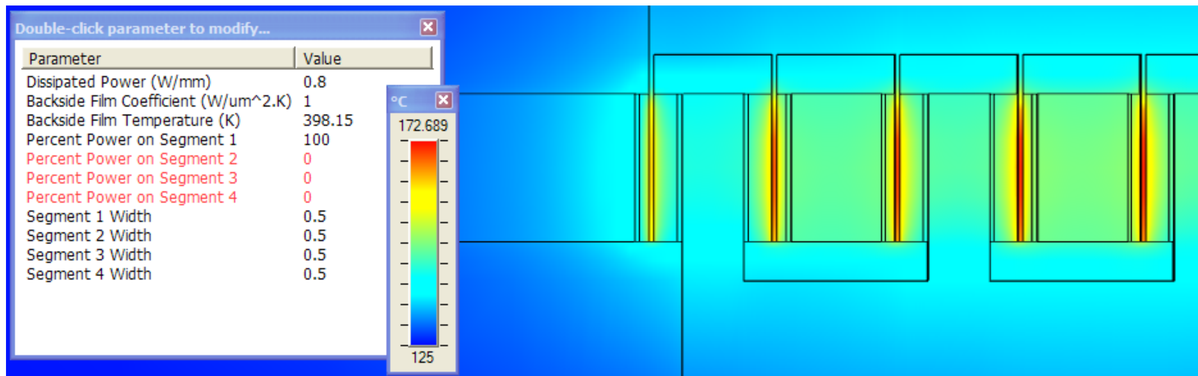
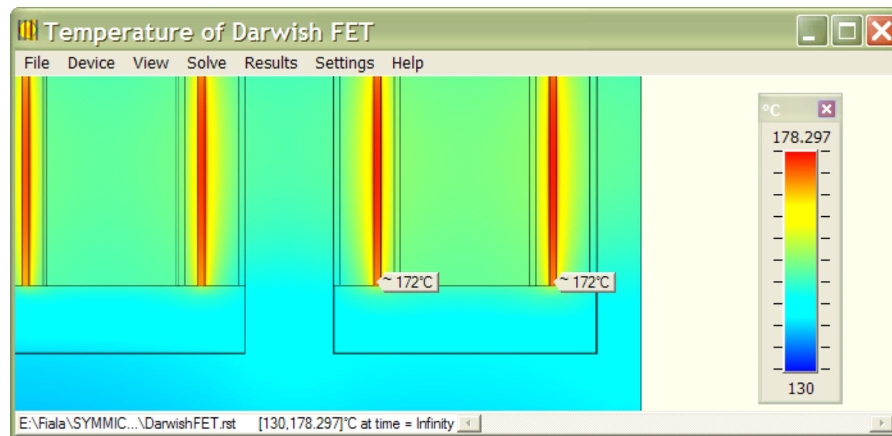


The Darwish et al. formula estimates the peak temperature to be 178°C for this configuration. As shown in the figure, SYMMIC calculates the peak temperature to be 172.6°C. To compare to the liquid crystal experimental results in [2], the base temperature must be raised to 130°C, in which case the peak temperature is raised to 178.3°C and the temperatures at the ends of the gates is 172°C, which matches the 172°C measured experimentally [2; Table 9].



Comparing Parameter Choices

The mesh automatically generated by SYMMIC for this analysis can be examined by selecting *Mesh lines* from the Settings menu. This option will display the meshes that underlie the colored temperature surfaces. SYMMIC generates an irregular mesh optimized to the geometrical features of the **Generic FET Template**. In the case of the simplified GaAs model, many of the features have been removed, but the mesh is still delineated along these features. The placement of mesh lines can be altered by shifting feature locations, as discussed in the next paragraph, but because the mesh is sufficiently refined this does not alter the temperature solution.

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The particular distribution of thicknesses chosen to get 100 µm of GaAs was not critical. An alternative set of thicknesses could have been chosen, such as Substrate Thickness=24, Solder Thickness=20, Metal Shim Thickness=30, Backside Adhesive Thickness=25. Since meshing of the layers below the substrate is very coarse by design, these thicknesses give more uniform meshing of the 100 µm GaAs block. The peak channel temperature is essentially unchanged when the simulation is rerun with these values. Increasing Mesh Refinement to 2 gave a mesh with almost 4 times as many nodes but only slightly altered the result (+0.3°C) .

Modeling Considerations

The **Generic FET Template** is designed to model a HEMT device better than thermal resistance models or other non-finite-element approaches, but the template may not be appropriate for all FET devices. Careful consideration should be made of the template's modeling assumptions. For example, the device template assumes the transistor has an even number of gates and that the device is symmetical about a central axis parallel to the gates. Such assumptions are properties of the template and not of SYMMIC; a different device template can specify a model with a different geometry.

Heat generation in the **Generic FET Template** is assumed to occur in a very thin region beneath the drain-side edge of the gate as expected for the quasi-2D electron gas of a HEMT. The peak temperature is affected by the distribution of power in the channel. Higher peak temperatures are obtained when all the power is dissipated in one narrow segment located far from the gate metal. Lower peak temperatures occur when power is spread in a wide region that straddles the edge of the gate. The small locus of heat generation results in a sharply-peaked temperature profile along the gate that is difficult to measure in a real device. A temperature peak that lies just to the drain side of the gate appears to be corroborated by micro-Raman spectroscopy [3], but these measurements are not effective where the gate metal is present. IR thermography also suggests a peak adjacent to the drain-side of the gate, but IR measurements have resolutions of only about 5 µm which significantly underestimates the peaks [4]. ***Because the resolution of the finite element mesh is designed to capture temperature peaks fully, the maximum temperature may be substantially higher than expected from measurements.***

The template includes the heat spreading effects of gate, source, and drain metal, but ignores the effects of interconnections between devices since these are not likely to be significant in most cases. Potential heat spreading effects of additional topside layers such as channel passivation are also ignored, but be aware that passivation layers of silicon nitride can often spread heat sufficiently to lower peak temperatures by 10%, depending on power distribution in the channel and the conductivities of other layers. The template also assumes that cooling is through the backside of the device and that there is no significant heat loss from the top surface through radiation or convection.

The above modeling assumptions may limit the applicability of the **Generic FET Template**, but a variety of other templates are available for modeling alternative device geometries, additional device components or boundary conditions, and different types of transistor technologies. Contact CapeSym, Inc. for details.

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References

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[2] J. Wright, B.W. Marks, K. D. Decker, "Modeling of MMIC devices for determining MMIC channel temperatures during life tests," in 7th IEEE Semiconductor Thermal Measurement, Modeling, and Management Symp., 1991, pp. 131–139.

[3] M. Kuball, A. Sarua, H. Ji, M.J. Uren, R.S. Balmer, T. Martin, "Integrated Raman - IR Thermography on AlGaN/GaN Transistors," Microwave Symposium Digest. 2006 IEEE MTT-S International. pp. 1339-42.

[4] SYMMIC Application Note: Simulations Versus IR Measurements. www.symmic.net

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