# Thermal Considerations in Low Cost T/R Module Design

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**Abstract:** *Commercial manufacturing technologies are being exploited to realize the transmit/receive module for a prototype multi-function phased array radar. This new manufacturing paradigm has the potential to significantly lower the cost of phased array systems. A critical question is the maximum total output power and duty cycle which can be achieved without expensive thermal packaging. To facilitate the evaluation of alternative designs for optimizing thermal performance, a parameterized finite element model of the T/R module was constructed. Thermal performance over a range of power levels and duty cycles was easily determined using SYMMIC, the template-based thermal simulator for monolithic microwave integrated circuits.*

**Keywords:** amplifier; GaAs; pHEMT; phased array radar

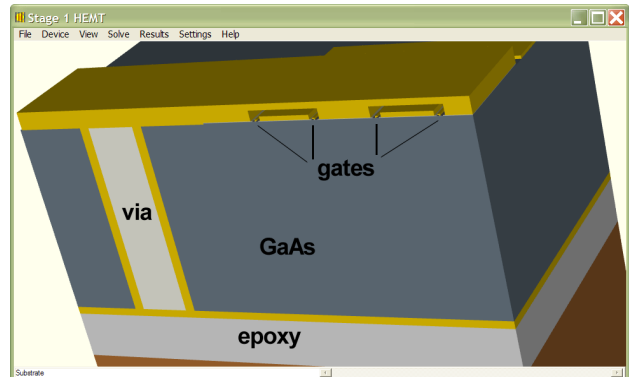## Introduction

Commercial technologies offering reduced manufacturing costs are being used for Transmit/Receive (T/R) module and Line Repeating Unit (LRU) prototypes for the FAA Multi-function Phased Array Radar (MPAR) system [1-2]. The T/R module provides for dual linear and circular polarization modes. The T/R module accomplishes this functionality with a custom set of multi-function gallium arsenide (GaAs) monolithic microwave integrated circuits, switches, and CMOS integrated circuits (ICs). High power amplifiers (HPAs), consisting of pseudomorphic high electron mobility transistors (pHEMTs), form the 8W output stage of the T/R module. All of the ICs are packaged in industry standard, power quad flat no-lead (PQFN) packages, and the module itself is fabricated on industry standard printed circuit board (PCB) technology. The PQFNs are surface mounted to the PCB with high volume, commercial pick and place techniques. A commercial off-the-shelf (COTS) pin-fin heat sink is attached to the backside of the T/R module with high thermal conductivity epoxy. This module approach establishes a new manufacturing paradigm offering the potential to significantly lower the manufacturing cost of phased array systems. This paper addresses the critical question of the maximum total output power and duty cycle which can be achieved with this manufacturing technology.

## Finite Element Modeling

Thermal analysis of microwave HPAs typically involves estimation of equivalent thermal resistances based on a simplified analysis [3-4], or finite difference calculations on a high resolution mesh [e.g. 5]. The disadvantage of the former approach is an inability to include details important to the accuracy of results, while the latter approach can be time-consuming and inflexible since the geometry and mesh must be built for each case considered.

To circumvent these problems, a detailed model of the MPAR T/R module was constructed using SYMMIC, the template-based thermal simulator for monolithic microwave integrated circuits [6]. SYMMIC facilitates rapid and accurate exploration of a design space via templates that parameterize the finite element analysis of transistors and circuits. SYMMIC's structured meshing is automatically generated and adaptive to geometry.
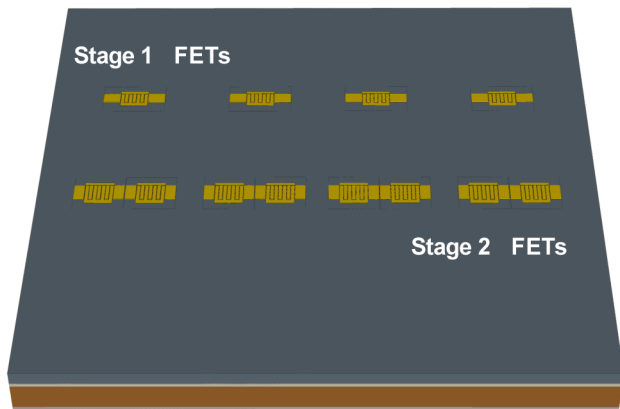


**Figure 1.** SYMMIC screenshot of the upper portion of the pHEMT device template that formed the basis of the high power amplifier MMIC thermal model.

Construction of a thermal model in SYMMIC begins with a device template for a pHEMT with parallel gates and source pad vias (Figure 1). For the field effect transistors (FETs) in the first stage of the HPA, the template was configured to represent half of the 8-gate device divided down the mid-line of symmetry. Gold-plated vias connect the topside metalizations through the GaAs substrate to the backside gold layer. Attachment to the C194 alloy slug of
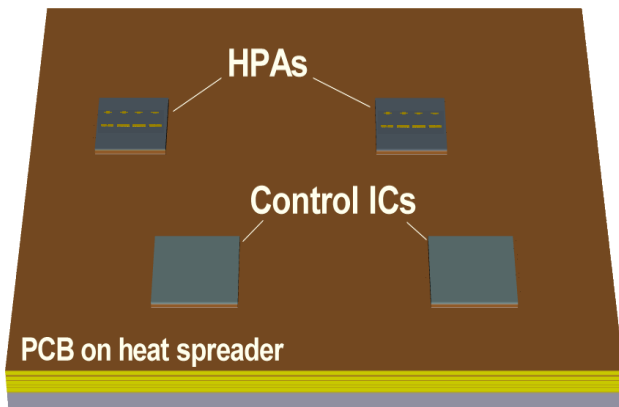
the chip frame was made by a layer of high thermal conductivity epoxy. The bottom layer of the device template described the Sn-Ag-Cu solder used to attach the chip to the PCB board. Adjustment of template parameters produced a second model for the stage 2 FETs, the main difference being that stage 2 FETs had finger widths of 150µm versus 100µm for stage 1.

Once templates are configured to match the devices, a layout is created which incorporates the FETs in the correct locations on the HPA (Figure 2). Each HPA had four stage 1 FETs and eight stage 2 FETs for 12.8mm of gate periphery in total.

Analysis of the HPA layout in SYMMIC will include the effect of FET adjacency on peak junction temperatures. However, accurate analysis depends on getting the correct boundary conditions for the location of the HPA in the T/R module. Placing the HPA layout in a model of the whole module is easily done in SYMMIC by "exporting" the HPA design onto a PCB template and creating a new layout combining the exported HPAs with the other ICs in the module (Figure 3).



**Figure 2.** The layout of field effect transistors that forms the parameterized model of a single high power amplifier in SYMMIC.



**Figure 3.** The layout of layouts that forms the parameterized model of the whole T/R module.

Building the finite element model in SYMMIC took minutes instead of days because it was only a matter changing parameters on the basic device templates and then creating the layouts. No time was spent specifying the mesh or loci of boundary conditions since these were already incorporated in the templates.

**Thermal Properties and Boundary Conditions**

To model the insulating effects of commercial plastic packaging, cooling is only assumed to occur through the bottom of the module where the COTS heat spreader is attached. Air moving at 10 ft³/min through this finned heat sink is used to cool the module. Assuming 50°C ambient air temperature as the worst-case scenario, the effective heat transfer coefficient was estimated to be 0.1 W/cm²°C at the bottom of the cold plate. When the cold plate is sized to the T/R module, this heat transfer rate corresponds to a thermal resistance of about 1 °C/W for the heat spreader.

To facilitate heat transfer from the ICs to the cold plate, thermally conductive vias are created by drilling an array of 256 holes through the PCB underneath each chip. The holes are plated with copper and filled with thermally conductive epoxy. PCB resin layers are low thermal conductivity Nelco Buried Capacitance epoxy, so the mixture of resin and filled holes gave an effective thermal conductivity of about 86 W/m°C in the through-PCB direction, but only 0.44 W/m°C in the lateral directions. Some of the metal layers of the PCB also were given orthotropic properties with higher through-PCB thermal conductivities than laterally, as determined by the density of traces within each layer.

Another important thermal property was the temperature-dependent thermal conductivity of GaAs, which was modeled as a function of temperature T by:
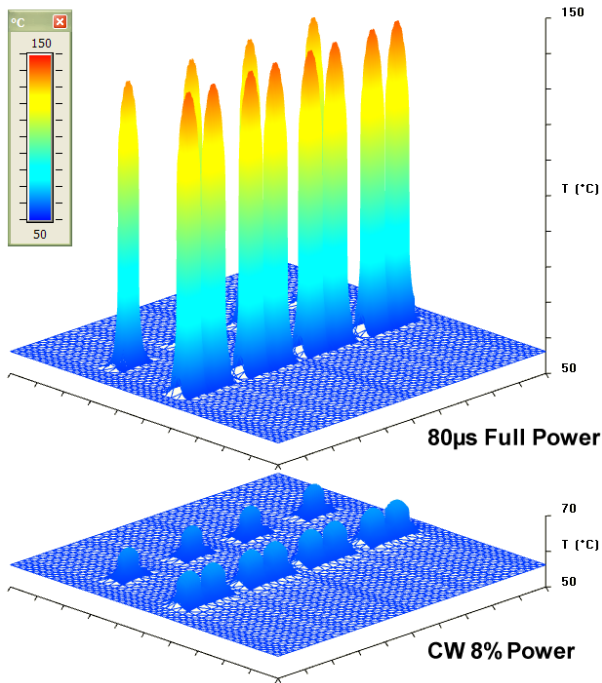
$$k_{GaAs} = 41.5(300/T)^{1.09} \text{ W/m°C}$$

**Simulating HPA Junction Temperatures**

To meet the peak junction temperature requirement of 150°C, a duty cycle is utilized and only one HPA is operated at a time. SYMMIC performs thermal analysis of on/off duty cycle transients, which is often difficult with other approaches. A steady-state analysis with reduced continuous power (CW) will not estimate duty cycle performance accurately. Applying full power even briefly results in much higher junction temperatures than expected from a pro rata CW analysis because the channel heats up very quickly (time constant < 10µs).

Boundary conditions on the bottom of the HPA, unlike the channel temperatures, could be extracted from T/R module CW analysis because the time constant on the PCB and cold plate was long (> 10ms) while the length of the duty cycle was short (1ms). Using the automatic coarsening operation in SYMMIC, the module layout was used to create a coarser-meshed device template and this was run at reduced power levels to simulate the long term effect of

duty cycle switching. This analysis showed that each HPA package reached a fairly uniform temperature except in the immediate vicinity of the FETs. This HPA temperature was used as the initial condition and fixed boundary condition for a transient simulation at full power on the HPA layout. The CW analysis also showed that the HPA nearest the edge would be hotter, so high-resolution analysis focused on this IC.

The HPA layout model included the full resolution mesh of each FET, with temperatures at over 2.7 million locations in total. The accuracy of SYMMIC's calculations has previously been calibrated against infrared and micro-Raman thermography [7-8], as well as compared to the calculations of other simulators [9]. High-resolution finite element models, as utilized by SYMMIC, reveal peak temperatures that are higher than measurements [10].
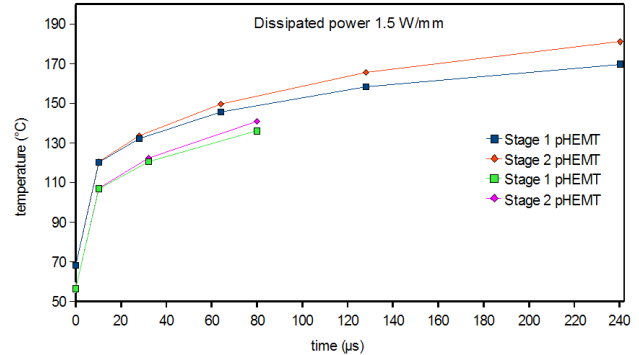


**Figure 4.** Plots of maximum temperatures over the HPA for transient (top) and CW (bottom) analyses of an 8% duty cycle of duration 1ms.
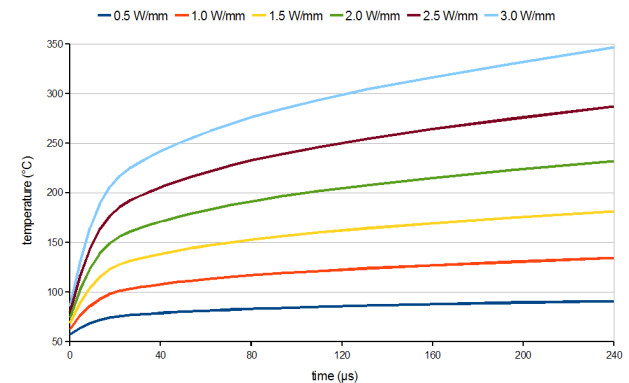
## Single HPA Operation

For an 8% duty cycle of 80µs on and 920µs off, and power dissipation of 1.5W/mm of gate periphery (19.2W total), the peak temperature in the HPA rose to 140.3°C (Figure 4). By comparison, pro rata CW analysis applying 8% power obtained a peak of only 65.8°C. Figure 5 shows the transient response during the on period for two different duty cycles. The stage 2 FETs get hotter than the stage 1 devices as expected for the increased finger width. There was no appreciable difference between FETs within a stage. At this power level, all FETs exhibit about a 50°C rise during the initial 10µs. Because the channel temperature rise is this fast, meeting temperature

requirements is critically dependent on the level of power dissipated during the on cycle (Figure 6).

A matrix of 36 cases involving different HPA power dissipation levels and different duty cycles was created in a spreadsheet and used as input parameters to the module-level pro rata CW analysis to determine the boundary condition on the backside of the HPA (Table 1). Table 2 shows the peak channel temperature in the HPA at the end of the first power pulse, starting from the uniform initial condition (also Table 1). This first peak was within 1% of the asymptotic value attained after several duty cycles.



**Figure 5.** Maximum FET channel temperatures in the HPA for duty cycles in which 1.5W/mm is dissipated for 80µs and 240µs (8% and 24% duty, respectively).



**Figure 6.** Maximum HPA channel temperatures for different power levels during the power pulse of a 24% duty cycle of duration 1ms.

**Table 1.** HPA backside boundary conditions (in °C).

| Duty Cyle | Dissipated Power (W/mm) | | | | | |
|---|---|---|---|---|---|---|
| | 0.5 | 1 | 1.5 | 2 | 2.5 | 3 |
| 4% | 51.1 | 52.0 | 52.9 | 53.9 | 54.8 | 55.7 |
| 8% | 52.3 | 54.2 | 56.0 | 57.9 | 59.7 | 61.6 |
| 12% | 53.5 | 56.3 | 59.1 | 61.9 | 64.7 | 67.5 |
| 16% | 54.7 | 58.5 | 62.2 | 65.9 | 69.6 | 73.4 |
| 20% | 56.0 | 60.6 | 65.3 | 69.9 | 74.6 | 79.2 |
| 24% | 57.2 | 62.8 | 68.4 | 73.9 | 79.5 | 85.1 |

**Table 2.** HPA peak channel temperatures (in °C).

| Duty Cyle | Dissipated Power (W/mm) | | | | | |
|---|---|---|---|---|---|---|
| | 0.5 | 1 | 1.5 | 2 | 2.5 | 3 |
| 4% | 72.9 | 96.9 | 122 | 149 | 177 | 207 |
| 8% | 78.4 | 108 | 140 | 174 | 210 | 248 |
| 12% | 82.4 | 117 | 153 | 192 | 234 | 279 |
| 16% | 85.7 | 123 | 164 | 208 | 254 | 305 |
| 20% | 88.5 | 129 | 173 | 220 | 272 | 326 |
| 24% | 91 | 134 | 181 | 232 | 287 | 346 |

### Evaluating Design Alternatives

The template-based approach does more than just facilitate thermal analysis of a particular module design. SYMMIC also aids rapid exploration of design alternatives. For example, the relative importance of the FET substrate vias to thermal performance can be assessed by changing materials to effectively remove them from the design. In the HPA, stage 2 FETs without vias attain peaks of 140.3°C at the end of an 80μs power cycle of 1.5W/mm, no different than the case when vias are present.

Given that substrate vias are thermally unimportant, can thermal performance be improved by using the via area between each pair of stage 2 FETs to increase the gate-to-gate spacing? Changing just ten parameter values in two templates sets up this thermal analysis, and reveals that the stage 2 channels would have a temperature rise 10% less than the previous HPA layout. At 1.5W/mm, 8% duty, the peak temperature in this alternative design occurs in stage 1 FETs (136°C) rather than stage 2 FETs (132°C).

In a similar way, SYMMIC makes it easy to assess the effects of other important design elements, such as the thickness or integrity of epoxy layers, or PCB vias. Replacing the orthotropic material of the PCB vias with Nelco resin makes the HPA 67°C hotter (than in Table 1 at 1.5W/mm, 8% duty), which clearly demonstrates the importance of PCB vias to thermal performance.

**Table 3.** Dual HPA peak temperatures (in °C).

| Duty Cyle | Dissipated Power (W/mm) | | | | | |
|---|---|---|---|---|---|---|
| | 0.5 | 1 | 1.5 | 2 | 2.5 | 3 |
| 4% | 73.1 | 97.4 | 123 | 150 | 179 | 209 |
| 8% | 78.9 | 109 | 142 | 176 | 212 | 251 |
| 12% | 83.1 | 118 | 155 | 195 | 238 | 283 |
| 16% | 86.6 | 125 | 167 | 211 | 259 | 310 |
| 20% | 89.7 | 131 | 176 | 225 | 277 | 333 |
| 24% | 92.4 | 137 | 185 | 238 | 294 | 355 |

### Dual HPA Operation

Operation of both HPAs simultaneously was evaluated by repeating the pro rata CW analysis for the T/R module with all four ICs fully powered during the on period of the duty cycle. The HPA boundary conditions obtained from this analysis were then applied to the channel temperature rise calculated by the high-resolution, transient HPA analysis. The results given in Table 3 are for the hotter HPA; the other HPA was consistently cooler but by less than 1% of the peak temperature rise.

### Conclusions

The MPAR T/R module design continues to evolve at M/A-COM, but commercial manufacturing and packaging technologies will meet performance requirements at very modest production costs. The use of advanced thermal analysis software such as SYMMIC now makes it feasible to ensure that thermal requirements are met while optimizing power performance. A very detailed thermal analysis can be performed in a reasonable amount of time with minimal effort.

### References

1. Benner, W., G. Torok, M. Batista-Carver, and T. Lee, "MPAR Program Overview and Status," *23rd Conf. Interact. Info. Proc.Sys. for Meteorol., Oceanog., & Hydrol.*, San Antonio, TX, AMS paper 7.1, 2009.

2. Carlson, D. J., "Making MPAR a Reality," *National Symposium on Multifunction Phased Array Radar*, Norman, OK, Oct. 2007. www.ofcm.gov/mpar-symposium/presentations2007.htm

3. Cooke, H.F., "Precise Technique Finds FET Thermal Resistance," *Microwaves RF* **25**(8):85-87, 1986.

4. Darwish, A.M., A. J. Bayba, H. A. Hung, "Accurate Determination of Thermal Resistance of FETs," *IEEE Trans. Microwave Theory Tech.* **53(**1):306-313, 2005.

5. Florian, C., Cignani, R., Vannini, G., Comparini, M.C. "A Ku band monolithic power amplifier for TT&C applications," *2005 Euro. Microwave Conf.*, Vol. 3(4-6) Oct. 2005.

6. SYMMIC™, www.symmic.net

7. Fiala, J. C., "Simulations versus IR Measurements," SYMMIC Application Note. www.capesym.com/SYMMIC/IRmeasurements.pdf

8. Fiala, J. C., "Simulations versus μRaman Spectroscopy," SYMMIC Application Note. www.capesym.com/SYMMIC/microRaman.pdf

9. Fiala, J. C., "Comparing SYMMIC to ANSYS and TAS," SYMMIC Application Note. www.capesym.com/SYMMIC/comparingSolvers.pdf

10. Green, D. S., et al. "GaN HEMT thermal behavior and implications for reliability testing and analysis," *Phys. Stat. Sol. C* **5**(6):2026-2029, 2008.