

BTA26
Triac Series

TOP 3

Absolute maximum ratings

| Parameter | Symbol | Value | Unit | Test condition |
|--|--------------------|-------------|------------|----------------------------|
| peak repetitive off-stage voltage | V_{DRM}, V_{RRM} | 600 | V | $I_D=0.1mA, I_R=0.1mA$ |
| on-state RMS current | $I_T(RMS)$ | 25 | A | all conduction angles |
| NON repetitive surge peak on-state current | I_{TSM} | 250 | A | $T_p=10ms, T_j=25^\circ C$ |
| critical rate of rise on-state current | di/dt | 50 | A/ μs | $I_{TM}=20A, I_G=50mA$ |
| peak gate current | I_{GM} | 4 | A | $t_p=20\mu s$ |
| average gate power dissipation | $P_G(AV)$ | 1 | W | |
| storage temperature range | T_{stg} | -40 to +150 | $^\circ C$ | |
| operating junction temperature range | T_j | 125 | $^\circ C$ | |

Electrical characteristics ($T_j=25^\circ C$) unless otherwise specified

| Parameter | Symbol | Value | Unit | Test condition |
|---|-------------|-------------|--------------|--------------------------------|
| gate trigger current | I_{GT} | ≤ 50 | mA | T2+G+ $V_D=12V, I_T=0.1A$ |
| | | ≤ 50 | mA | T2+G- $V_D=12V, I_T=0.1A$ |
| | | ≤ 50 | mA | T2-G- $V_D=12V, I_T=0.1A$ |
| | | ≤ 100 | mA | T2-G+ $V_D=12V, I_T=0.1A$ |
| gate trigger voltage | V_{GT} | ≤ 1.30 | V | $V_D=12V, I_T=0.1A$ |
| hold current | I_H | ≤ 50 | mA | $V_D=12V, I_T=0.1A$ |
| critical rate of rise off-state voltage | dv/dt | ≥ 200 | V/ μs | $V_D=67\%V_{DRM}$ |
| on-state voltage | V_{TM} | ≤ 1.55 | V | $I_T=35A$ |
| off-state leakage current | I_{DRM} | ≤ 3.00 | mA | $V_D=V_{DRM}; T_j=125^\circ C$ |
| thermal resistance | Rth(j-a) | 50 | $^\circ C/W$ | |
| | Rth(j-c) AC | 1.20 | | Insulated |

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damage resulting from such sale(s).

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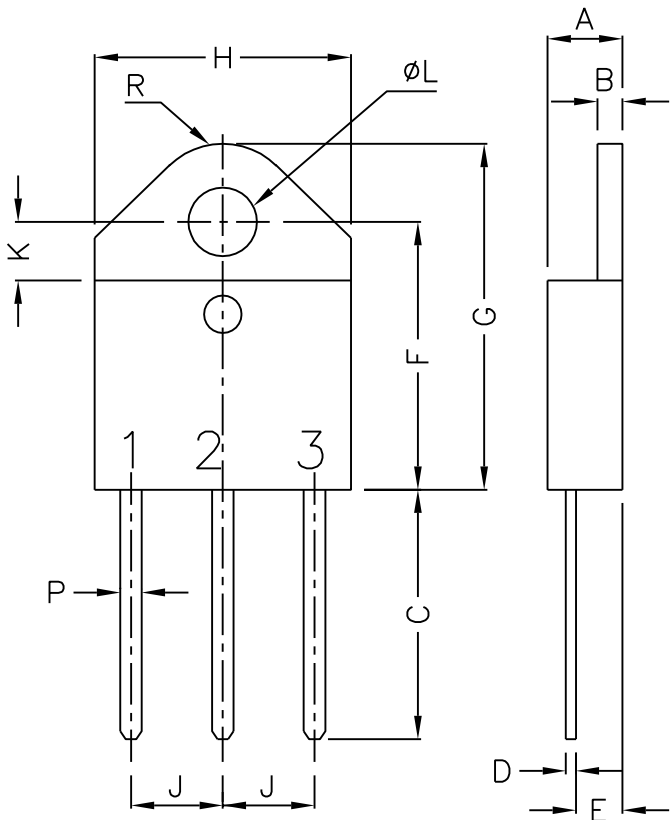
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Continental Device India Limited

C-120 Naraina Industrial Area, New Delhi 110 028, India.

Telephone + 91-11-2579 6150, 4141 1112 Fax + 91-11-2579 5290, 4141 1119

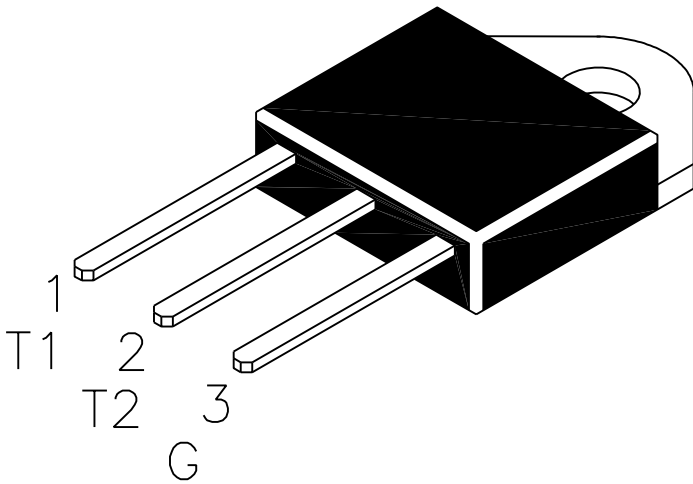
email@cdil.com www.cdilsemi.com

PACKAGE TO-P3



| DIM | MIN | TYP. | MAX |
|-----|-------|------|-------|
| A | 4.40 | | 4.60 |
| B | 1.45 | | 1.55 |
| C | 14.35 | | 15.60 |
| D | 0.50 | | 0.70 |
| E | 2.70 | | 2.90 |
| F | 15.80 | | 16.50 |
| G | 20.40 | | 21.10 |
| H | 15.10 | | 15.50 |
| J | 5.40 | | 5.65 |
| K | 3.40 | | 3.65 |
| L | 4.08 | | 4.17 |
| P | 1.20 | | 1.40 |
| R | | 4.60 | |

ALL DIMENSIONS ARE IN mm



PIN CONFIGURATION

1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE