UHF Narrow band radio transceiver
STD-302N-R 447MHz

Operation Guide

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302N-R is a high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. A narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302N-R 447MHz, a narrowband module with 12.5 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

Features

- 10 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time
- High sensitivity -120 dBm
- Excellent mechanical durability, high vibration & shock resistance
- EU RoHS compliance

Applications

- Telemetry

  Water level monitor for rivers, dams, etc.
  Monitoring systems for environmental data such as temperature, humidity, etc.
  Transmission of measurement data (pressure, revolution, current, etc) to PC
  Security alarm monitoring

- Telecontrol

  Industrial remote control systems
  Remote control systems for factory automation machines
  Control of various driving motors

- Data transmission

  RS232/RS485 serial data transmission

SPECIFICATIONS

STD-302N-R 447 MHz

* The MIN/TYP/MAX values for the RF output power and BER are specified in the range of operation environment temperature.
* All values in the Specification column are specified at 25 ºC+/-10 ºC unless otherwise noted.

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Communication method		One way, Half-duplex			
Emission class		F1D			
Operating frequency range	MHz	447.275		447.9875	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Aging rate (/ year)	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance *	ppm	-1.5		1.5	TX freq., RX Lo freq. At delivery
Dimensions	mm	30 x 50 x 9 mm			Not including protrusion
Weight	g	25 g			

* Initial frequency tolerance: At delivery
Initial frequency tolerance is defined as frequency drift at delivery within 1 year after the final adjustment

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type		PLL controlled VCO			
Frequency stability (-20 to 60°C)	ppm	-4		4	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		12.5		
Data rate	bps	2400		4800	DO/DI
Max. pulse width	ms		15	20	DO/DI
Min. pulse width	us	200			DO/DI
Data polarity		Positive			DI vs DO
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		46	50	Vcc = 3.0 V
RX consumption current	mA		26	30	Vcc = 3.0 V

For PLL interface, refer to the documents of MB15E03SLP and use it within the specification.

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power	mW		10		Conducted 50 Ω 447.6 MHz
Deviation	kHz	+/- 1.8	+/- 2.2	+/- 2.5	PN9 4800 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.17		DI=L, LPF=20 kHz
Spurious emission	dBm		- 37		Conducted 50Ω
Adjacent CH power	dB	40			PN9 4800 bps
Occupied freq. bandwidth	kHz			8.5	PN9 4800 bps

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type		Double superheterodyne			
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits) *1	dBm	-107	-115		PN 9 4800bps
BER (1 % error) *2	dBm		-120		PN 9 4800bps
Sensitivity 12dB/ SINAD	dBm		-120		fm1 k/ dev 2 kHz CCITT
Spurious response rejections*3	dB		55		1 st Mix, 2 signal method, 1 % error
			50		2 nd Mix, 2 signal method, 1 % error
Adjacent CH selectivity *3	dB		45		+/- 12.5 kHz, 2 signal method, 1 % error
Blocking	dB		75		Jamming signal +/- 1MHz 2 signal method, 1% error
Intermodulation *4	dB		50		2 signal method, 1 % error
DO output level	V	0		2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 25 kHz (from PLL setup)
			50	70	When power ON (from PLL setup)
Time until valid Data-out *5	ms		50	100	CH shift of 25 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation (1st Lo)	dBm		-60	-54	Conducted 50 Ω
RSSI	mV	300	350	400	With -97 dBm at 447.6 MHz
		190	240	290	With -113 dBm at 447.6 MHz

Specifications are subject to change without prior notice

Notice

- Communication range depends on the operation environment and ambient surrounding
- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection.
- RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the pattern used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to the wide GND pattern to avoid any change in characteristics.

Notes about the specification values

*1 BER: RF level where no error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*2 BER (1 % error): RF level where 1% error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*3 Spurious response, CH selectivity: Jamming signal used in the measurement is unmodulated.
*4 Intermodulation: Ratio between the receiver input level with BER 1% and the signal level (PN9 4800 bps) added at the points of 'Receiving frequency - 200 kHz ' + ' Receiving frequency -100kHz' with which BER 1% is achieved.
*5 Time until valid Data-out: Valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 4800bps, 1010 repeated signal.

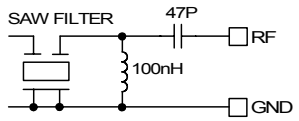
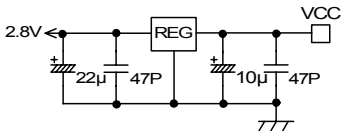
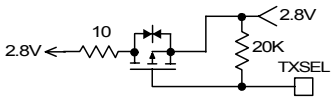
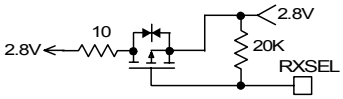
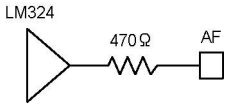
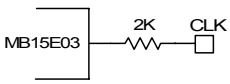
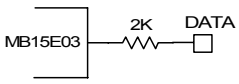
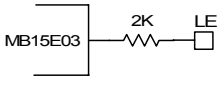
Conditions:

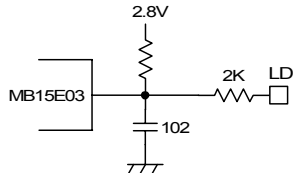
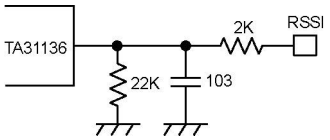
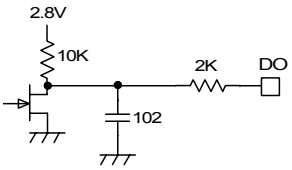
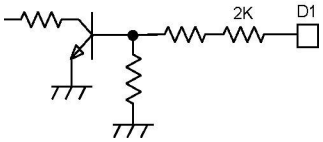
All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

Measuring equipment:

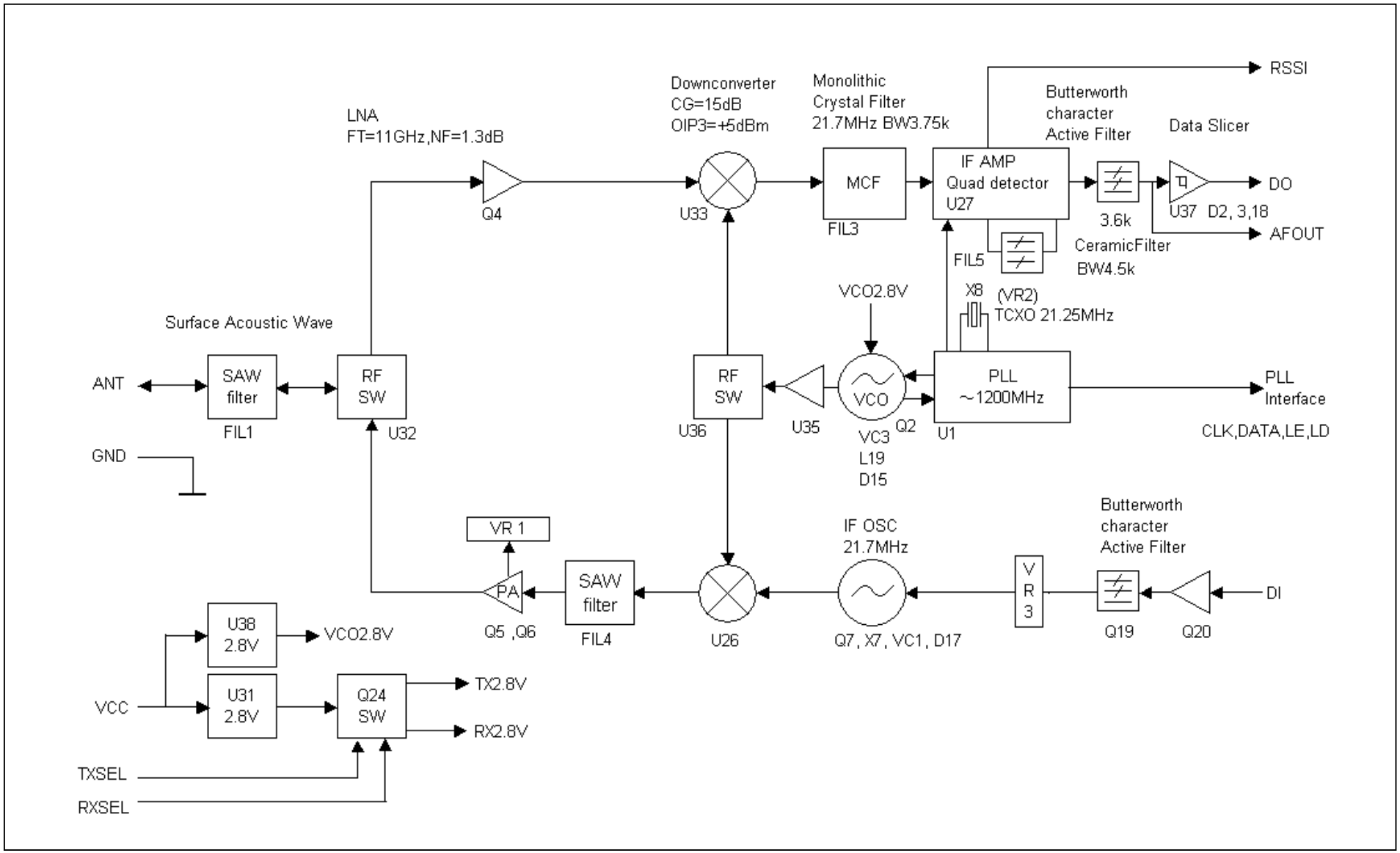
SG=ANRITSU communication analyzer MT2605
Spectrum analyzer = ANRITSU MS2663G, BER measure = ANRITSU MP1201G

PIN DESCRIPTION

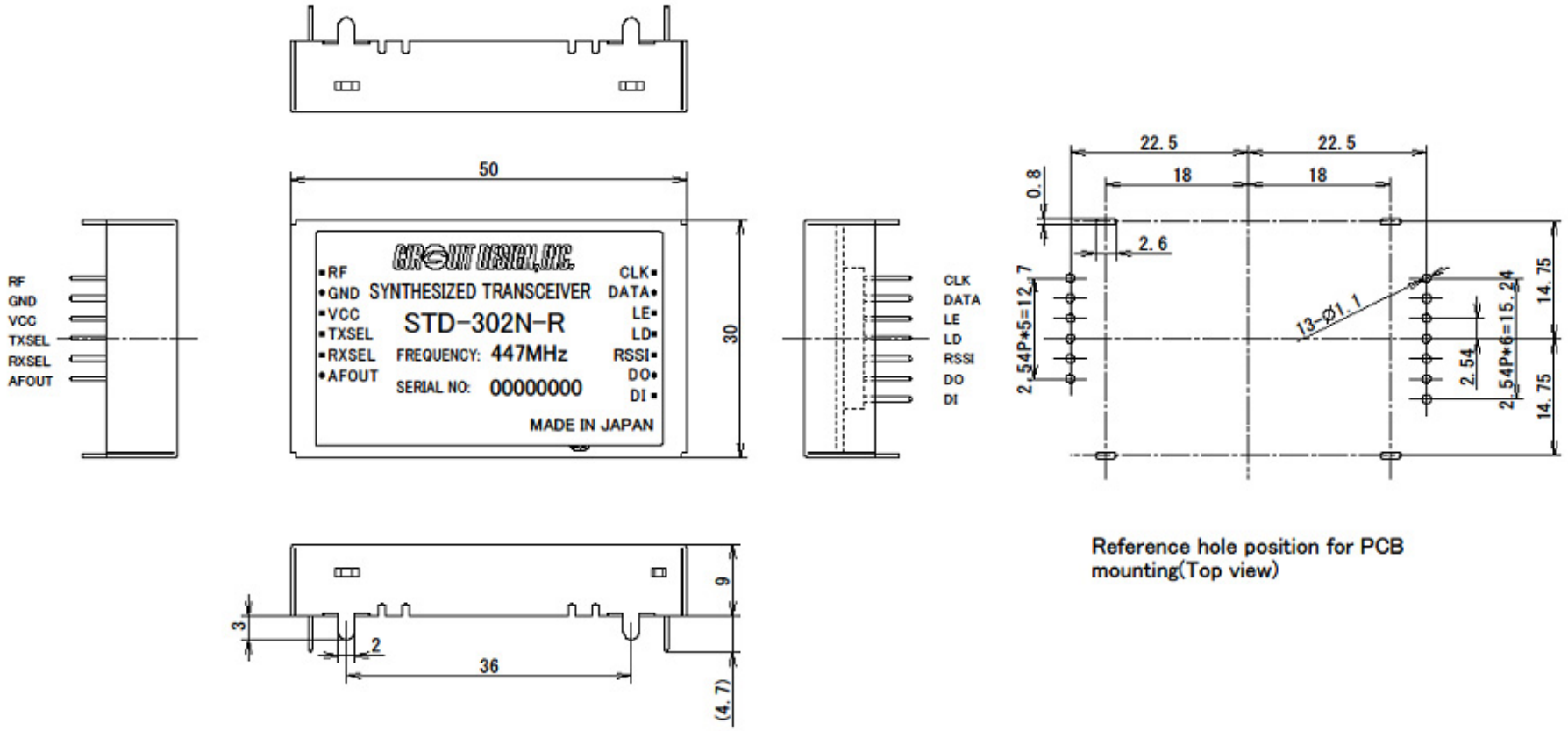
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 **Ω**	
GND	I	GROUND terminal The GND pins and the feet of the shield case shoud be connected to the wide GND pattern.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AF	O	Analogue output terminal There is DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
LE	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

LD	O	PLL lock/unlock monitor terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min.208 µs Max. 20 ms	

BLOCK DIAGRAM <STD-302N-R 447 MHz>



DIMENSIONS

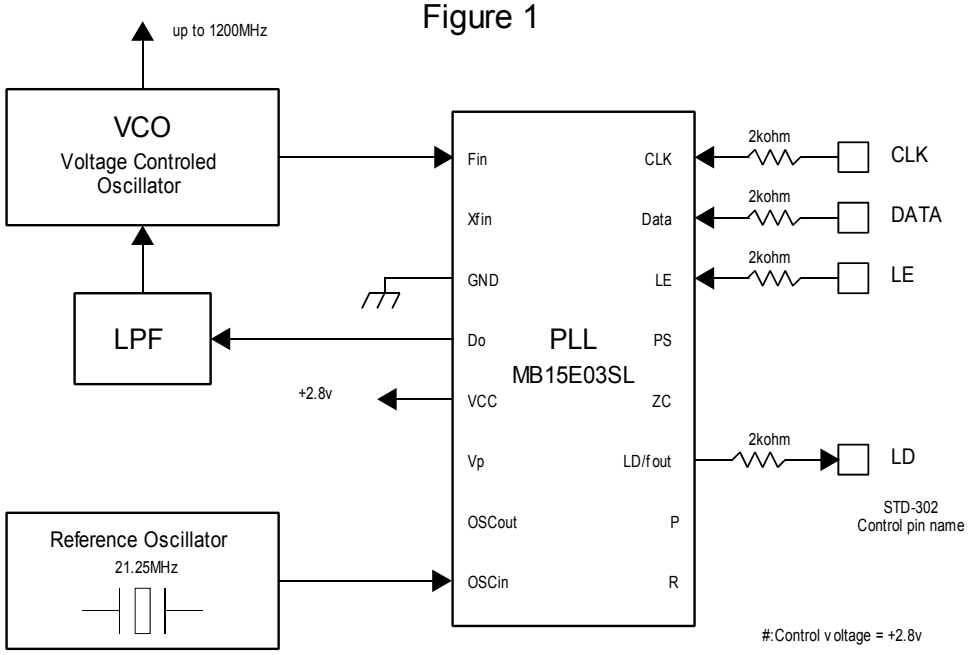


Reference hole position for PCB mounting(Top view)

PLL IC CONTROL

- **PLL IC control**

Figure 1



STD-302N-R is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302N-R has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302N-R has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302N-R is 2.8 V, so the control voltage must be the same.
STD-302N-R comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302N-R. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

- **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.

$f_{vco} = [(M \times N)+A] \times f_{osc} / R$ -- Equation 1

f_{vco} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$ $A<N$))
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302N-R, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch}. Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.

$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency $f_{vco.}$ This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302N-R uses 21.25 MHz for the reference clock $f_{osc.}$ f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where “n” is the number for division.

$f_{vco}=n*f_{comp}$ ---- Equation 3 $n = f_{vco}/f_{comp}$ ---- Equation 4 note: $f_{comp} = f_{osc}/R$

Also, this PLL IC operates with the following R, N, A and M relational expressions.

$R=f_{osc}/f_{comp}$ ---- Equation 5 N = INT (n / M) ---- Equation 6 A = n - (M x N) ---- Equation 7
INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 869.725 MHz can be calculated as below.
The constant values depend on the electronic circuits of STD-302N-R.

Conditions: Channel center frequency: f_{ch} = 869.725 MHz
Constant: Offset frequency: f_{offset}=21.7 MHz
Constant: Reference frequency: f_{osc}=21.25 MHz
Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M

The frequency of VCO will be

$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 869.725 –21.7 = 848.025MHz

Dividing value “n” is derived from Equation 4

$n = f_{vco} / f_{comp}$ = 848.025MHz/25kHz = 33921

Value “R” of the reference counter is derived from Equation 5.

$R = f_{osc}/f_{comp}$ = 21.25MHz/25kHz = 850

Value “N” of the programmable counter is derived from Equation 6.

N = INT (n/M) = INT(33921/64) = 530

Value “A“ of the swallow counter is derived from Equation 7.

A = n – (M x N) = 33921 – 64 x 530 = 1

The frequency of STD-302N-R is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.
Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.cdt21.com/).

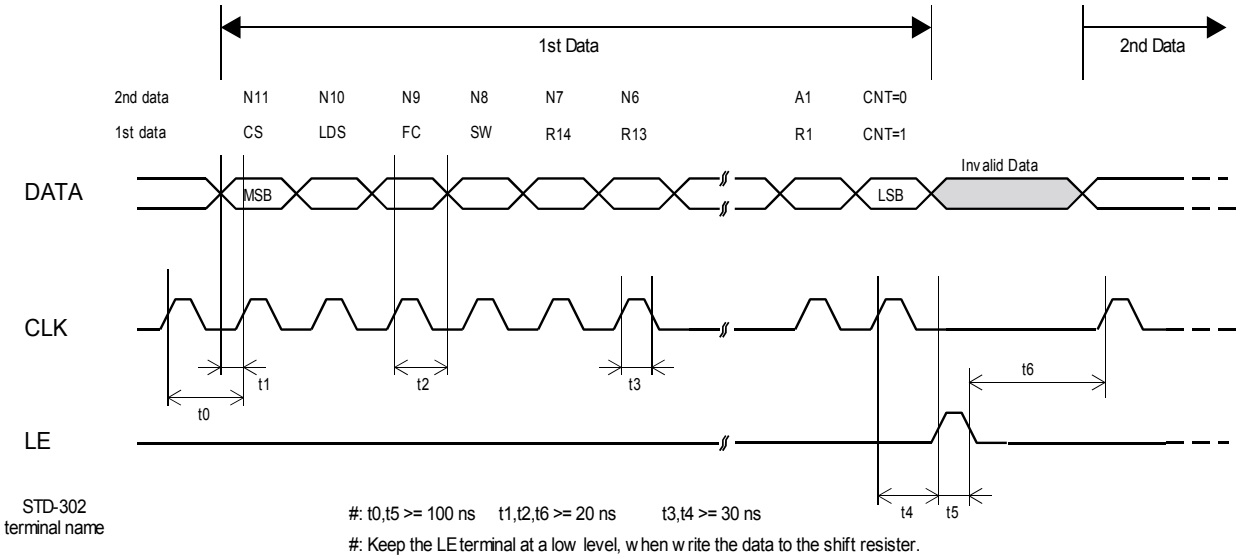
The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

- **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

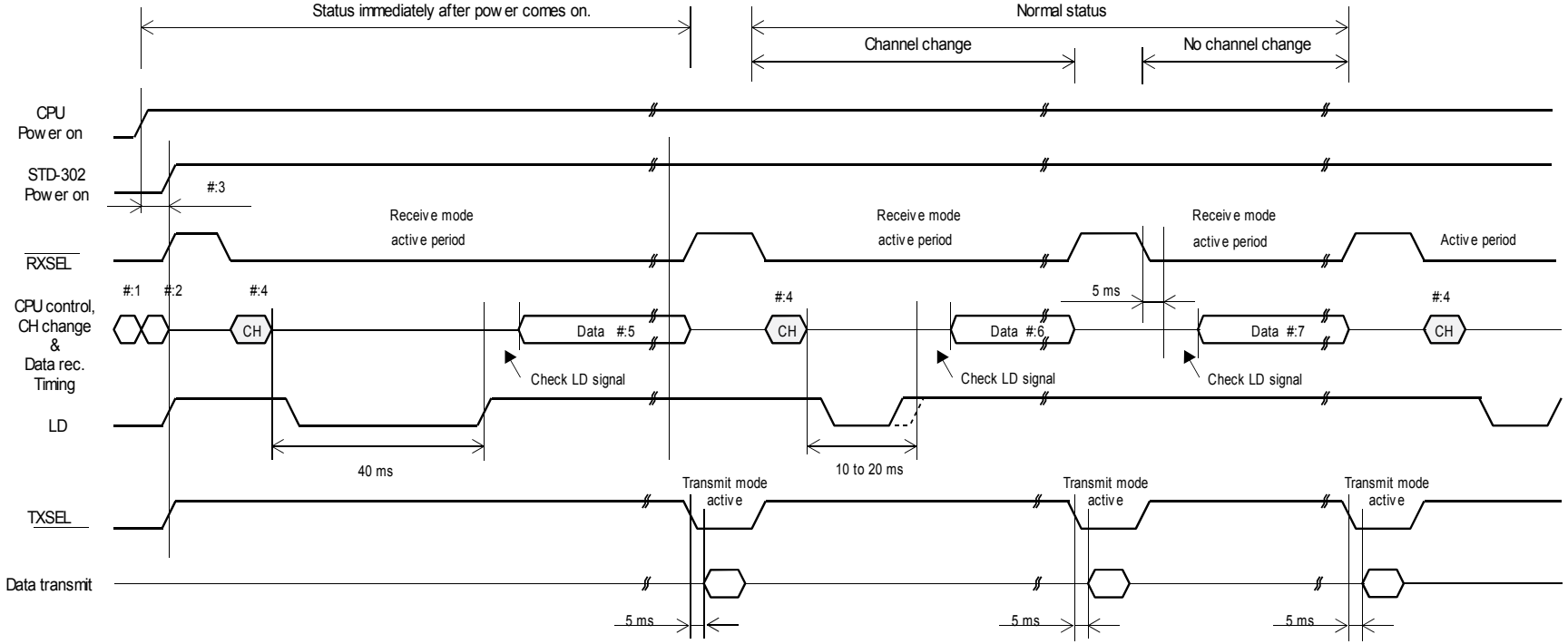
If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[*1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[*2].
Check that the Lock Detect signal is “high” 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[*1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is urged to verify operation at low temperature and optimize the timing.

[*2] Sending ‘10101…..’ preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver.
For 4800 bps, a preamble of ‘11001100’ is effective.
Recommended preamble length: 20 ms

Remark
For details about PLL control and the sample programs, see our technical document ‘STD-302 interface method’

Figure 3: Timing diagram for STD-302



#:1 Reset control CPU
#:2 Initialize the port connected to the module.
#:3 Supply power to the module after initializing CPU.
#:4 RFchannel change must be performed in receiving mode.

#:5 40 ms later, the receiver can receive the data after changing the channel..
#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.
#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

447 MHz ISM band (447.275 – 447.9875 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	12.5
Start Channel Frequency F_{ch} [MHz]	447.2750
Channel Step Frequency [kHz]	12.5
Number of Channel	58
Prescaler M	64

: For data input
: Result of calculation
: Fixed value

Parameter name	Value
Reference Frequency F_{osc} [MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

Parameter name	Value
Reference Counter R	1700
Programmable Counter N Min. Value	531
Programmable Counter N Max. Value	532
Swallow Counter A Min. Value	0
Swallow Counter A Max. Value	63

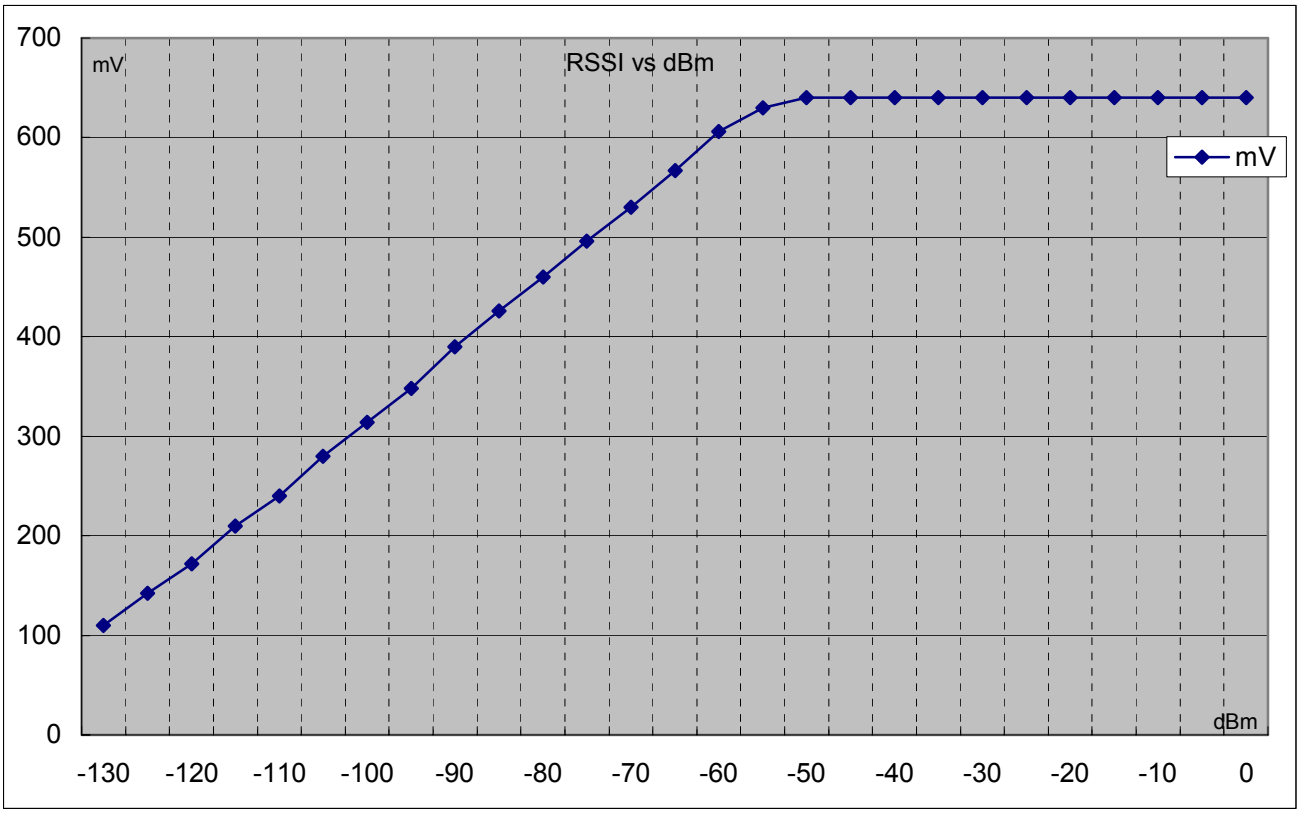
No.	Channel Frequency FCH (MHz)	Expect Frequency FEXPECT (MHz)	Lock Frequency FVCO (MHz)	Number of Division n	Programmable Counter N	Swallow Counter A
0	447.2750	425.5750	425.5750	34046	531	62
1	447.2875	425.5875	425.5875	34047	531	63
2	447.3000	425.6000	425.6000	34048	532	0
3	447.3125	425.6125	425.6125	34049	532	1
4	447.3250	425.6250	425.6250	34050	532	2
5	447.3375	425.6375	425.6375	34051	532	3
6	447.3500	425.6500	425.6500	34052	532	4
7	447.3625	425.6625	425.6625	34053	532	5
8	447.3750	425.6750	425.6750	34054	532	6
9	447.3875	425.6875	425.6875	34055	532	7
10	447.4000	425.7000	425.7000	34056	532	8
11	447.4125	425.7125	425.7125	34057	532	9
12	447.4250	425.7250	425.7250	34058	532	10
13	447.4375	425.7375	425.7375	34059	532	11
14	447.4500	425.7500	425.7500	34060	532	12
15	447.4625	425.7625	425.7625	34061	532	13
16	447.4750	425.7750	425.7750	34062	532	14
17	447.4875	425.7875	425.7875	34063	532	15
18	447.5000	425.8000	425.8000	34064	532	16
19	447.5125	425.8125	425.8125	34065	532	17
20	447.5250	425.8250	425.8250	34066	532	18
21	447.5375	425.8375	425.8375	34067	532	19
22	447.5500	425.8500	425.8500	34068	532	20
23	447.5625	425.8625	425.8625	34069	532	21
24	447.5750	425.8750	425.8750	34070	532	22
25	447.5875	425.8875	425.8875	34071	532	23
26	447.6000	425.9000	425.9000	34072	532	24
27	447.6125	425.9125	425.9125	34073	532	25
28	447.6250	425.9250	425.9250	34074	532	26
29	447.6375	425.9375	425.9375	34075	532	27
30	447.6500	425.9500	425.9500	34076	532	28
31	447.6625	425.9625	425.9625	34077	532	29
32	447.6750	425.9750	425.9750	34078	532	30

33	447.6875	425.9875	425.9875	34079	532	31
34	447.7000	426.0000	426.0000	34080	532	32
35	447.7125	426.0125	426.0125	34081	532	33
36	447.7250	426.0250	426.0250	34082	532	34
37	447.7375	426.0375	426.0375	34083	532	35
38	447.7500	426.0500	426.0500	34084	532	36
39	447.7625	426.0625	426.0625	34085	532	37
40	447.7750	426.0750	426.0750	34086	532	38
41	447.7875	426.0875	426.0875	34087	532	39
42	447.8000	426.1000	426.1000	34088	532	40
43	447.8125	426.1125	426.1125	34089	532	41
44	447.8250	426.1250	426.1250	34090	532	42
45	447.8375	426.1375	426.1375	34091	532	43
46	447.8500	426.1500	426.1500	34092	532	44
47	447.8625	426.1625	426.1625	34093	532	45
48	447.8750	426.1750	426.1750	34094	532	46
49	447.8875	426.1875	426.1875	34095	532	47
50	447.9000	426.2000	426.2000	34096	532	48
51	447.9125	426.2125	426.2125	34097	532	49
52	447.9250	426.2250	426.2250	34098	532	50
53	447.9375	426.2375	426.2375	34099	532	51
54	447.9500	426.2500	426.2500	34100	532	52
55	447.9625	426.2625	426.2625	34101	532	53
56	447.9750	426.2750	426.2750	34102	532	54
57	447.9875	426.2875	426.2875	34103	532	55

TEST DATA

RSSI typical output level characteristic
Measurement frequency: 447.6 MHz

25 ºC +/- 5 ºC



Sig (dBm)	RSSI (mV)
-130	110
-125	142
-120	172
-115	210
-110	240
-105	280
-100	314
-95	348
-90	390
-85	426
-80	460
-75	496
-70	530
-65	567

Sig (dBm)	RSSI (mV)
-60	606
-55	630
-50	640
-45	640
-40	640
-35	640
-30	640
-25	640
-20	640
-15	640
-10	640
-5	640
0	640

Measurement is done with the PLL setting control board prepared by Circuit Design.

Regulatory compliance information

Compliance

STD-302N-R 447 MHz was designed to be installed in radio equipment for use in Korea. The technical specifications referred to in the design phase are shown below:

Frequency	447.8625 - 447.9875 MHz
Channel spacing	12.5 kHz
Frequency type	F(G)1D, F(G)2D
Radio output	≤ 10 mW
Occupied band width	≤ 8.5 kHz

The relevant laws and regulations are subject to change.

Compliance assessment

This product was designed to meet the specification above, however it has not been assessed for conformity with the appropriate regulations. Users are required to verify that their final product meets the appropriate specifications and to perform the procedures for regulatory compliance.

Guarantee of regulatory compliance

We only guarantee that this product meets the specification in this document. We are exempt from any other responsibilities relating to regulatory compliance.

We also recommend that the user consults the authorities in the relevant country for detailed regulatory information such as valid regulations, test specifications, assessment procedures, marking methods etc, before starting any project with this product.
If technical documentation is required for compliance assessments, we will provide any documents, which may be considered necessary for assessment, under NDA. The documentation is only available in English.

Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take a part or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

Revision history

Version	Date	Description	Remark
1.0	Apr. 2008	STD-302N-R 447 MHz The first issue	