UHF Narrow band radio transceiver

STD-302S 429 MHz

Operation Guide

Version 1.2 (Oct. 2015)

- This product requires electrical and radio knowledge for setup and operation.
- To ensure proper and safe operation, please read this operation guide thoroughly prior to use.
- Please keep this operation guide for future reference.

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302S is a high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. The narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302S 429 MHz, a narrowband module with 12.5 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

This product is designed to meet the basic specifications of Japanese ARIB STD-T67 standard, however it has not been certified for conformity with the technical regulations. Users are required to perform the procedures for certification with their final products after installing this product in their systems.

Features

- 10 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time
- High sensitivity -120 dBm
- Excellent mechanical durability, high vibration & shock resistance
- ARIB STD-T67 compliant

Applications

- Telemetry

  Water level monitor for rivers, dams, etc.
  Monitoring systems for environmental data such as temperature, humidity, etc.
  Transmission of measurement data (pressure, rpm, current, etc) to PC
  Security alarm monitoring
- Telecontrol

  Industrial remote control systems
  Remote control systems for factory automation machines
  Control of various driving motors
- Data transmission

  RS232/RS485 serial data transmission

SPECIFICATIONS

STD-302S 434 MHz

All ratings at 25 +/-10 °C unless otherwise noted

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Communication method		Simplex, Half-duplex			
Emission class		F1D			
Operating frequency range	MHz	429.25		429.7375	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Frequency drift / year	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance	ppm	-1.5		1.5	TX freq., RX Lo freq.
Dimensions	mm	30 x 50 x 9 mm			Not including antenna
Weight	g	25 g			

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type		PLL controlled VCO			
Frequency stability (-20 to 60°C)	ppm	-4		4	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		12.5		
Data rate	bps	2400		4800	DO/DI
Max. pulse width	ms		15	20	DO/DI
Min. pulse width	us	200			DO/DI
Data polarity		Positive			DO/DI
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		44	48	Vcc = 3.0 V
RX consumption current	mA		26	30	Vcc = 3.0 V

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power	mW	5	9	12	Conducted 50 Ω, 429.5 MHz
Deviation	kHz	±1.7	±2.0	±2.3	PN9 4800 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.17		DI=L, LPF=20 kHz
Spurious emission	dBm		-37	-27	Conducted 50 Ω
Adjacent CH power	dB	40			PN9 4800 bps
Occupied freq. bandwidth	kHz			8.5	PN9 4800 bps

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type		Double superheterodyne			
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits) *1	dBm	-108	-115		PN 9 4800bps
BER (1 % error) *2	dBm		-120		PN 9 4800bps
Sensitivity 12dB/ SINAD	dBm		-120		fm1 k/ dev 2kHz CCITT
Spurious response rejection *3	dB		70		1 st Mix, 2 signal method, 1 % error
			55		2 nd Mix, 2 signal method, 1 % error
Adjacent CH selectivity *3	dB		50		+/- 12.5kHz, 2 signal method, 1 % error
Intermodulation *4	dB		50		2 signal method, 1 % error
DO output level	V	0		2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 12.5 kHz (from PLL setup)
			50	70	When power ON (from PLL setup)
Time until valid Data-out *5	ms		50	100	CH shift of 12.5 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation	dBm		-60	-54	Conducted 50 ohm
RSSI	mV	300	350	400	With -97 dBm at 429.5 MHz
		190	240	290	With -113 dBm at 429.5 MHz

Specifications are subject to change without prior notice

Notice

- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection.
- RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the trace used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to a wide GND pattern to avoid any change in characteristics.

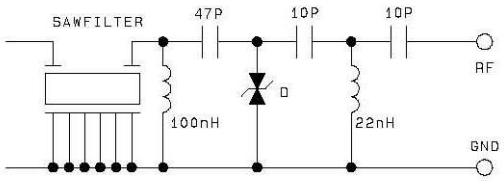
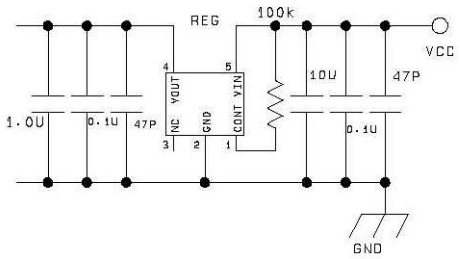
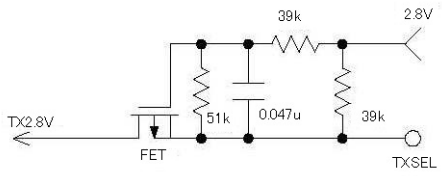
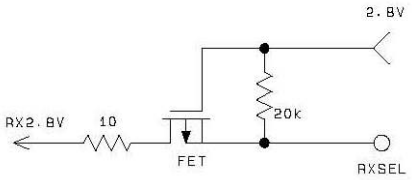
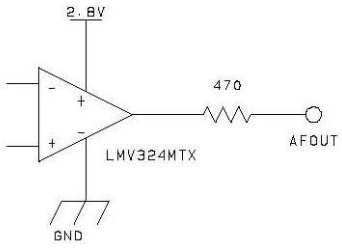
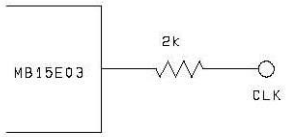
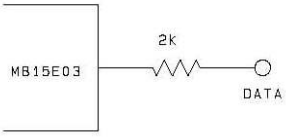
Notes about the specification values

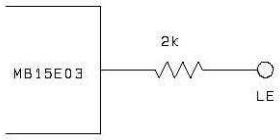
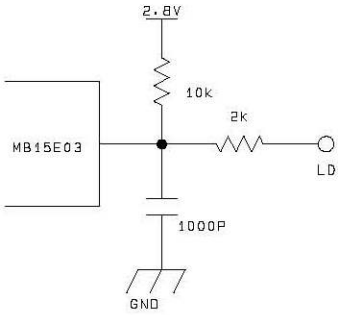
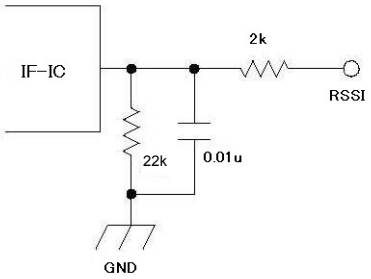
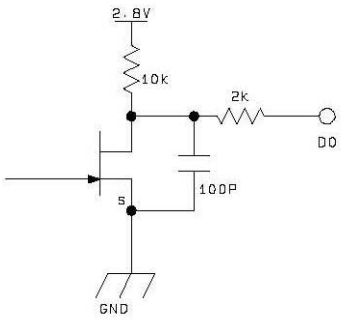
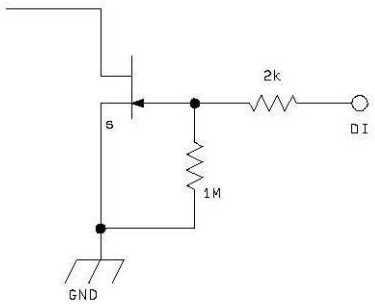
*1 BER: RF level where no error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*2 BER (1 % error) : RF level where 1% error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*3 Spurious response, CH selectivity: Jamming signal used in the measurement is unmodulated.
*4 Intermodulation: Ratio between the receiver input level with BER 1% and the signal level (PN9 4800 bps) added at the points of 'Receiving frequency - 200 kHz ' + ' Receiving frequency -100kHz' with which BER 1% is achieved.
*5 Time until valid Data-out : Valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 4800bps, 1010repeated signal.

All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

Measuring equipment:
SG=ANRITUS communication analyzer MT8802
Spectrum analyzer = ANRITSU MS2830A
BER measure = ANRITSU MP1201G

PIN DESCRIPTION

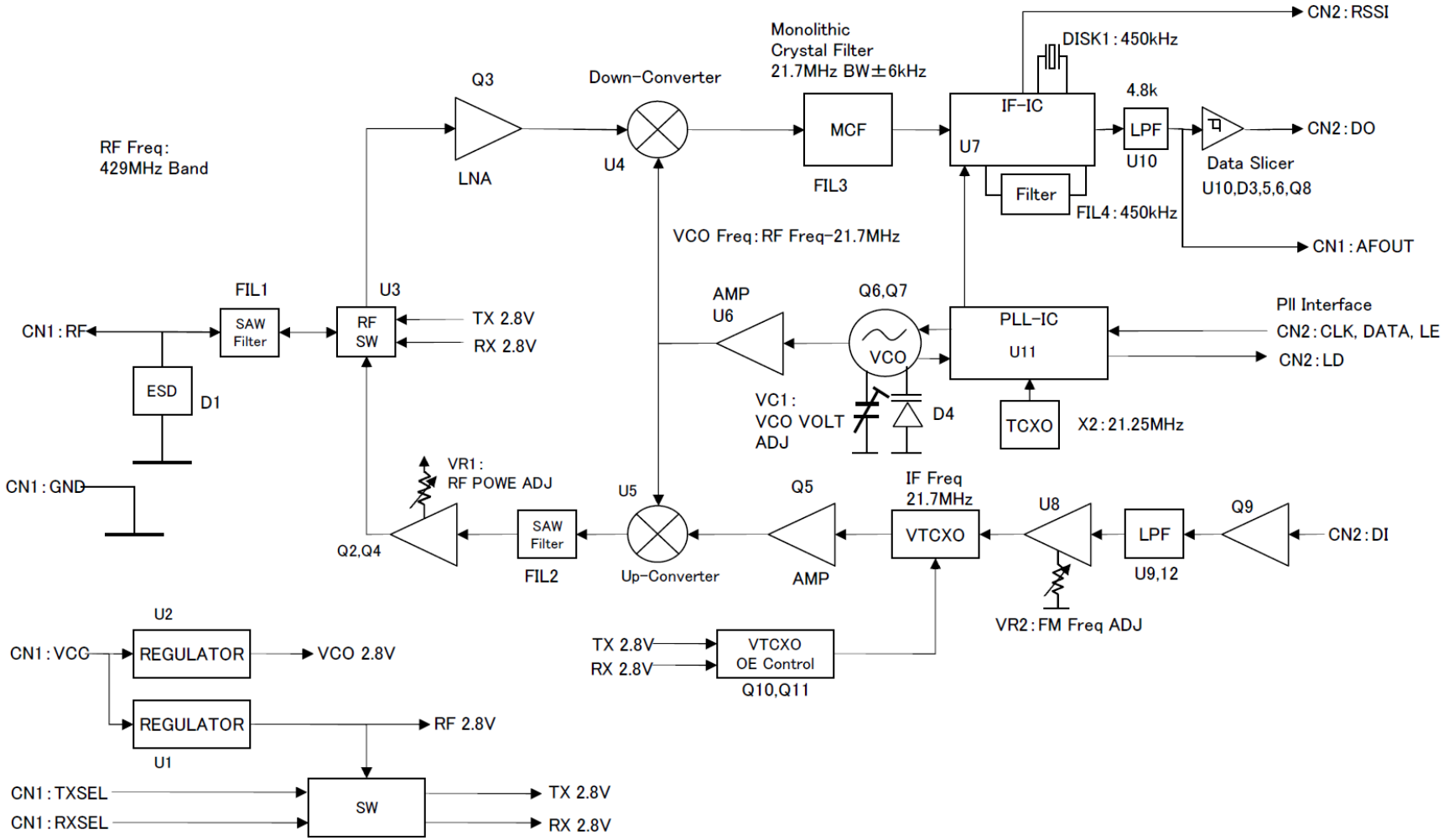
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 **Ω**	
GND	I	GROUND terminal The GND pins and the feet of the shield case should be connected to a wide GND plane.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AFOUT	O	Analogue output terminal There is a DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	Clock terminal fof PLL data setting input Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

LE	I	Load enable signal input terminal for PLL data setting input Interface voltage H = 2.8 V, L = 0 V	
LD	O	PLL lock/unlock indicator terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min.200 µs Max. 20 ms	

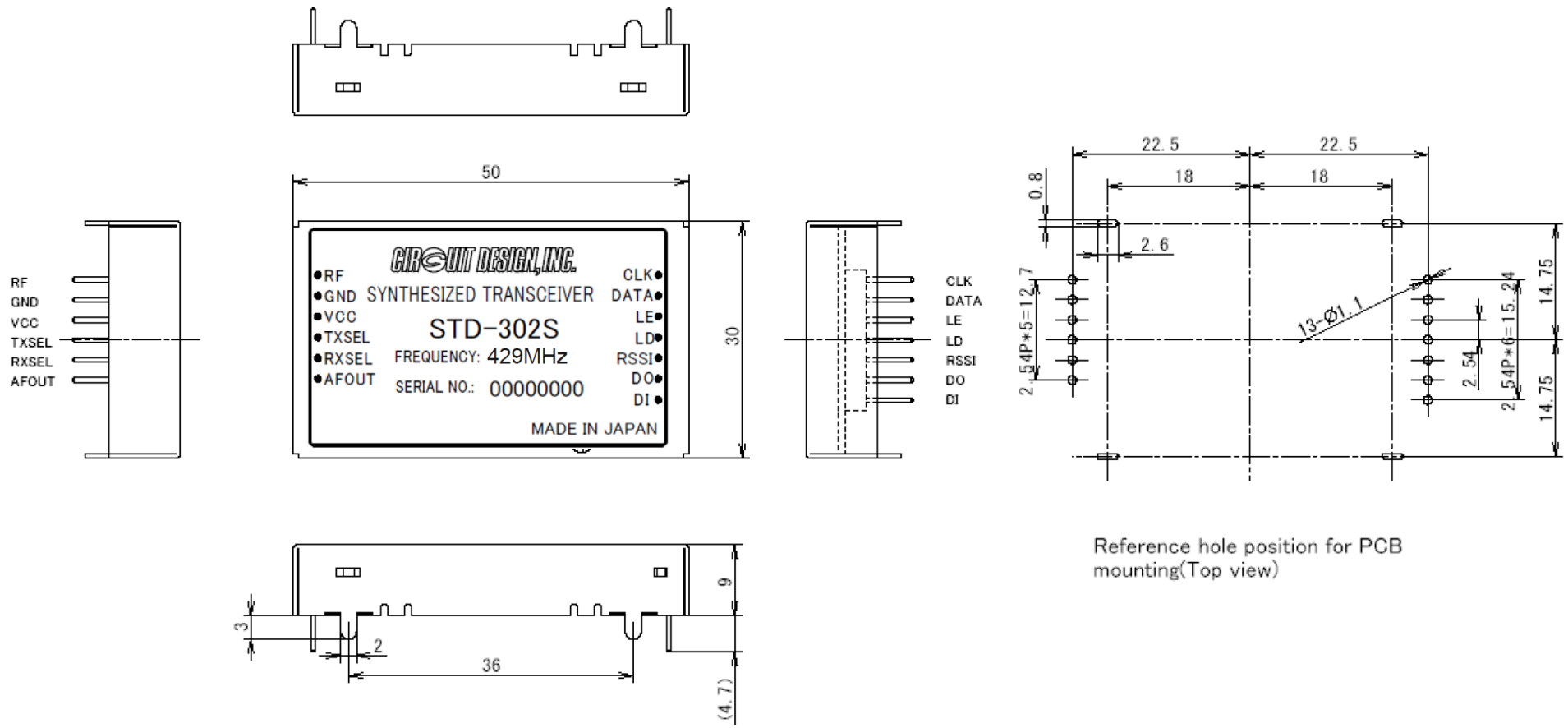
FREQUENCY TABLE (STD-T67)

Channel number	Operating frequency (MHz)	Transmission time restriction
1	429.1750	Transmission for 40 sec, pause for 2 sec
2	429.1875	
3	429.2000	
4	429.2125	
5	429.2250	
6	429.2375	
7	429.2500	Continuous transmission (Intermittent communication possible)
8	429.2625	
9	429.2750	
10	429.2875	
11	429.3000	
12	429.3125	
13	429.3250	
14	429.3750	
15	429.3875	
16	429.3625	
17	429.3750	
18	429.3875	
19	429.4000	
20	429.4125	
21	429.4250	
22	429.4375	
23	429.4500	
24	429.4625	
25	429.4750	
26	429.4875	
27	429.5000	
28	429.5125	
29	429.5250	
30	429.5375	
31	429.5500	
32	429.5625	
33	429.5750	
34	429.5875	
35	429.6000	
36	429.6125	
37	429.6250	
38	429.6375	
39	429.6500	
40	429.6625	
41	429.6750	
42	429.6875	
43	429.7000	
44	429.7125	
45	429.7250	
46	429.7375	

BLOCK DIAGRAM <STD-302S 429MHz>



DIMENSIONS

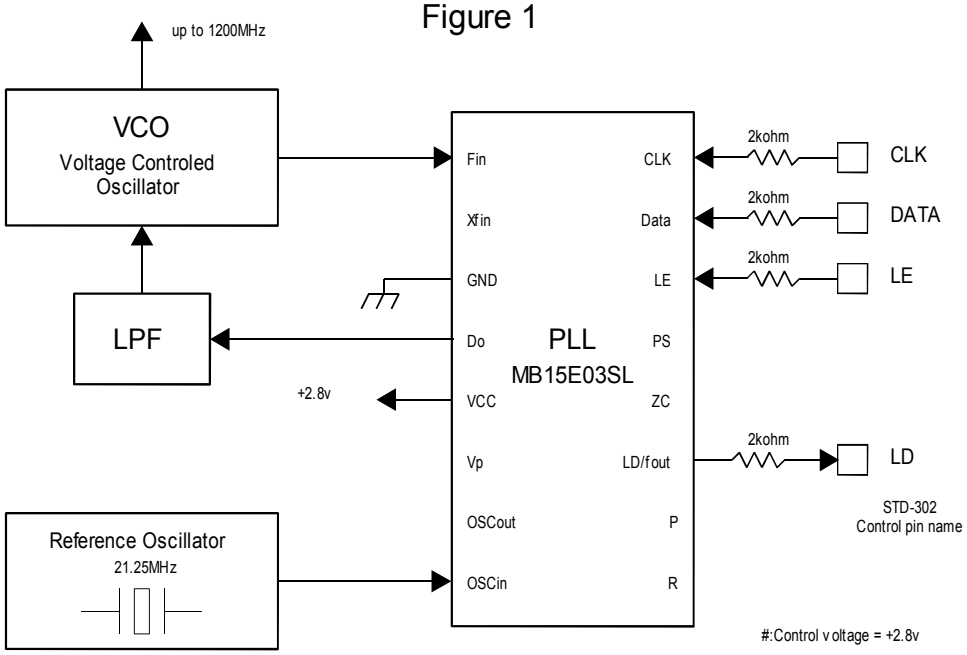


Reference hole position for PCB mounting(Top view)

PLL IC CONTROL

- **PLL IC control**

Figure 1



STD-302S is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302S has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302S has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302S is 2.8 V, so the control voltage must be the same.
STD-302S comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302S. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

- **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.
$f_{vco} = [(M \times N)+A] \times f_{osc} / R$ -- Equation 1
f_{vco} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$ A<N))
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302S, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch}. Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.
$f_{vco} = f_{expect} = f_{ch} – f_{offset}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency $f_{vco.}$ This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302S uses 21.25 MHz for the reference clock $f_{osc.}$ f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where “n” is the number for division.
$f_{vco}=n*f_{comp}$ ---- Equation 3 $n = f_{vco}/f_{comp}$ ---- Equation 4 note: $f_{comp} = f_{osc}/R$

Also, this PLL IC operates with the following R, N, A and M relational expressions.
$R=f_{osc}/f_{comp}$ ---- Equation 5 N = INT (n / M) ---- Equation 6 A = n - (M x N) ---- Equation 7
INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 429.500 MHz can be calculated as below.
The constant values depend on the electronic circuits of STD-302S.

Conditions: Channel center frequency: f_{ch} = 429.500 MHz
Constant: Offset frequency: f_{offset}=21.7 M
Constant: Reference frequency: f_{osc}=21.25 MHz
Set 12.5 kHz for Phase comparison frequency and 64 for Prescaler value M

The frequency of VCO will be
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 429.500–21.7 = 407.800 MHz
Dividing value “n” is derived from Equation 4
$n = f_{vco} / f_{comp}$ = 407.800 MHz/12.5 kHz = 32624
Value “R” of the reference counter is derived from Equation 5.
$R = f_{osc}/f_{comp}$ = 21.25 MHz/12.5 kHz = 1700
Value “N” of the programmable counter is derived from Equation 6.
N = INT (n/M) = INT(32624/64) = 509
Value “A“ of the swallow counter is derived from Equation 7.
A = n – (M x N) = 32624-64x509 = 48

The frequency of STD-302S is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies. Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.circuitdesign.jp).

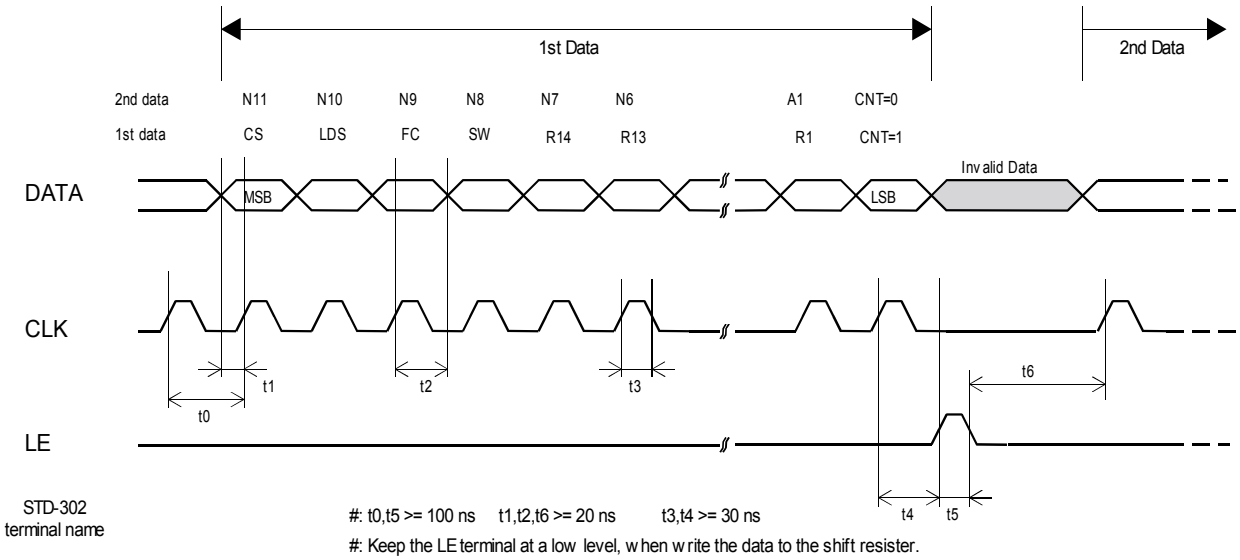
The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

- **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

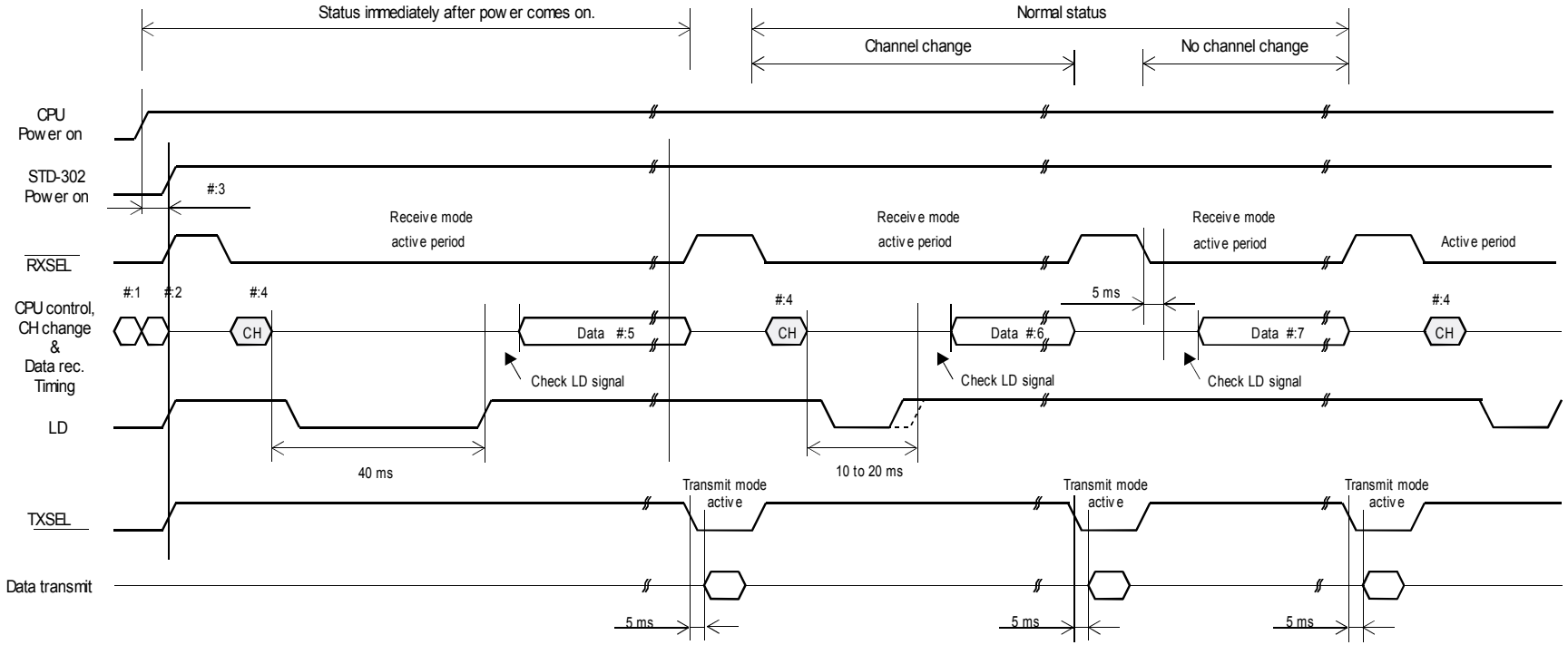
If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[*1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[*2].
Check that the Lock Detect signal is “high” 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[*1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is requested to verify operation at low temperature and optimize the timing.

[*2] Sending ‘10101…..’ preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver. For 4800 bps, a preamble of ‘11001100’ is effective.

Remark
For details about PLL control and the sample programs, see our technical document ‘STD-302 interface method’

Figure 3: Timing diagram for STD-302



#:1 Reset control CPU
#:2 Initialize the port connected to the module.
#:3 Supply power to the module after initializing CPU.
#:4 RFchannel change must be performed in receiving mode.
#:5 40 ms later, the receiver can receive the data after changing the channel..
#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.
#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

429 MHz ISM band (429.1750 – 429.7375 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	12.5
Start Channel Frequency F_{ch} [MHz]	429.1750
Channel Step Frequency [kHz]	12.5
Number of Channel	46
Prescaler M	64

Parameter name	Value
Reference Frequency F_{osc} [MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

: For data input
: Result of calculation
: Fixed value

Parameter name	Value
Reference Counter R	1700
Programmable Counter N Min. Value	509
Programmable Counter N Max. Value	510
Swallow Counter A Min. Value	0
Swallow Counter A Max. Value	63

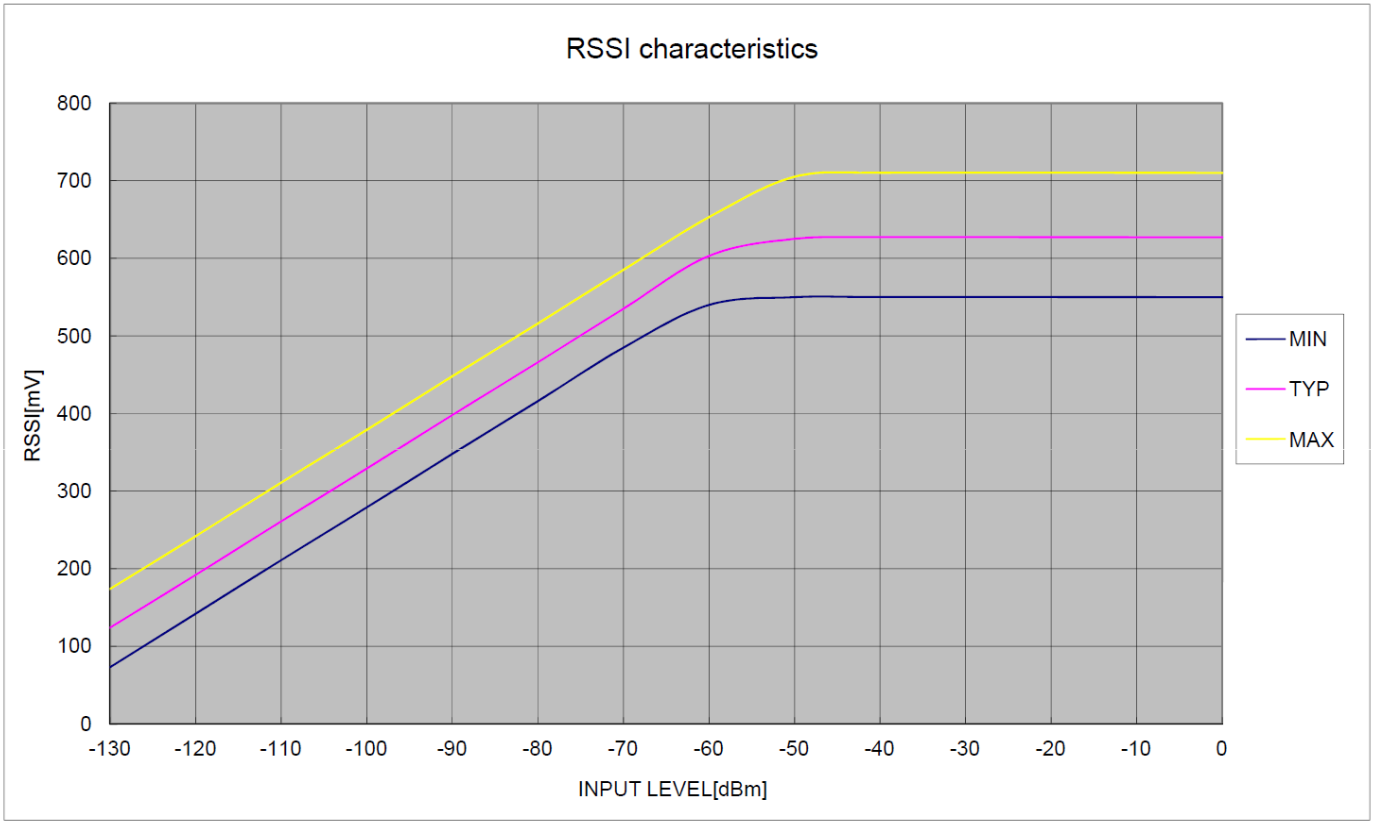
No.	Channel Frequency FCH (MHz)	Expect Frequency FEXPECT (MHz)	Lock Frequency FVCO (MHz)	Number of Division n	Programable Counter N	Swallow Counter A
1	429.1750	407.4750	407.4750	32598	509	22
2	429.1875	407.4875	407.4875	32599	509	23
3	429.2000	407.5000	407.5000	32600	509	24
4	429.2125	407.5125	407.5125	32601	509	25
5	429.2250	407.5250	407.5250	32602	509	26
6	429.2375	407.5375	407.5375	32603	509	27
7	429.2500	407.5500	407.5500	32604	509	28
8	429.2625	407.5625	407.5625	32605	509	29
9	429.2750	407.5750	407.5750	32606	509	30
10	429.2875	407.5875	407.5875	32607	509	31
11	429.3000	407.6000	407.6000	32608	509	32
12	429.3125	407.6125	407.6125	32609	509	33
13	429.3250	407.6250	407.6250	32610	509	34
14	429.3375	407.6375	407.6375	32611	509	35
15	429.3500	407.6500	407.6500	32612	509	36
16	429.3625	407.6625	407.6625	32613	509	37
17	429.3750	407.6750	407.6750	32614	509	38
18	429.3875	407.6875	407.6875	32615	509	39
19	429.4000	407.7000	407.7000	32616	509	40
20	429.4125	407.7125	407.7125	32617	509	41
21	429.4250	407.7250	407.7250	32618	509	42
22	429.4375	407.7375	407.7375	32619	509	43
23	429.4500	407.7500	407.7500	32620	509	44
24	429.4625	407.7625	407.7625	32621	509	45
25	429.4750	407.7750	407.7750	32622	509	46
26	429.4875	407.7875	407.7875	32623	509	47
27	429.5000	407.8000	407.8000	32624	509	48
28	429.5125	407.8125	407.8125	32625	509	49
29	429.5250	407.8250	407.8250	32626	509	50
30	429.5375	407.8375	407.8375	32627	509	51
31	429.5500	407.8500	407.8500	32628	509	52
32	429.5625	407.8625	407.8625	32629	509	53
33	429.5750	407.8750	407.8750	32630	509	54

34	429.5875	407.8875	407.8875	32631	509	55
35	429.6000	407.9000	407.9000	32632	509	56
36	429.6125	407.9125	407.9125	32633	509	57
37	429.6250	407.9250	407.9250	32634	509	58
38	429.6375	407.9375	407.9375	32635	509	59
39	429.6500	407.9500	407.9500	32636	509	60
40	429.6625	407.9625	407.9625	32637	509	61
41	429.6750	407.9750	407.9750	32638	509	62
42	429.6875	407.9875	407.9875	32639	509	63
43	429.7000	408.0000	408.0000	32640	510	0
44	429.7125	408.0125	408.0125	32641	510	1
45	429.7250	408.0250	408.0250	32642	510	2
46	429.7375	408.0375	408.0375	32643	510	3

TEST DATA

RSSI output level characteristic
Measurement frequency: 429 MHz / Modulation: unmodulated

25°C +/- 5°C



Signal level [dBm]	RSSI [mV] (Typ.)
-130	124
-120	192
-110	261
-100	329
-90	398
-80	466
-70	535
-60	603
-50	625
-40	627
-30	627
-20	627
-10	627
0	627

Measurement is done with the PLL setting control board prepared by Circuit Design.

Important notice

- Customers are advised to consult with Circuit Design sales representatives before ordering.
  Circuit Design believes the provided information is accurate and reliable. However, Circuit Design reserves the right to make changes to this product without notice.
- Circuit Design products are neither designed nor intended for use in life support applications where malfunction can reasonably be expected to result in significant personal injury to the user. Any use of Circuit Design products in such safety-critical applications is understood to be fully at the risk of the customer and the customer must fully indemnify Circuit Design, Inc for any damages resulting from any improper use.
- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.

Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take a part or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

REVISION HISTORY

Version	Date	Description	Remark
1.0	Jan. 2015		
1.1	Apr. 2015	RSSI graph was revised (P.18)	
1.2	Oct. 2015	Correction of erroneous description, RSSI graph was revised.	