Introduction to the Thermal Resistance Tester Model PDA-4:6

The **"Transient Thermal Resistance"** test is used as an indicator of the capability of a semiconductor DUT to dissipate heat whilst absorbing energy.

There are many explanations of this parameter. A **simple approach** is;

- choose a parameter within the DUT which can be calibrated as a "thermometer" of the chip's temperature. Choice will depend on DUT type, ease of measurement etc. For a diode, its forward voltage when conducting a set current is the usual choice, for 3 terminal devices, there many options,
- measure the DUT chip temperature when cold (V1) using the chosen method,
- hit the DUT with a known power pulse (volts x current).
- Immediately (<= 30usec) after energy removal, revert to the measurement circuit as before and measure the hot temperature (V2).
- Thermal Resistance for that pulse width will be;

  Temperature Rise (V2-V1) / Power in oC/W

This will give the Transient Thermal Resistance (or Dynamic Thermal Resistance or Thermal Impedance) value for that pulse width.

There are many notes available on this subject, on this parameter's applications and on the associated Static Thermal Resistance measurement. Challenge Innovations have a file of some of these papers but a search on "Google" or similar search engines is the ideal starting point.

The PDA-4:6 Transient Thermal Resistance Tester provides;

a) A dissipation supply with a current capability of 19.9 Amps in 0.1 A steps, a voltage capability of 20 volts in 8 bit (255) steps all for a time of 0.1 msec to 100sec.

b) Two measurement options, one which uses the DUT's threshold voltage V(th) with a set Vce and current on 3 terminal devices and Vf at a set current as the chip's thermometer, and choice of a 'K' or 'T' type thermocouple or a Pt100 resistance sensor to measure the package's temperature.

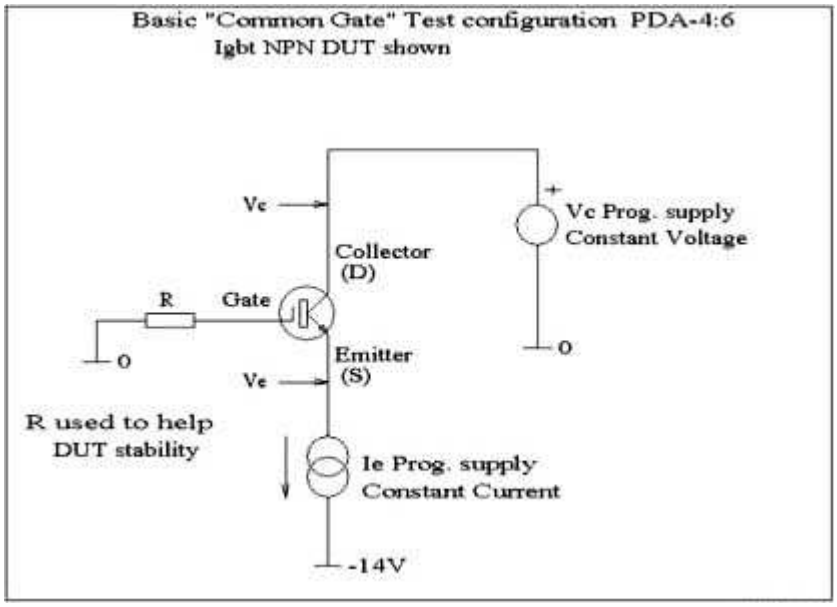
c) Facilities to test Diodes and Igbt/Power-fet devices. The "common Gate" circuit is used for dissipation and calibration of a 3 terminal DUT. A diode is treated as a collector (anode) and emitter (cathode) with gate open.

d) The link to the external control PC is via the RS-232 port, at the front of or at the back of the unit. The optional PC main software, written in Visual-Basic, sets up all the parameters in this Analyser and displays all the results.
There is a collection of calibration and repair software aids written in QBASIC included, as is the information on how to run the Tester using customer-written software.

e) All the necessary power supplies and control electronics.

Most modern power Igbt and power-fets are optimised to operate in switching mode. It is very difficult to make them operate in the linear mode necessary for energy dissipation. The “common gate” configuration has been found to give the most stable results and is used for both dissipation and temperature measurement in this Analyser.

A simplified “common gate “ configuration is;



The internal Adcon measurement system will monitor Vc , Ve and a differential amplifier will monitor Vc+Ve = Vce.
The calibration circuit used the same Vc and a lower value of Ie = Ical.

The test sequence is preset to (simplified waveforms shown below);

1. Measure the thermocouple / sensor temperature and store as T1,
2. Turn on the collector voltage Vc on to the required value, up to 20 volts. On diodes, set this to 0V.
3. Turn on the calibration current (Ical), choice of 0 to 100mA in 8 bit (255) steps,
4. If set Vce = 0, assume a diode is being tested, measure the Vf at this Ical and store this value as V1.
5. If Vce > 0 then assume an Igbt/P-fet is being tested, measure Vge at this Ical and store as V1.
6. Turn on the required collector dissipation current (Ic) for the required time (Tdiss). This energy will raise the temperature of the “chip”. On all device types, the Cs-Es voltage is measured during this dissipation period. On diodes a 10V full scale range is used, else a 50V full scale range. This value is used to calculate the Power.
7. At the end of the Tdiss period, the dissipation is quickly removed and the circuit reverted back to the calibration current (Ical) plus Vce state. This change must take place quickly (< 30µsec). The shape of the Es waveform will show the “Cooling Curve”.
8. After a chosen delay (PPS), measure the Vf or Vge again and store this (hot) value as V2. The AUTO choice does 3 samples of Vf/Vge then approximates the V2 value at dissipation removal time.
9. Measure the thermocouple /sensor temperature and store as T2.
10. The temperature rise of the “chip” is then proportional to
    delta V = V2-V1.
11. The energy dissipated is Vce x Ic therefore:

$$\text{Thermal Resistance (j)} = \frac{\text{delta V}}{K\ (\text{Vce} \times \text{Ic})}$$

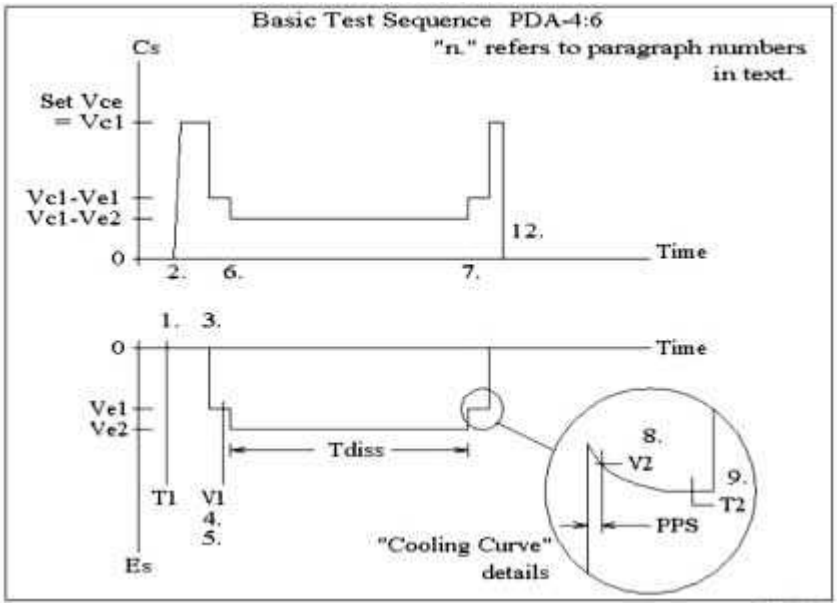
Where K is the “K-Factor” in mV/oC. This factor has to be

determined for the DUT before testing. There is a software facility provided with this Tester to simplify this job.

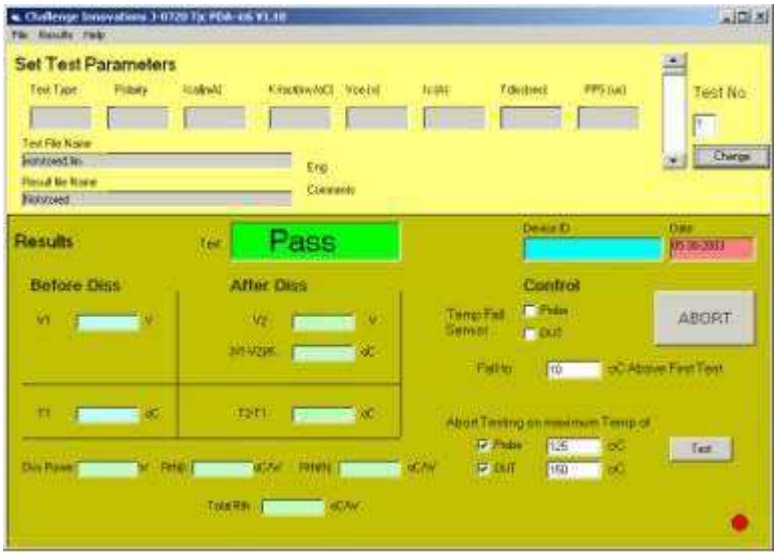
12. Switch (Ical) and (Vce) off.
13. The thermocouple / sensor derived Thermal Resistance is;

$$\text{Thermal Resistance (th)} = \frac{T2 - T1}{(Vce \times Ic)}$$

The **simplified waveforms** are shown below. These show the above paragraphs 1. through 9. then 12. but for a 3 terminal device;



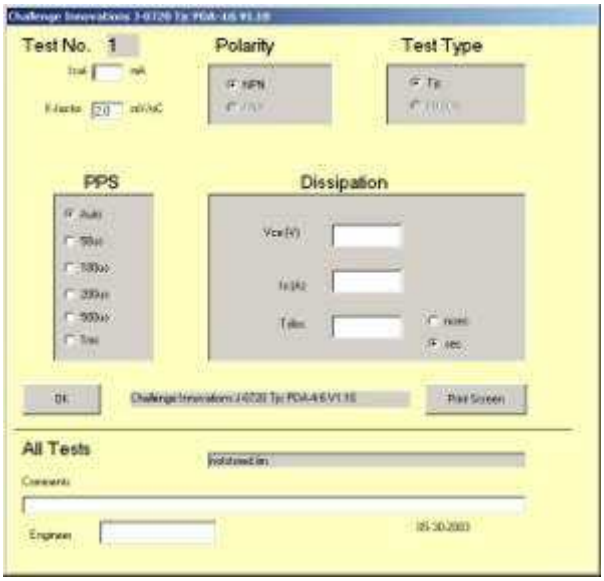
The "Windows" based software **PDA46ENG** provided will set the test parameters to the Tester's specifications, up to 100 tests with a temperature monitor choice between tests and all the usual facilities.



Shows the main screen. The top half shows the test parameters, the bottom the test results. The “Change” button enters the test set-up screen below.

Includes “Device ID” and a general Pass/Fail legend for production.

The test set-up screen allows each of the 100 tests to be set within the Tester’s spec.



A software package **KFAC03** provided allows the calibration of the DUT so that the K-Factor can be calculated.

The **PDA-4:6 Tester** is a complete unit housed in a choice of bench-top case, 560mm wide, 300mm high by 400mm deep or a “Standard 19 inch” cabinet format, 9U (400mm) high and 460mm deep. The control PC package with its software is external. Trolley mounted systems are an option.

Challenge Innovations make a range of similar Testers including;

PDA-4:4 - Similar design concept but capable of up to 20V and 360 Amps. Used for testing the larger multi-Igbt/P-fet modules.

PDA-4:5 - Similar design concept but capable of 1kV and 100A on bipolars, Igbt and P-fets in both polarities.

TRA2:7 - Special design of Static Thermal Resistance for diodes to 100A. Uses software generated rectangular and sinusoid (both 50 and 60 Hz) current waveforms. Samples the resultant voltage waveforms and, in the sinusoid option, calculates the dissipated power as the average value of multiple current * voltage samples.

Please contact **Challenge Innovations** or their Agents for further details and a ball-park price for these Testers or your special requirements.