STA - 3 Dynamic Parameter Tester

The **Dynamic Parameters** of a power semiconductor device are the measurements taken from and the behaviour of the device whilst switching from one state to another.
The wide use of power devices in switching applications makes the measurement of these parameters more and more important.
The main testing problem is to ensure that the measurements taken are of the device under test and not of the capability of the Tester. As the voltage and current capabilities of the modern power device increases, this problem can become very difficult.
Challenge Innovations make the STA-3 Dynamic Parameter Tester for the measurement of all the usual Dynamic parameters.
These include;

Inductive Load Switching;

Igbt	Clamp Diode
td(off)	Irrm
tfi	trr
Eoff	Qrr
td(on)	trr1
tri	Qrr1
tdv(on)	di/dt
tfv	s-factor
Eon	

Resistive Load Switching;

td - off to on current delay time (td(on)),
tr - off to on current rise time,
ts - on to off current storage time (td(off)) and
tf - on to off current fall time.

RBSOA;

Vce(pk)
Ic(pk)

Short Circuit Capability (a type of FBSOA)

Ic(pk) (max. current)
Iclamp (current flowing just before gate turn-off)
Ioff (current flowing after gate turn-off)

Clamped and Un-clamped Inductive Load Capability

Ilm, Eas etc.

Refer to the many “Industry Standard” definitions of these parameters.
Challenge Innovations' own definitions are included at the end of this Introduction.
Challenge Innovations also produces a range of “Information Notes”. These show the test results obtained from a range of the many device types we have tested.
Please ask for a copy. A list of these “Notes” is shown in the Feb-03 or later “Decision Guide” section of the web site.

Test Methods;

All the **Inductive Load Switching and the RBSOA tests** are made on the **classic test circuit** shown in Fig A. The device under test DUT1 (an Igbt is shown) is connected via an inductive load L across a capacitor bank C. Its gate is driven by a fast gate driver with the required series resistors Ron and Roff. If an associated clamp diode is to be tested (Clamp Diode Tests) it is connected as DUT2. If not, then a suitable diode must be added as DUT2 and the diode tests skipped.

First the capacitor bank C is charged to Vcl using the charger PS inside the Controller Box. When charged, it is fully isolated from this charger supply by relays.

The simplified waveforms are shown in Fig B.

1. The gate of DUT1 is turned on for a programmed time Tch. This time is chosen in the test software to charge the load L to the required current Ic. The DSO is triggered at about this time.
2. The gate is turned off for a suitable time, usually 10usec.. All the turn-off measurements are made from this part of the waveform.
3. In the Inductive Load test, the gate is turned back on for a suitable time. All the turn-on measurements on DUT1 and , if the if required, the diode measurements on DUT2.
   In the RBSOA test this second turn-on is skipped.
4. The gate is turned off and the test sequence finished.
5. The DSO waveforms on Ch1,Ch2 and Ch3 (some designs also Ch 4 for improved voltage or current resolution) are now downloaded to the control PC for processing then result display, EXCEL download etc..

The capacitor bank C is now discharged.

This sequence is repeated for every test type or whenever a different Vcl and / or Ic is required. If all the Inductive Load Switching tests (Igbt + Diode) are made at one Vcl and Ic value, then only one charge/discharge sequence will be needed.

Notes:

- The turn-off measurements (2. above) are made at the first turn-off to keep the current Ic as equal as possible to the Ic at turn-on (3. above).
  This allows;
  - the inductor L and the capacitor bank C to be relatively small,
  - the charge up time for the capacitor bank C to be kept short and
  - the discharge energy into a bad DUT to be kept small (limit the big bang).

  The design of the test head will optimise all these factors to suit the DUT1 and DUT2 used.

- The Vge display (Ch 1) is taken directly from the DUT1 gate after the series resistors Ron and Roff. This method will show the gate charge effects and any “ringing” present.

- The DSO is always grounded. The emitter sense terminal of DUT1 is used as the common point and is switched to suit whichever device is tested in a multi-device module. All the other parts of this test circuit are fully isolate during the test sequence. As a bonus, all the waveform displays will be the same polarity for all arms of an “H” connected module.

- When the module is presented to the test contacts, the gates are arranged to make first contact. All the gate drivers are always driving “off” except for

the one used in the active test sequence.

- There is an "Integrity" test performed at the start and at the end of each sequence. This test is transparent to the software. It tests both the DUT for a short and open condition plus it's associated diode. Any fault is shown in the test result.

When measuring the **Clamp Diode Parameters**, there is an option available to add a second current transformer into the diode current loop and connect this into Channel 4 of the DSO. The PC software is modified to download this extra channel and to compute the diode parameters from this download. This option greatly improves the accuracy of the diode measurements.

The **Short Circuit Capability Test** uses the same items as above but now the DUT1 is connected directly across the capacitor bank C and the clamp diode shortd. The capacitor bank is charged to the required voltage and the DUT1 gate turned on for (usually) 10usec. The DUT1 gate is then turned off and, sometime later, the capacitor bank discharged. The DSO waveforms of the test sequence are downloaded and the results computed.All the above notes apply.

The above Test Method description shows a single DUT+Diode combination. When testing **multiple DUT modules** the same method is used but relays bring each of the DUT+Diode combinations into test. The Tester's micro controls all these relays, their delays etc.. A strict rule is that all relays are only changed when the capacitor bank is discharged. Half briges (two DUT+Diode), 3-phase bridges (six DUT+Diode) and 3-phase bridge plus brake (seven DUT+Diode) are all common applications.

In general, the design always uses **separate gate drivers**, one for each DUT. All gate drivers are fully isolated from ground and each other using HF transformers for the power side and opto couplers / fibre optics for the signal side. The DSO common is always earthed. Reed relays switch the DSO inputs to the various DUTs.

Please contact **Challenge Innovations** for more information on all the test types and typical waveforms obtained.

The STA-3 Tester;

The **Challenge Innovations STA-3 Dynamic Parameter Tester** brings together all the necessary parts for testing a wide range of modern power semiconductors housed in single device packages and in multiple device modules. Its design incorporates many years of experience of this type of testing, both for volume production and for evaluation purposes.

Picture showing a typical STA-3 Tester with the MCP-5 based Safety Test Head.

An STA-3 Tester is divided into 5 major parts;

1. **The Digital Sampling Oscilloscope (DSO).** This is a commercial item chosen from the range sold by Tektronix and LeCroy. It can be provided by Challenge Innovations as part of the STA-3 Tester package, purchased

separately or an existing unit used. The DSO is used only as a 3 (or 4) channel digitizer. Its internal computation facilities are not used. All the downloaded samples are manipulated then the parameters calculated by Challenge Innovations software running in the external control PC (item 4. below).
This method of DSO use is based on long experience and probably provides the best testing speed / greatest computation power combination.

The algorithms used in the computation include;

- compensation for voltage probes offsets
- current transformer offsets,
- corrections for any time delays and non linearities in the measurement transducers used,
- distortions in the gate drivers etc..

The DSO is not modified or fixed to the Tester and can be used for other purposes when not required by the STA-3. Challenge Innovations will provide the data on the various DSO types and the website has the address of both manufacturers. The DSO is linked to the external control PC using either the IEEE-488 bus, the RS232 (in special circumstances) or the Ethernet 10BaseT bus depending on the DSO choice.
The usual choice is the LeCroy DSO with the Ethernet link.

2. The Controller Box. This is used for all versions of the STA-3. It contains a microcontroller for overall hardware control, the Adcon and Dacons for internal measurements, the capacitor bank charge P/S and the link to the external control PC. All are housed in a box;

The capacitor bank charge P/S is chosen from the LAMBDA-EMI or similar series.
They range from 1kV to 6kV (or 10kV) in output voltage with various charge rates for each voltage. Please contact **Challenge Innovations** for further information.
Remember that most dynamic measurements are taken with the capacitor bank at half the DUT's rated voltage.

3. The Safety Test Head brings together the Device under Test (DUT) with all the parameter set-up components, using the best possible contact and circuit techniques. This is where the waveforms obtained will either show the DUT's true performance or the Tester's flaws.
Challenge Innovations have made many such Test Heads on a broad range of packages over many years. Each is optimised for that package. The method used is to divide the Test Head into two parts –

a. **LOWER SECTION** which does the mechanical handling of the package, its temperature control (option) and it's insertion into the test circuitry.

b. UPPER SECTION which carries all the critical test circuitry. This includes the test relays, multiplexer relays, current transformer/s, DSO inputs probe connections, the load coil etc..

The Safety Test Head design is usually an adaptation of the Challenge Innovations range of Safety Test Heads which best suits the size of the package or packages that are to be tested.

These include;
MCP-3 for packages up to 190mm x 280mm by up to 120mm high,
MCP-5 for packages up to 70mm x 140mm by up to 30mm high,
MCP-7 for packages up to 150mm x 160mm by 30mm high.
(The OSC-5 is unsuitable for dynamic testing).
Please refer to "The Safety Test Heads – An Introduction" in our web site for further details.

Dynamic Parameter Tester Model STA-3 Safety Test Head adapted from MCP-5

A typical example shown above is the adaptation of the MCP-5 for testing the "ECONO-2 / 6pack" and the "ECONO-2 / PIM" modules widely used in motor controllers.

In this example, because the pin-outs of the two module are very different, two UPPER SECTIONS are supplied, one for each package type plus one LOWER SECTION common to both. Use is made of pneumatics for device movement and, if needed, vacuum pads for device retention.

Similar size UPPER SECTIONS could be added for the ECONO-3 module and another for the Half-Bridge and Single Device packaged in the industry standard 62x108mm base package.

In the experience of Challenge Innovations, there is no practical "universal test head" design for dynamic testing. Each module outline will need its own best contact method, best circuit layout, best gate drive generator position and type, best current measurement method and so on.

Existing installations include MCP-3 adaptations for up to 140 mm x 190 mm Igbt modules pairs (one as igbt + one as diode) tested to >3kA and >3kV and others used for volume production and incoming quality testing.

A new design of floor mounted Safety Test Head adapted from the MCP-3, extends this capability to > 5kA and 5kV for testing the new range of 3.3kV and 6.5kV power Igbt used in the traction market.

4. External control PC. This is a commercial unit chosen from a wide range of manufacturers and a wide range of performance specifications. The latest "Windows" operating software is currently used and the usual packages ("Excel", "Word" etc.) are included. It can be provided by Challenge Innovations as part of the STA-3 Tester package or supplied by the customer.

5. Software.

The STA-3 Tester contains a collection of programmes designed to provide a wide range of facilities.

The "DOS" based package consisting of STA3ED and STA3ENG and is being replaced by the "Windows" fully integrated package STA3WED and STA3PROD.

STA3WED - The Editor, which guides the operator through the task of producing test files or modifying existing test files, then storing them into the database.

There are many facilities provided including:

- Test type menus with test limits made to suit the Tester's hardware.
- Up to 100 tests per file .
- All the usual editing facilities, i.e. add, delete, insert change etc.
- Printout of all or part of the file for reference and storage.
- Removable "Key Disk" floppy for secure entry with identification of user.
- Retrieval and storage of the file to/from any part of the PC's disk with listing of directories.

A typical example of an STA3WED page is shown below. Here a half-bridg module will be tested for seven parameters. Each test has it's max. and min. limits set. The Mux=1 cell shows that these tests will be made on the "upper" DUT using the "lower" diode. A change in the Mux cell to "Mux=2" will test the other combination.

The various pull-down menus provide all the usual facilities.

Perhaps the most useful facility is that, if the STA-3 Tester and DSO is connected to the PC, then the tests on the list can be performed immediately andthe results displayed in the “Results” and the “P/F” columns. This means that a test file can be thoroughly tested and verified as it is written and before storing into the PC’s disk, all inside one programme.

The DSO pull-down menu includes options to;

- display the special sample points shown in the “Definition” sheets below,
- dowloading all the active channel samples into a .csv file for loading into “EXCEL”. Later these can be used to reproduce these waveforms,
- choice of channel used to trigger the waveforms,
- choice of gains for various channels.

STA3PROD - The “Windows” based production driver.
This is a visual display of the pass/fail performance of a multiple device module.
It is ideal for use by non-engineering people. It presents the module’s test plan on one screen, it shows in real time the tests taking place then shows the final test result. It is a big change from the never ending “test results column” approach of the other commercial packages.
When first loaded, the user is presented with a display of 30 columns arranged in a 10 wide by 3 deep matrix.

Each column represents all the tests that will be done on one device in a multi device module.
The user then sets this matrix arrangement to suit the module to be tested.
Three examples are;

A shows a six-pack module with devices 1 thro 6 sequenced from left to right,
B shows a similar six-pack plus brake Igbt and diode module with the three “upper” Igbts plus the brake diode on the top row and the three “lower” Igbt plus the brake Igbt on the bottom row,
C shows a PIM module with the six Igbt on the top row, the six power diodes on the middle row and the brake Igbt plus diode on the bottom row.

Note that the widths and heights of the columns are automatically sized by the software to suit the screen space available.
The choice is completely open within the starting 10 wide by 3 deep matrix.
Each column is now given a descriptive label, a multiplexer number which conforms to that device’s position in the “Upper Section” wiring and a test file name previously generated and tested within the editor programme ATS2WED.
This means that up to 3000 tests (30 x 100) can be performed in a test sequence.
The columns are automatically graduated with the number of tests represented by that column. This matrix design is now saved for future use.
One example is a two column matrix generated for testing the above half-bridge;

As only two devices, Igbt1 and Igbt2 are to be tested, only two columns have been used, one above the other to represent the two halves of the module. Two columns side by side could also have been chosen.
The test sequence is then started by the choices available ie, close the drawer on the Safety Test Head, click on the “Start Test” button, hit the F10 key etc.

As the testing proceeds, as each device is tested, that column’s graduations will display green for a passed and red for a failed test. Note that as the original test file had 7 tests, there are 7 graduations in each column.

At the end of the test sequence, the legend at the bottom of the screen will show a large **“PASS"** on a green background, **“FAIL"** on a red background, “**O/RANGE**" on a pink background etc. depending on the overall test result.
Now any graduation of any column can be inspected by clicking on it. This will display the test type, parameters and the result obtained.

The facilities now include;

- Direct loading of the test results into EXCEL running as a parallel task. This facility allows special macros to “massage” the results and display them in a format required by the customer.
If testing is aborted during a sequence, only the testing task will need to be re-started. The test results previously obtained are kept within the Excel task.

- The statistics, graphs, printout options etc. are all produced by macros within Excel. There is a wide range available or can be provided by Challenge.

- Facility to “Skip failed multiplexer position” or “ Abort testing” completely on the first failed test.

- Facility for reading a module’s bar-code before testing.

- Ethernet link between the Tester’s PC and a general network is a simple and proven option that works well.

All the desired programmes are run from the operating system in use by typing the programme's name or clicking on the “desktop” logo. Because this is a “windows” based package, all the usual multi tasking facilities can be used.

There are separate “Information Notes” which show typical results from a range of device types.

The STA-3 Tester is supplied with:

- One A4 size manual containing:
Operating instruction on the hardware and the software.
Calibration procedures with details of Challenge Innovations calibration equipment used.
Listings of all the diagrams supplied.
All the A3 and A4 size diagrams.
All the printed circuit card layouts and parts lists.
Maintenance and repair procedure.

List of any spare parts included.
Any A2 size electrical diagrams and other manufacture's handbooks, in a wallet.
- All the standard software provided with this Tester in a CD rom / floppy disks.
- Spare parts of all the items that are not readily available within the EC, US etc. markets. More comprehensive spares kits are available.
- Certificates of conformance to the LVD and EMC regulations.
- Optional trolley or table made to carry the STA-3 Tester plus the DSO, PC and printer.

The **Challenge Innovations** dynamic test definitions follow on the next three pages;

These reduced size pages are from the STA-3's handbook. The latest and larger versions are available on request.

The Inductive Load "Off" measurements

The Inductive Load “On” measurements

NOTE: This simplified Diode Measurements set-up uses the inverse of Vce shown in diagram STDEF_ON for the voltage. For greated accuracy and a requirement if Erec is to be measured, a second current transformer needs to be wired into the diode current loop and a differential probe needs to monitor the diode voltage. Contact Challenge Innovations for details.

Challenge Innovations Inductive Load Test / Diode Definitions Apr - 02 STDEF_DI/B

The Inductive Load “Diode” measurements.

The RBSOA measurements.

The Short Circuit Test measurements

Summary:

- The STA-3 will test for all the normal Dynamic Parameters on a very wide range of Igbt and power-fet modules, all with their associated diode.
BJT can be tested but with special options.
- It will present the test results on the VDU and download then directly into “EXCEL”. All result printouts, graphics, statistics, reports etc. use “EXCEL” as the starting point with macros written by Challenge Innovations or the customer.
- The STA-3 is a complete unit, there are no extras to add.
- The STA-3 consists of;
- DSO LeCroy LT series with the Ethernet link is the usual choice.
- Controller Box includes the capacitor bank charge power supply.
A 1kV unit will suffice for devices with up to 2kV working, options to 5kV.
- Safety Test Head dependent on the range of modules/devices to be tested.
The MCP-5 for base sizes to 70mm x 140mm,
the MCP-3 for base sizes to 190mm x 280mm and
the MCP-7 for base sizes to 150mm x 160mm are the usual choices.
One separate “Upper Section” is required for each module type.
Sometimes more than one module type can be accommodated by one “Upper Section” but this depends on many factors. Please ask.
- Control PC plus printer.
- Software Package including STA3WED and STA3PROD,

- Optional trolley or table to carry all the above.

To obtain the latest prices contact **Challenge Innovations**, or their Agents, with the range of module/device packages and the dynamic test requirements of all the units to be tested.
A price plus delivery time will then be provided.