PFC-PWM CM6800/01/02/24 and CM6900/01/02 Design Algorithms

Also, for Single PFC, CM6500 and CM6501, Please use the equations for CM6800/01/02

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All the values should be typical values unless it was specified otherwise.

1.) Select Switching Frequency

Majority designer will select fpfc=70Khz to ease the EMI design.
Fosc=fpfc=fpwm for CM6800/01/24 and CM6900/01
Fosc=fpwm= 2 x fpfc for CM6802 16 pin or CM6902 20 pin

Fosc=1/(tramp+tdeatime) for CM6800/01/24 and CM6900/01.
Fosc=1/(4x(tramp+tdeatime)) for CM6802 and CM6902.
Tramp=Ct x Rt x 0.5108256
Tdeadtime=800 x Ct + 200nS
Tdeadtime/Tramp should be around 5%.

Usually, we choose Ct between 1nF to 470pF.
If we choose Ct=470pF, to design fosc=70Khz, Rt=57.1K ohm.

2.) Select fpfc=fpwm or fpfc= 0.5 x fpwm

Only CM6802 16 pin and CM6902 20 pin are fpfc=0.5 x fpwm.

All the CM6800/01/24 and CM6900/01 family is fpfc=fpwm.

3.) Choose from CM6800/01/02 16 pin, CM6900/01 20 pin, or CM6824 16 pin,
GMv = 65umho for CM6800/01/02, and CM6901/02
GMv = 85umho for CM6824
GMi = 100umho for CM6800/01/02 and CM6900/01
CMi = 195umho for CM6824

Definition: (When VEAO = 6V which is the maximum VEAO.)

Igainmod = Isense-Ioffset (here, Ioffset~75uA)
K~0.372093 which is the peak value when VEAO = 6V and VRMS=1.1V for CM6800/01 and VRMS=1.2V for CM6824.

K of the Gain Modulator = (Isense-75uA)/[IAC x (VEAO-0.625)] [1/mV]

K of the Gain Modulator = Gain/(VEAO-0.625) [1/mV]

K of the Gain Modulator = Gain/(6-0.625) = Gain x 0.1860465

K≒0.4502325/(VRMS)^2 (VRMS PEAK AT 1.1Vfor CM6800/01) and K≒0.535814/(VRMS)^2 (VRMS PEAK AT 1.2V for CM6824)

Maximum Gain of the Gain Modulator = 2 = (Isense-88uA)/IAC = K x 5.375 When VEAO = 6V.
Igainmod = K x [IAC x (VEAO-0.625)]
Igainmod = [IAC x (VEAO-0.625) x 0.4502325]/VRMS^2 for CM6800/01/02 and CM6900/01
Igainmod = [IAC x (VEAO-0.625) x 0.535814]/VRMS^2 for CM6824

Igainmod x 3.6K ohm =Iin x Rs For CM6800/01/02, CM6900/01/02,

Igainmod x 3.6K ohm =Iin x Rs For CM6824.

4.) Design Self-Bias Section for powering up the chip:

Typical VCC should be around 15V for all the CM6800/01/02, CM6900/01 and CM6824 despite the UVLO is 13V or 15V.

Designers have 3 choices to power up the chip:

1.) Boost trap the voltage from the boost inductor.
2.) Boost trap the voltage from the DC-to-DC transformer.
3.) Combine 1 and 2.

In this section, we need to consider the following issues:

a. Switching Noise:

Designers should add a resistor between the boost trap winding and the chip. The pole frequency should be less than 100hz.

b. Hold-up time: Assume the hold-up time 30mS.

Depending the external power mosfets, it will determine the supply current of the controller and driver section. Usually, it is less than 20mA. Therefore, the bypass capacitor will be around 120uF.

c. Boost trap resistor:

The start-up current is around 100uA. A 600K ohm resistor is able to turn-on the chip when VIN is 80VAC. However, it will be slow. A 100K ohm resistor will be faster but it reduces the efficiency during the light load. Therefore, designer could choose a High Voltage depletion NMOS to boost trap the self-bias section.

5.) Design the DC to DC Stage:

Usually, designer will select the single switch forward converter for the DC to DC stage.

a. Design the transformer ratio:
In this section, designers should consider the hold-up time and efficiency. The maximum duty cycle of the DC to DC section is between 45% and 50%.
Since the DCOK threshold is 1.5V and 2.45V, it represents the PFC output voltage from 381.8377V to 230.1026V. Therefore, even the input voltage of the DC to DC stage is 230.1026V; the final DC output needs to be regulated.

For example, if the output is 5V, turn ration should be 20 ~ 230.1026 x 0.45/5. Therefore, during steady state and the input voltage of DC to DC stage is 381.8377V, the PWM duty cycle will be around 27%.

6.) Design the AC to DC Stage:

Based on the input voltage range and the maximum the input voltage, we start to design the AC to DC stage, PFC Boost Converter.

a. Base the maximum input power DC to DC stage to define the maximum input power of AC to DC stage (PFC stage):

Assume the efficiency of PFC stage is 80%. If the maximum DC to DC input power is 350W, the maximum input power of the AC to DC will be 437.5W.

b. Design the current sensing resistor, Rs of the PFC stage:

Rs = 0.7V x Vin peak x 1.414214/(2 x Maximum input Power)

= 0.7V x 80V x 1.414214/(2 x 437.5W) = 0.09050967 ohm.

c. Design the filter on ISENSE (pin 3)

This filter should be located between fpfc and fpfc/6.

Rfilter usually should be less than 100 ohm.

If fpfc = 70Khz, and fpfc/6 = 11.666667Khz,

Cfilter is 139.4185nF and Rfilter is 100 ohm.

There are 2 purposes of this filter:

1.) Protect Isense pin because during the start up, the inrush current and voltage can be very very big on pin 3.

2.) If the customers use the small inductor and the boost is in DCM, it will enhance the THD performance.

(Be Careful**: This will create additional pole for the current loop.)**

d. **Design the VRMS Filter:**

To get the constant power, the constant band width and to get the brown out at your design low line, VRM filter and Rac will determine them. Therefore, it is very important to design the RAC and VRM filter.

When the input line voltage is the lower line voltage, the VRMS voltage should be average 1.1V with ripple less than 200mV.

Usually, it is a 2-pole filter without any zeroes. However, to get the good line transient when your customers request to test line voltage from 80VAC to 260VAC then from 260VAC back to 80VAC in the short period. It will require a 2 pole low pass filter with a high pass filter. To get the detail information, please see the websim circuit or contact our application engineers.

e. Design the Rac for pin IAC (pin2):

Rac = Vin peak x 7.9K. If Vin peak is 80 x 1.414214=113.137, Rac = 879.9551K ohm.

f. Design the Boost Output Voltage and the resistor divider.

The Boost Output Voltage should be determined by the maximum input voltage. Typical maximum input voltage is 270VAC for universal input voltage; therefore, the peak input voltage is 270V x 1.414214= 381.8377 , which should be the output voltage of the PFC Boost Converter.

The reference voltage of the VFB is 2.5V. Rb/(Ra+Rb) = 0.00657284.
Let Ra + Rb = 0.7 M ohm. Rb = 4.583099 K ohm and Ra = 695.4169 K ohm.

g. Design the Boost Capacitor, C

The value of the Boost Capacitor, C should be determined by the desired hold-up time when the input voltage is suddenly removed.

If the hold-up time is around 30mS, C needs to hold up enough energy for 100mS from 381.8377V to 230.1026V because the VINOK comparator threshold is 2.45 and 1.5V.

The different energy during the hold-up time is (0.5 x C x 145.8K)-(0.5 x C x 52.94722K). [(0.5 x C x 145.8K)-(0.5 x C x 52.94722K)]/(hold-up time) is the maximum DC to DC power.

For example: If the maximum DC to DC input power is 350Watt,
C = 350W x (hold-up time) x 2/(145.8K-52.947K)
C = 700W x (30mS)/92.853K = 226.1639 uF

Boost converter C will be protected when boost converter is more than 10% of the design value, which is 420.0215V.

Typical Boost Converter C is rated at 400V.

h. Design the Boost Inductor, L

The value of the Boost Inductor should be determined by the desired minimum input ripple current when the input voltage is minimum.

For example: If the minimum input voltage is 80VAC and the output voltage of the PFC is 381.8377V, the delta voltages are 80V x 1.414214 = 113.1371V and 268.7006V. During the steady State, duty cycle is 0.7037037; therefore, On time is 0.7037037 x (1/70Khz) = 10.05291uS and Off time is 4.232804uS.

Based on the desired input ripple current, we can define L when the input power of AC to DC is the maximum condition. Here, we use 437.5Watt for the maximum input power of the boost converter. The input line current will be peak at 1.4142 x 437.5W/80 = 5.46875 x 1.414214A = 7.73398 A. The 20 percent of 7.73398A is 1.54696A. Now, we have all the data and we can calculate L. L = 113.1371V x 10.05291uS/1.54696A = 735.2987 uH.

i. Design the Voltage loop of the Boost Converter

Mainly in this section, we need to design the compensation network, Zcv. Typically, Zcv is a lead-leg compensation net work which is composed of 1 pole and 1 zero; therefore, Zc has 2 Capacitor, C56 and C57 and 1 resistor, R63.

Loop Gain of the Voltage Loop = (dVout/dVeao) x (dVfb/dVout) x (dVeao/dVfb)
= Pin x 2.5V x GMv x Zcv/(381.8377 x dVeao x S x C x 381.8377)

Pin: Maximum Input Power
GMv: VEAO's transconductance. GMv~65u mho (CM6800/01) GMv~85u mho (CM6824)
Zcv: Compensation Net Work at VEAO, Voltage Error Amplifier
Vout: 381.8377V, PFC boost converter output voltage
DVeao: Maximum Effective Swing which is 6V – 0.625V = 5.375V

Usually, fc, the unity gain frequency of the voltage loop is 0.5 x line frequency ~ 60/2 = 30hz.

First, let loop gain = 1 when S = line frequency/2 = 30 hz.
It means GMv x Zcv = (381.8377V x 381.8377V x 5.275V x 30hz x 2 x π x 226.1639 uF)/(Pin x 2.5V) ≒ GMv x R63.
From Above equation, R63 = 469.9256 K ohm (CM6800/01) = 359.3548 K ohm (CM6824).

Second, fc = 30 hz ≒ 1/(2 x π x R63 x C57). Therefore, C57 = 1/(2 x π x R63 x 30) = 11.28937nF (CM6800/01) = 14.76303 nF (CM6824). The fc actually is the pole location of the error amplifier.

Third, let fz = 0.1x fp; fp = 30hz, therefore, fz = 3hz and C56 = 10 x C57 = 112.8937nF (CM6800/01) = 147.6303nF (CM6824).

j. Design the Current loop of the Boost Converter

Mainly in this section, we need to design the compensation network, Zci. Typically, Zci is a lead-leg compensation net work which is composed of 1 pole and 1 zero; therefore, Zci has 2 Capacitor, C41 and C43 and 1 resistor, R58.

Loop Gain of the current loop = (dVieao/dVs) x (dVs/dDoff) x (dDoff/dIeao) = (Gmi x Zci) x [(Vout-Vin) x Rs/(S x L)] x (1/2.5)

Gmi: Current Loop Error Amplifier's Transconctance; Gmi = 100u mho (CM6800/01) and Gmi = 195u mho (CM6824)
Vs: Signal at Isense pin called Vs, which is also, is PFC sense resistor signal.
Doff: (1-Don)
DIeao: Maximum effective swing at IEAO, Pin 1 and Here, Dieao = 2.5V
Vout-Vin: The worst condition is vin=0V and Vout = 381.8377V

Usually, fc, the unity gain frequency of the current loop is fpfc/6 ~ 11.66667Khz.

First, let Loop Gain of the current loop = 1 = (Gmi x Zci) x [(Vout-Vin) x Rs/(S x L)] x (1/2.5) when S = 2 x π x 11.66667Khz. It means Gmi x Zci = (S x L x 2.5)/(Vout x Rs) = (2 x π x 11.66667K x 735.2987 u x 2.5)/(381.8377 x 0.09050967)=3.899031≒Gmi x R58.
From above equation, R58 = 38.99031Kohm (CM6800/01/02 and CM6900/01/02) = 19.99503Kohm (CM6824).

Second, fc = 11.66667Khz = 1/(2 x π x R58 x C41); therefore, C41 = 347.878pF (CM6800/01/02 and CM6900/01/02) = 682.262pF (CM6824).
However, due to the filter on Isense pin, C41 is optional and C41 is not a necessary components.

Third, C43 = 10 x C41 and C43 and R58 will create the zero for the current loop. Therefore, C43 = 3.47878nF (CM6800/01/02 and CM6900/01/02) = 6.82262nF (CM6824).