GENERAL DESCRIPTION

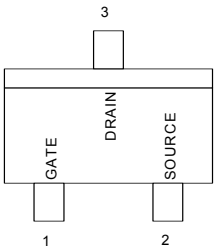
This N-Channel enhancement mode field effect transistor is produced using high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching and ESD enhanced performance. It can be used in most applications requiring up to 115mA DC and can deliver pulsed currents up to 800mA. This product is particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

FEATURES

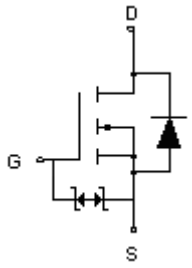
- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability
- ESD Protected 2KV HBM

PIN CONFIGURATION

SOT-23
TOP View



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT2N7002K	SOT-23
CMT2N7002KX*	SOT-23

***Note:** X : Suffix for Halogen Free Product

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage (R_{GS} = 1.0MΩ)	V_{DGR}	60	V
Drain to Current — Continuous	I_D	115	mA
— Pulsed	I_{DM}	800	
Gate-to-Source Voltage — Continue	V_{GS}	±15	V
— Non-repetitive	V_{GSM}	±15	V
Total Power Dissipation	P_D	225	mW
Derate above 25℃		1.8	mW/℃
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	℃
Thermal Resistance — Junction to Ambient	θ_{JA}	417	℃/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	300	℃

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = 25℃.

Characteristic		Symbol	CMT2N7002K			
			Min	Typ	Max	Units
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 10 μA)		$V_{(BR)DSS}$		60		V
Drain-Source Leakage Current		I_{DSS}				
(V_{DS} = 60 V, V_{GS} = 0 V)					1.0	μA
(V_{DS} = 60 V, V_{GS} = 0 V, T_J = 125℃)					0.5	mA
Gate-Source Leakage Current-Forward (V_{gsf} = 15 V)		I_{GSSF}			1.0	μA
Gate-Source Leakage Current-Reverse (V_{gsf} = -15 V)		I_{GSSF}			-1.0	μA
Gate Threshold Voltage * (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$		1.0	2.5	V
On-State Drain Current (V_{DS} ≧ 2.0 $V_{DS(on)}$, V_{GS} = 10V)		$I_{d(on)}$		500		mA
Static Drain-Source On-Resistance *		$R_{DS(on)}$				Ω
(V_{GS} = 10 V, I_D = 0.5A)					7.5	
(V_{GS} = 10 V, I_D = 0.5A, T_J = 125℃)					13.5	
(V_{GS} = 5.0 V, I_D = 50mA)					7.5	
(V_{GS} = 5.0 V, I_D = 50mA, T_J = 125℃)					13.5	
Drain-Source On-Voltage *		$V_{DS(on)}$				V
(V_{GS} = 10 V, I_D = 0.5A)					3.75	
(V_{GS} = 5.0 V, I_D = 50mA)					0.375	
Forward Transconductance (V_{DS} ≧ 2.0 $V_{DS(on)}$, I_D = 200mA) *		g_{FS}		80		mmhos
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}			50	pF
Output Capacitance		C_{oss}			25	pF
Reverse Transfer Capacitance		C_{rss}			5.0	pF
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 500 mA,	$t_{d(on)}$			20	ns
Turn-Off Delay Time	V_{gen} = 10 V, R_G = 25Ω, R_L = 50Ω) *	$t_{d(off)}$			40	ns
Diode Forward On-Voltage (IS = 115 mA, VGS = 0V)		V_{SD}			-1.5	V
Source Current Continuous (Body Diode)		I_S			-115	mA
Source Current Pulsed		I_{SM}			-800	mA

* Pulse Test: Pulse Width ≦300μs, Duty Cycle ≦2%

TYPICAL ELECTRICAL CHARACTERISTICS

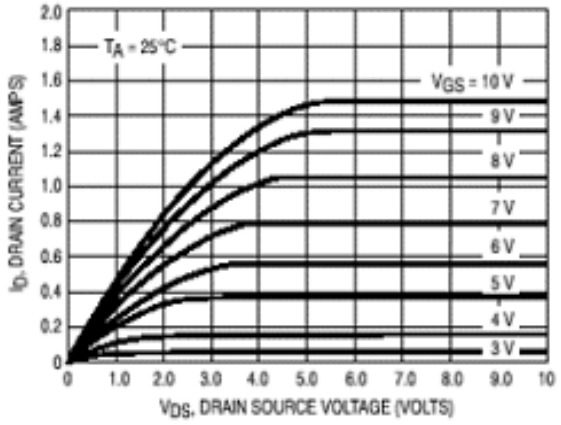


Figure 1. Ohmic Region

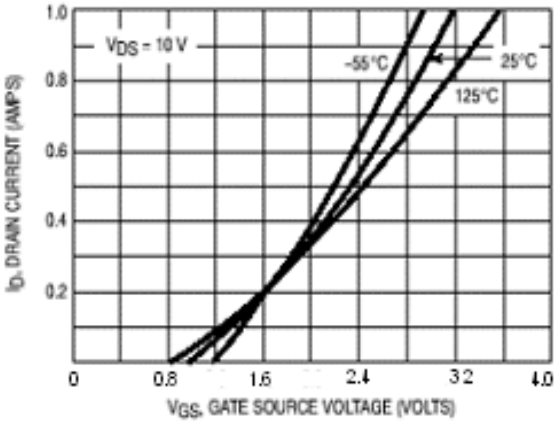


Figure 2. Transfer Characteristics

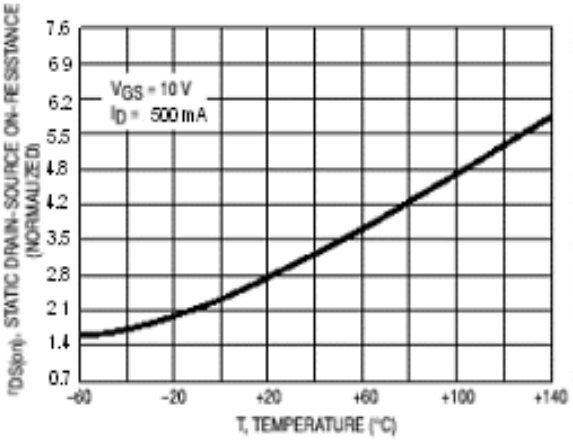


Figure 3. Temperature versus Static Drain–Source On–Resistance

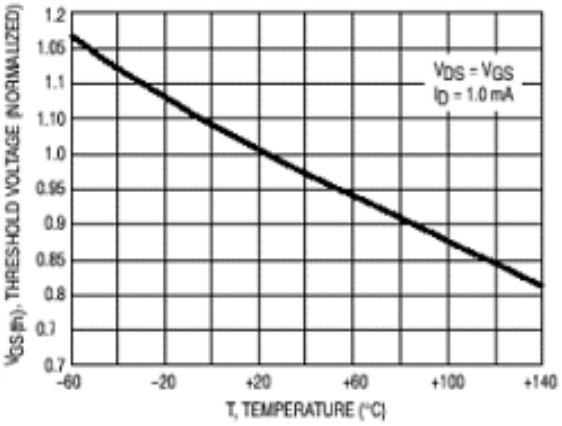


Figure 4. Temperature versus Gate Threshold Voltage

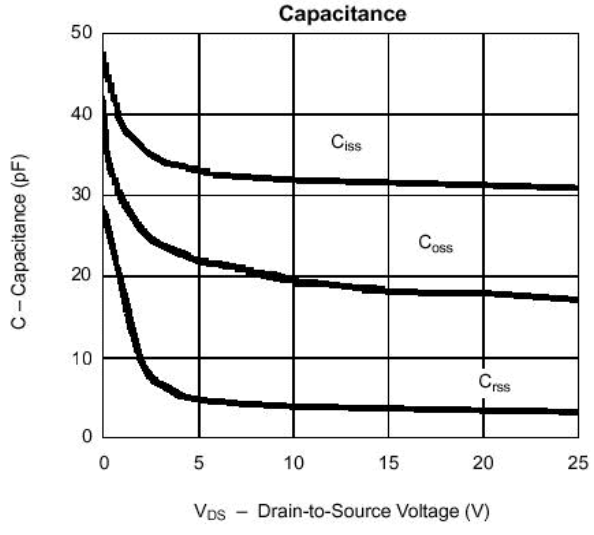
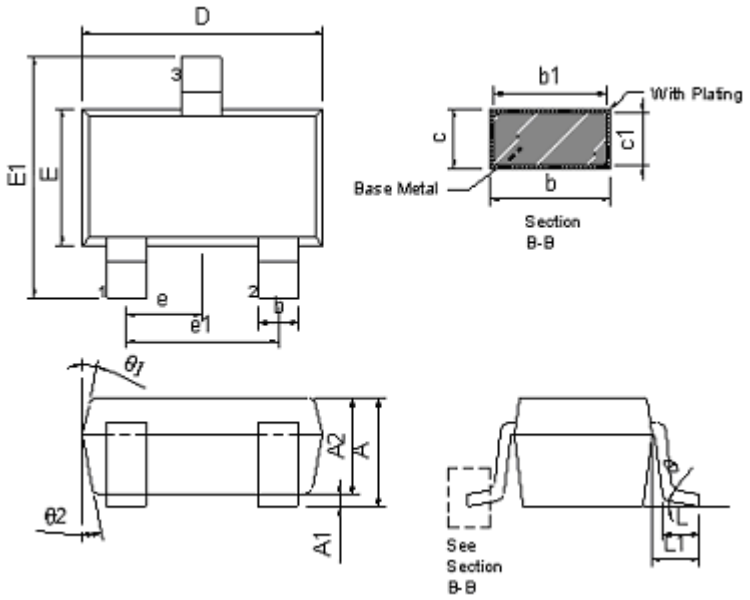


Figure 5. Capacitance

PACKAGE DIMENSION

SOT-23



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°

IMPORTANT NOTICE

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