Bias Flyback Design

There is a requirement in this digital DC-DC converter to supply auxiliary power. The dsPIC requires 3.3V and the gate drivers require 12V. The dsPIC device must have power supplied to it prior to start-up of the supply. The scheme to accomplish this is to utilize an analog converter, not only for start-up, but for continuous operation. This avoids possible glitches or uncontrolled operation events during abnormal operation or unanticipated transient conditions. The analog controller itself will require a boot strap supply once it has gone through soft-start. It has been empirically determined that the auxiliary power will range from 4-6.5W. In the power calculations for the analog bias supply we have assumed a worst case needed power of 7.4W.

$Pconv := 7.4$

The analysis that follows is that of the flyback transformer design required to serve this bias power need.

The input voltage range will be that of the DC-DC converter itself, namely 36-72 Vin. We perform our analysis at the minimum input voltage:

$Vin := 36$

We establish the nominal operating frequency of the IC as 250 KHz:

$Fsw := 250 \cdot 10^{3}$ $\quad Tp := \frac{1}{Fsw}$ $\quad Tp = 4 \times 10^{-6}$

The dsPIC requires 3.3V and we interpose a linear regulator in advance of that so the headroom required at one output is ~4V. In our analysis we reflect all loads into [1] 12V output:

$Vout := 12.0$

We will assume an overall efficiency of 80%:

$Eff := .80$

With Output Current reflected into [1] 12V Output, we get:

$Iout := \frac{Pconv}{Vout}$ $\quad Iout = 0.617$

The iteration process in flyback design begins with some choices/assumptions regarding primary magnetizing current and secondary to primary turn ratio. In this design we used:

$Np := .375$

$Lm := 42 \cdot 10^{-6}$

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However, keep in mind that these choices will change based on our iteration.

The factors we are assessing in the design based on these assumptions are peak current, duty cycle, DCM vs CCM operation and the ability to resolve the turn ratio into integer turns.

Based on our choices we arrive at a peak current of:

$Imax = 1.355$

And a minimum current of:

$Imin = 0$

……ensuring DCM operation

Our on time is calculated as:

$$Ton := \frac{Lm \cdot (Imax - Imin)}{Vin} \qquad Ton = 1.581 \times 10^{-6}$$

…. With ensuing duty cycle of ~ 40%:

$$D := Ton \cdot Fsw \qquad D = 0.395$$

Since this is a flyback transformer (coupled inductor), the secondary inductance values is:

$$L_{sec} := Ns^2 \cdot Lm \qquad L_{sec} = 5.906 \times 10^{-6}$$

The resulting off time can be calculated as:

$$Toff := L_{sec} \cdot \frac{\frac{1}{Np} \cdot (Imax - Imin)}{Vout} \qquad Toff = 1.779 \times 10^{-6}$$

… and thus our dead time:

$$Tdead := Tp - Ton - Toff \qquad Tdead = 6.396 \times 10^{-7}$$

… ensuring DCM operation.

Check Vout

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$$Vo := Vin \cdot \left(\frac{Ton}{Toff} \right) \cdot (Np) \qquad Vo = 12$$

Now we need to determine the integer turns to use and the core upon which to place them.

This also is an iterative process but helped immensely by using the following equations.

Let's assume 16T to be used for the primary.

$$Np\_integer := 16$$

Solving for the required number of secondary turns:

$$Ns\_integer := ceil(Np \cdot Np\_integer) \qquad Ns\_integer = 6$$

Checking:

$$V_o := Vin \cdot \left(\frac{Ton}{Toff} \right) \cdot \left(\frac{Ns\_integer}{Np\_integer} \right) \qquad V_o = 12$$

Then, for the 4V output we have:

$$Vdesired := 4$$

$$Ndesired := \frac{Ns\_integer \cdot Vdesired}{V_o} \qquad Ndesired = 2$$

SO set the turns to 2T.

$$Nconv4 := 2$$

Checking:

$$Vo\_conv4 := V_o \cdot \left(\frac{Nconv4}{Ns\_integer} \right) \qquad Vo\_conv4 = 4$$

We arrive at the transformer schematic then for this device:

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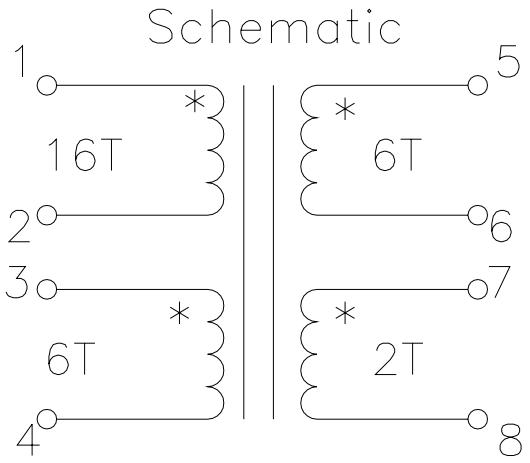
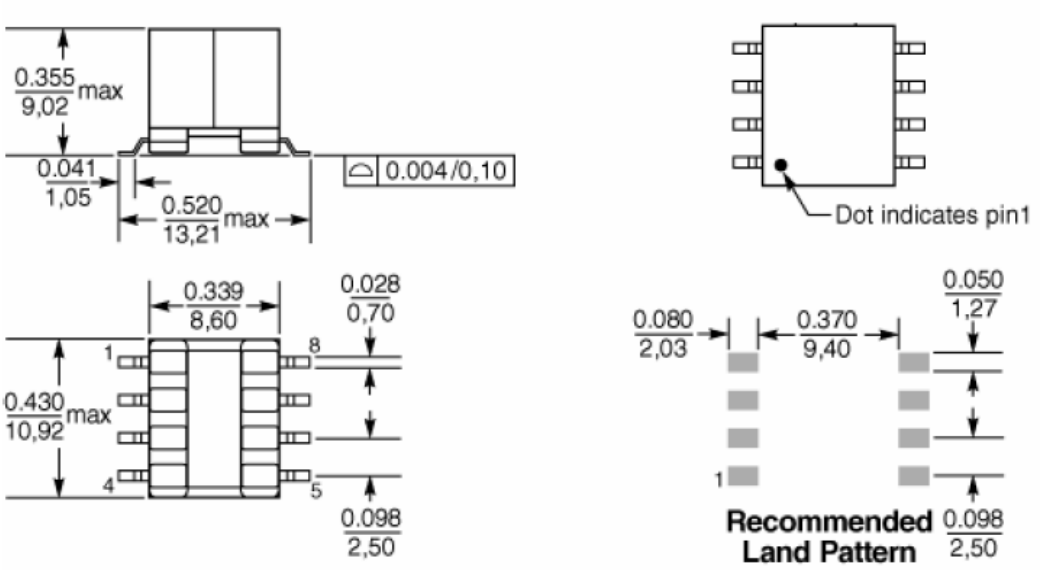


Now we must convert this into a practical design.

We have some practical guidelines from 2-7W flyback designs used as stand-alone devices for bias an PoE applications.

A 7W design in regular use is as follows:



The problem in this case is the 9mm height. This will need to reside either on the top or bottom surface. We have an overall height of <10mm for the entire converter. The multilayer pcb used as the embedded structure requires a nominal 4mm thickness. That leaves a maximum of 3mm height left for the bias flyback transformer.

Another possibility considered was the following:

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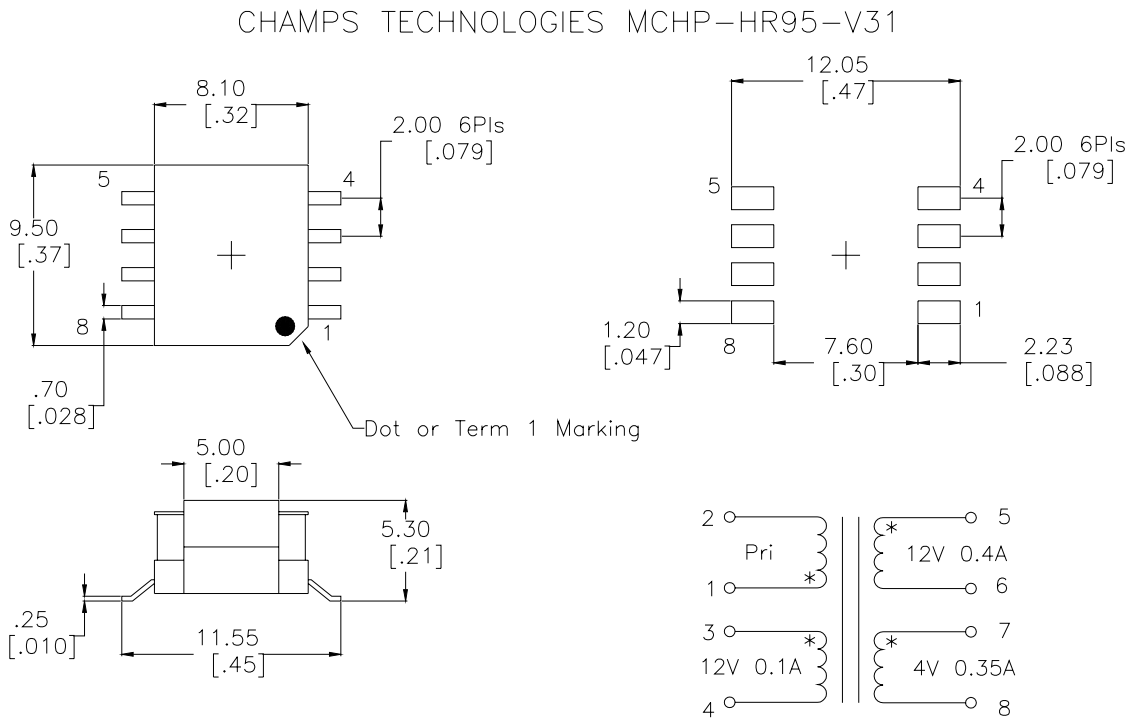

This also failed in that the maximum height was still 5.5mm and operation was marginal at 85C and our maximum power requirement of 7.4W.

It was decided to embed this magnetic also which would also save on BOM component costs since we would be implementing the primary and secondary windings as pcb traces within the multi-layer pcb.

To embed a magnetic the core window must accommodate the pcb thickness.

When we undertook the design and pcb layout we arrived at the following footprint:

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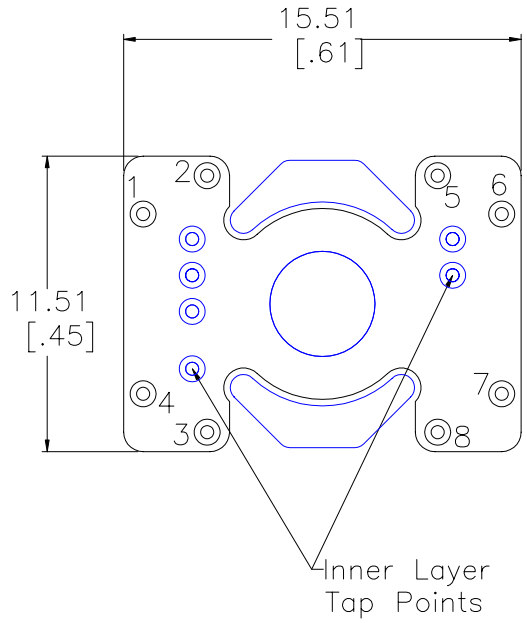

This was very encouraging since the length x width or footprint of the device was not too much greater than what a stand-alone magnetic device would be. Indeed, the footprint shown above was further reduce in the final implementation and thus we were able to implement the entire bias converter as part of the embedded design.

We then proceed to calculate the required center post air gap based on the formula:

$$L_{gap} := \frac{.4 \cdot \pi \cdot N_{pri}^{2} \cdot A_e \cdot 10^{-8}}{L_{reqd}} \cdot FFF \qquad L_{gap} = 0.012 \ \text{(cm)}$$

$$L_{gap\_in} := \frac{L_{gap}}{2.54} \qquad L_{gap\_in} = 4.591 \times 10^{-3} \ \text{(in)}$$

This works out to a required Al value to be submitted to the core gapper of:

$$A_l := \frac{L_{reqd} \cdot 10^{9}}{N_{pri}^{2}} \qquad A_l = 164.063$$

We check that at our peak current we are not saturating at 85C ambient:

$$B_{pk} := \frac{.4 \cdot \pi \cdot N_{pri} \cdot i_{pk}}{L_{gap}} \qquad B_{pk} = 2.337 \times 10^{3}$$

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We check that we are delivering the required maximum output power for DCM operation, factoring in efficiency:

$$Po := \frac{1}{2} \cdot L_{reqd} \cdot Imax^2 \cdot Fsw \qquad Po = 9.646$$

…. and we check that we derive the required induced voltage across the primary of the transformer:

$$V_{in} := L_{reqd} \cdot \left(\frac{di}{dt} \right) \qquad V_{in} = 36$$

We can now calculate RMS flux density:

$$B_{rms} := \sqrt{\frac{1}{Tp} \cdot \int_0^{t_{on}} \left[\frac{\left(V_{in} \cdot t_{on} \right) \cdot 10^8}{2 \cdot N_{pri} \cdot A_e} \right]^2 dTp} \qquad B_{rms} = 771.454$$

The only efficiency penalty in using a digital controller is the bias supply efficiency of 80% and the power draw of the dsPIC itself. All converters will share approximately the same FET driver loss. We saw that the footprint of the device as embedded was only slightly larger than typical stand-alone magnetic devices used for this same purpose.

The only further penalty is the footprint or space occupied by the bias supply within the available outline package of the converter itself. The main advantage as discussed at the outset is that the controller is “always on”, that is, it supplies power in a controlled fashion and rides out abnormalities and transients that might at the least require hiccup start-up for an analog controller.

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