Chelsio Communications
Accelerate

Chelsio Terminator Core IP

High Performance Converged Ethernet Interface Engine

Specifications

- High performance packet and protocol processor with complete software suite
- Multiple Ethernet ports
- Configurable port speed 1/10/25/40/50Gb
- ACE system bus interface
- Optional ccNUMA controller
- Complete stateless offload suite
  - IPv4/IPv6
  - TCP/UDP
- Complete full offload suite
  - TCP and UDP with zero copy
  - RDMA
  - iSCSI
  - FCoE
- Flexible DMA engine
- Cut-through design
  - Low memory usage
  - Ultra low latency
- Flexible I/O virtualization support
  - Network virtualization tagging
  - Independent virtual interfaces
- Optional integrated edge switch
  - SDN and OpenFlow
  - L2/VLAN and L3/L4/L7 rules
- Network Function Virtualization
- Hardware Traffic management and QoS

Applications

- General networking
- Storage networking
- High performance computing
- Network convergence
- Distributed systems
- Web 2.0 cloud installations
- Virtualization and multi-tenant clouds
- Traffic monitoring and network security
- WAN optimization

Advantages

- Low risk, silicon proven IP
- Performance leadership
  - High bandwidth
  - High packet processing rate
  - Low latency
- Comprehensive feature set
- Highly efficient in area and power
- Complete software suite
  - Windows, FreeBSD, Linux

Chelsio's Terminator Core IP is a configurable, high performance Ethernet packet processing engine with a full suite of software, suitable for a wide range of SoC network connectivity solutions. At the heart of the Terminator line of silicon proven Network Interface Card (NIC) controllers, Chelsio's Core architecture is designed for low latency, high capacity cut-through processing, minimum cycles per byte (CPB) and maximum memory efficiency.

Terminator Core is the culmination of more than a decade of expertise with high performance network protocol implementation, and five generations of field proven designs. It offers support for a complete suite of storage and high performance computing networking protocols. Integrating the Core in an SoC design provides a drop-in server grade Ethernet managed and hyper-virtualized network controller. An optional edge switch component provides flexible packet replication and switching, with access control support, and an optional ccNUMA controller allows native integration within the SoC memory subsystem.

Unified Wire Convergence

The Terminator Core can be configured to offload a comprehensive set of networking, storage and compute protocols, including a complete list of stateless server adapter features including:

- Large Send Offload (LSO) and Large Receive Offload (LRO)
- Checksum offloads for TCP/UDP over IPv4/IPv6
- CRC offloads for RDMA, FCoE and iSCSI
- Load balancing – RSS
- Drop/Steer/Route filters and NAT offload
- NVGRE/VXLAN/GENEVE offload
- Timestamping, sniffing, tracing and other NFV features

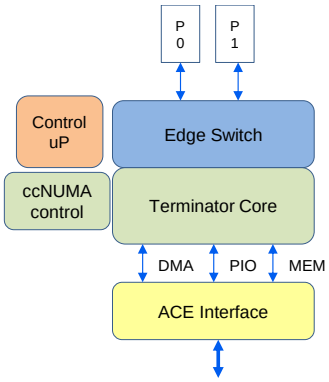
The Core can also be configured to support one or more of the stateful offloads:

- iSCSI – PDU and full offload with T10-DIX
- FCoE – PDU and full offload with T10-DIX
- iWARP RDMA over Ethernet
- TCP/IP and UDP/IP sockets

With multiple high speed port connectivity and ultra-low latency, the Terminator Core eliminates bottlenecks that impede the scalability of SoC based distributed system architectures and cloud installations.

Terminator Core Architecture

The Terminator architecture is a proven 5th generation design with superior scalability and performance characteristics. The architecture easily scales from 1Gbps to 50Gbps speeds, and at 1Gbps per 8MHz is highly power and clock rate efficient. It centers on a proprietary, deeply pipelined programmable data-flow processor, designed from the ground up for cut-through processing, without access to external memory. The unique architecture is protected by more than 25 patents covering the design, features and operation of the Terminator Core.



Core Interfaces

The Terminator Core architecture is highly integrated with a single system bus interface such as ACE on the host side, and one or more Ethernet ports on the network side. The system interface is used for both system memory access and the Core memory access. Optionally, a cache coherent directory based NUMA controller can be added that extends SoC cache coherence to multiple nodes.

The Core can also be configured to utilize system memory to scale full offload protocols and flow state support.

The optional embedded edge switch allows forwarding traffic from host-to-host side, enabling v-switch offload in virtualized environments and from wire-to-wire port on the network side. The switch is SDN/OpenFlow compatible, and supports forwarding traffic based on L2-7 rules, providing switching, routing and application payload proxy functionality. The Core supports up to 1M matching rules and more than 200K updates/sec. It also implements header rewrite capabilities, which enable advanced functionality such as Network Address Translation (NAT) offload and Intrusion Detection Services (IDS).

A control processor module runs the Core firmware component, which handles the control path and management functions.

Software Support

Chelsio's line of adapters benefits from a complete suite of drivers and software for all the major operating systems, and has been deployed in storage and high performance networking solutions.

Configuration Options

The Core IP can be configured with the following options:

- Multiple Ethernet side interfaces
- Connection capacity: 32 up to 1M
- Link speeds: 1G, 10G, 25G, 40G and 50G
- Embedded edge switch
- Protocol offload capabilities

Ordering Information

CORE-IP-ACE-2X1G	**– Core IP with two 1G interfaces**
CORE-IP- ACE-2X10G	**– Core IP with two 10G interfaces**
CORE-IP- ACE-2X25G	**– Core IP with two 25G /10G interfaces**
CORE-IP- ACE-2X40G	**– Core IP with two 40G interfaces**
CORE-IP- ACE-2x50G	**-- Core IP with two 50G interfaces**
Add EVB	**– Embedded edge switch for Core IP**
Add ccNUMA	**- ccNUMA controller**

Key Statistics

- High packet pipeline processing capacity
- Less than 800nsec latency at 500MHz for full (TX+RX) processing path
- Single pipelined engine design
- No dependency on traffic pattern
- No dependency on number of connections
- Microcode and Firmware programmable
- Edge switch with 140 virtual interfaces and broadcast/multicast support
- v-switch at line rate with up to 1M matching rules supporting more than 200K updates/sec

Firmware

- Single firmware image for all protocols
- Open interfaces for adding support for different physical interfaces

Solution

- Encrypted Core IP
- Verification environment
- FPGA SDK
- Integration guide
- Terminator data book
- Firmware interface specifications
- Register set specifications
- Software drivers

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