

■ Features, Benefits and Applications

- 30 standard frequencies from 1.544 MHz to 49.152 MHz
- 100% pin-to-pin drop-in replacement to quartz based VCXO
- Wide pull range options: ± 50 , ± 100 , ± 150 , ± 200
- Superior pull range linearity of $\leq 1\%$, 10 times better than quartz
- LVCMOS/LVTTL compatible output
- Three industry-standard packages: 3.2 mm x 2.5 mm (4-pin), 5.0 mm x 3.2 mm (6-pin), 7.0 mm x 5.0 mm (6-pin)
- Outstanding silicon reliability of 2 FIT (10x improvement over quartz-based devices)
- Ultra short lead time
- Ideal for telecom clock synchronization, instrumentation, low bandwidth analog PLL, jitter cleaner, clock recovery, audio, video, FPGA, broadband and networking

■ Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1.544	–	49.152	MHz	Refer to the supported frequency list on page 5
Frequency Stability	F_stab	-25	–	+25	PPM	Inclusive of Initial tolerance ^[1] at 25 °C, operating temperature, rated supply voltage variation and load variation (15% pF $\pm 10\%$)
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	Contact SiTime for any other voltage support between 2.5V and 3.3V
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Pull Range ^[2,3]	PR	± 50 , ± 100 , ± 150 , ± 200			PPM	
Upper Control Voltage	VC_U	1.7	–	–	V	Vdd = 1.8 V, Voltage at which maximum deviation is guaranteed.
		2.4	–	–	V	Vdd = 2.5 V, Voltage at which maximum deviation is guaranteed.
		2.7	–	–	V	Vdd = 2.8 V, Voltage at which maximum deviation is guaranteed.
		3.2	–	–	V	Vdd = 3.3 V, Voltage at which maximum deviation is guaranteed.
Lower Control Voltage	VC_L	–	–	0.1	V	Voltage at which minimum deviation is guaranteed.
Control Voltage Input Impedance	Z_vin	100	–	–	k Ω	For the voltage control pin
Linearity	Lin	–	0.1	1	%	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage Bandwidth(-3dB)	V_BW	–	8	–	kHz	Contact SiTime for 16 kHz and other high bandwidth options
Current Consumption	Idd	–	31	33	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	29	31	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	–	70	μ A	All Vdds, $\overline{ST} = \text{GND}$, output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.5	2	ns	Vdd = 1.8, 2.5, 2.8 or 3.3 V, 10% - 90% Vdd level
Output Voltage High	VOH	90%	–	–	Vdd	OH = -7 mA, IOL = 7 mA, (Vdd = 3.3 V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8 V)
Input Pull-up Impedance	Z_in	–	100	250	k Ω	For the OE/ \overline{ST} pin if available
Start-up Time	T_start	–	6	10	ms	
OE Enable/Disable Time	T_oe	–	–	150	ns	f=80 MHz, all Vdds. For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	–	10	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	1.5	2	ps	f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	2	3	ps	f = 75 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.5	1	ps	f = 75 MHz, Integration bandwidth = 12 Mhz to 20 MHz, all Vdds
Aging	F_aging	–	–	± 5	PPM	10 years

Notes:

1. Initial tolerance is measure at Vin = Vdd/2
2. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage
3. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)
4. All electrical specifications in the above table are measured with 15pF output load, unless stated otherwise in the Condition, Contact SiTime for higher drive options.

■ Specifications (Cont.)

Pin Description Tables (4-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change

Pin Map	
Pin	Connection
1	VIN
2	GND
3	CLK
4	Vdd

Pin Description Tables (6-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change
Pin #2 Functionality
NC
H or L or Open: No effect on output frequency or other device functions
OE
H or Open ^[5] : specified frequency output
L: output is high impedance. Only output driver is disabled.
ST
H or Open: specified frequency output
L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I _{std}

Pin Map	
Pin	Connection
1	VIN
2	OE/ $\overline{\text{ST}}$
3	GND
4	CLK
5	NC
6	Vdd

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	6000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, Vdd (0 to 3.65 V)	1,000+	–	years

Environmental Compliance

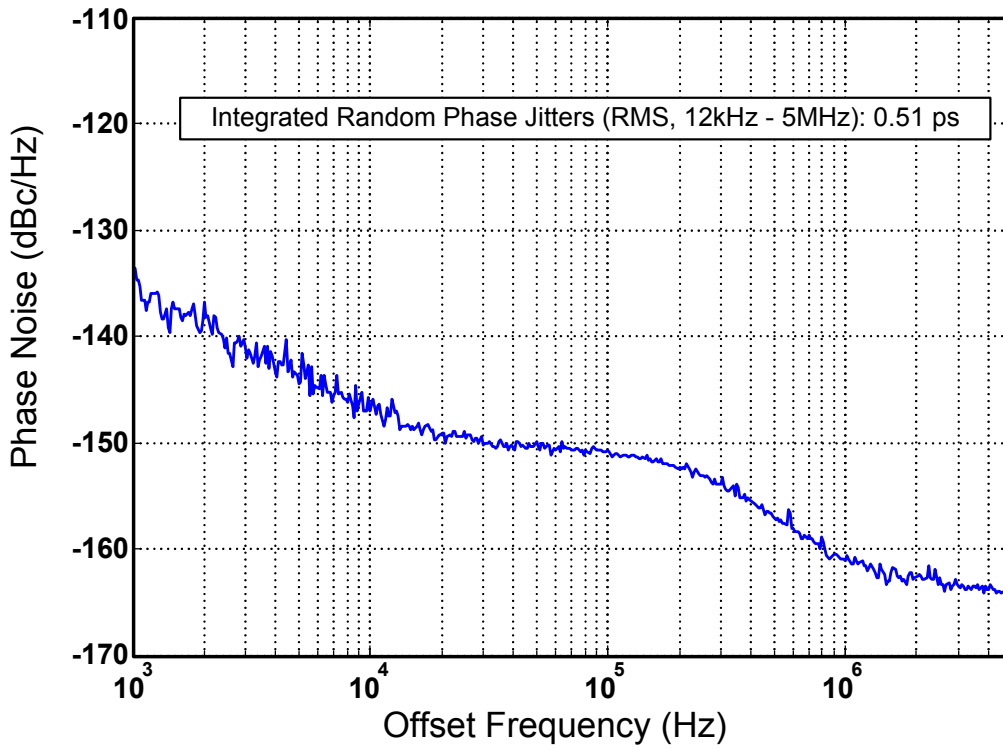
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002; 50kG
Mechanical Vibration	MIL-STD-883F, Method 2007; 70G
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

Notes:

5. A resistor of <100 kΩ between OE/ $\overline{\text{ST}}$ pin and VDD is recommended for all voltages.

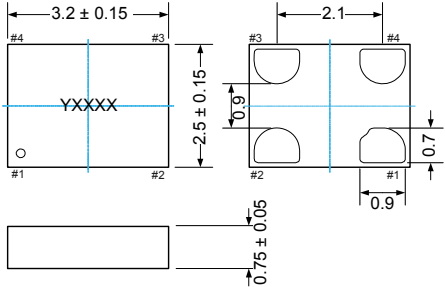
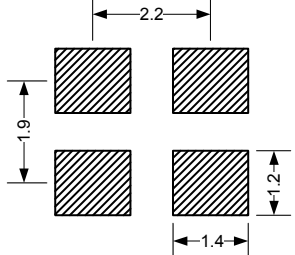
Phase Noise Plot

SiT3807, 10MHz, Pull range ± 100 ppm, 3.3V, LVCMOS output

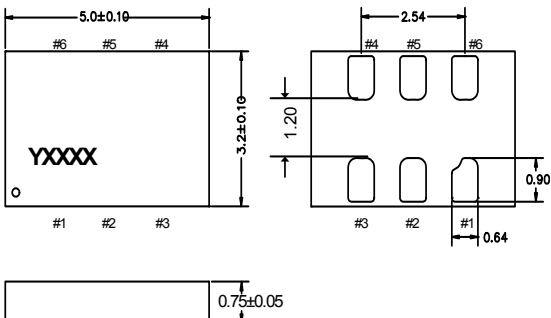
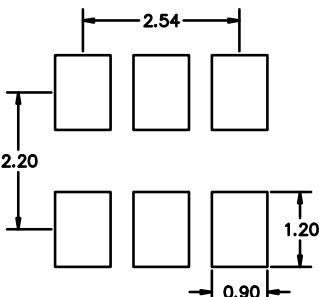
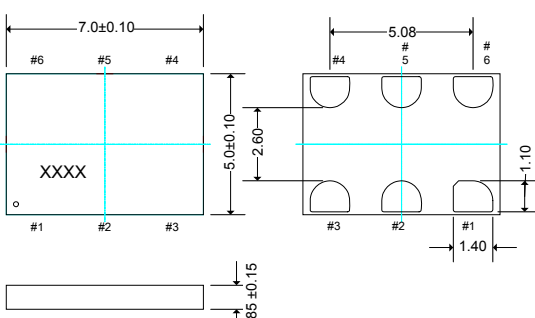
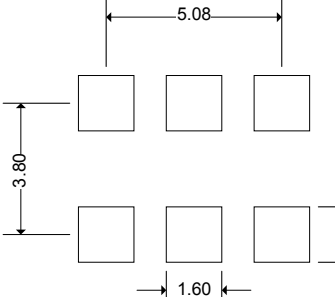


■ Dimensions and Land Patterns

Packages (4-pin device)

Package Size – Dimensions (Unit: mm) ^[6]	Recommended Land Pattern (Unit: mm) ^[7]
<p>3.2 x 2.5 x 0.75 mm</p>  <p>The diagram shows the package dimensions and the recommended land pattern for a 4-pin device. The package size is 3.2 x 2.5 x 0.75 mm. The top view shows a rectangular package with pins #1, #2, #3, and #4. The top marking is YXXXX. The dimensions are: total width 3.2 ± 0.15 mm, total height 2.5 ± 0.15 mm, pin pitch 2.1 mm, pin width 0.9 mm, pin height 0.7 mm, and package thickness 0.75 ± 0.05 mm. The recommended land pattern shows a 2x2 grid of pads with dimensions: pad width 2.2 mm, pad height 1.9 mm, pad spacing 1.4 mm, and pad thickness 1.2 mm.</p>	 <p>The recommended land pattern for the 4-pin package is a 2x2 grid of pads. The dimensions are: pad width 2.2 mm, pad height 1.9 mm, pad spacing 1.4 mm, and pad thickness 1.2 mm.</p>

Packages (6-pin device)

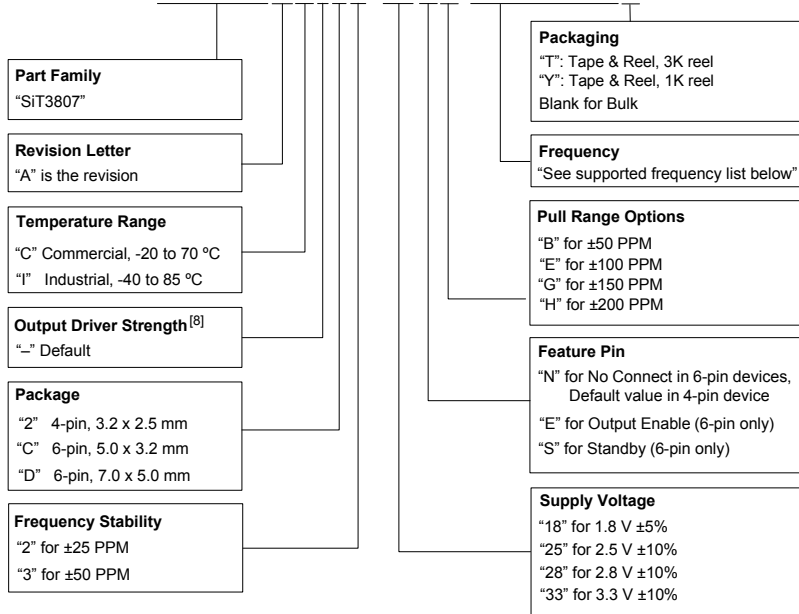
Package Size – Dimensions (Unit: mm) ^[6]	Recommended Land Pattern (Unit: mm) ^[7]
<p>5.0 x 3.2 x 0.75 mm</p>  <p>The diagram shows the package dimensions and the recommended land pattern for a 6-pin device. The package size is 5.0 x 3.2 x 0.75 mm. The top view shows a rectangular package with pins #1, #2, #3, #4, #5, and #6. The top marking is YXXXX. The dimensions are: total width 5.0 ± 0.10 mm, total height 3.2 ± 0.10 mm, pin pitch 2.54 mm, pin width 0.64 mm, pin height 0.90 mm, and package thickness 0.75 ± 0.05 mm. The recommended land pattern shows a 2x3 grid of pads with dimensions: pad width 2.54 mm, pad height 2.20 mm, pad spacing 0.90 mm, and pad thickness 1.20 mm.</p>	 <p>The recommended land pattern for the 6-pin package is a 2x3 grid of pads. The dimensions are: pad width 2.54 mm, pad height 2.20 mm, pad spacing 0.90 mm, and pad thickness 1.20 mm.</p>
<p>7.0 x 5.0 x 0.90 mm</p>  <p>The diagram shows the package dimensions and the recommended land pattern for a 6-pin device. The package size is 7.0 x 5.0 x 0.90 mm. The top view shows a rectangular package with pins #1, #2, #3, #4, #5, and #6. The top marking is XXXXX. The dimensions are: total width 7.0 ± 0.10 mm, total height 5.0 ± 0.10 mm, pin pitch 5.08 mm, pin width 1.40 mm, pin height 1.10 mm, and package thickness 0.85 ± 0.15 mm. The recommended land pattern shows a 2x3 grid of pads with dimensions: pad width 5.08 mm, pad height 3.80 mm, pad spacing 1.60 mm, and pad thickness 1.10 mm.</p>	 <p>The recommended land pattern for the 6-pin package is a 2x3 grid of pads. The dimensions are: pad width 5.08 mm, pad height 3.80 mm, pad spacing 1.60 mm, and pad thickness 1.10 mm.</p>

Notes:

6. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
7. A capacitor of value 0.1 μF between Vdd and GND is recommended.

■ Part No. Guide - How to Order

SiT3807AC-2F-33EH-10.000000T



Supported Frequencies

1.544000 MHz	4.096000 MHz	6.176000 MHz	8.000000 MHz	8.192000 MHz	10.000000 MHz	11.289600 MHz	12.288000 MHz	12.352000 MHz
13.500000 MHz	16.000000 MHz	16.348000 MHz	16.8 MHz	19.440000 MHz	20.000000 MHz	24.576000 MHz	24.700000 MHz	25.000000 MHz
25.576000 MHz	27.000000 MHz	30.000000 MHz	31.720000 MHz	32.000000 MHz	32.768000 MHz	35.328000 MHz	38.880000 MHz	39.322000 MHz
40.000000 MHz	44.736000 MHz	49.152000 MHz						

APR Definition

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_{stab}) - Aging (F_{aging})

APR Table

Nominal Pull Range	Frequency Stability	
	± 25	±50
	APR (PPM)	
± 50	± 20	—
± 100	± 70	± 45
± 150	± 120	± 95
± 200	± 170	± 145

Note:

8. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.

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