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RF & Microwave Systems

IMS 2011 SPECIAL ISSUE

NOBLE AWARD HONORS SILICON ON SAPPHIRE FOUNDERS

NEW DIRECTIONS IN RFIC AND MMIC

MEETING THE 3G/4G CHALLENGE

RETURN OF THE FEMTOCELL

RF LOSES ITS MYSTERY

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AT THE FRONTIERS OF SIMULATION
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2011

RF & Microwave Systems

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Top Stories and News

- **Editorial: Turn Up the Heat with an Electrical-Thermal MMIC Design Flow**
  AWR and CapeSym provide high-power RF designers with an integrated tool to optimize electrical performance and thermal operating properties.
- **Editorial: The Race is on for RF MEMS**
- **Atmel New Evaluation Kits Target Wireless ZigBee PRO and RF4CE Applications**
- **Vivante GPU IP Cores Power the Latest Freescale i.MX 6 Series of Application Processors**
- **Lattice MachXO2 Pico Development Kit Simplifies Consumer Applications**
- **EU Sets Ground Rules for Rural 4G Broadband**
- **Broadcom moves on to top 10 list as 2010 semi revenue records more than 30% growth**
- **Expanded Student Competitions at IMS2011 in Baltimore Attract More Collegiate Talent than Ever Before**
- **More Than 1 Billion Devices to Have Embedded Wireless Networking Capability in 2011**

Featured Articles

- **Editorial: RFICs and MMICs Forge New Paths**
  The ability to hit Terahz speeds has created new applications for body and security imaging, as well as for ultrahigh speed secure data communication.
- **RFIC Complexity Demands an Advanced RF Analysis and Design Environment**
  It is possible to enable first-pass silicon realization for RFICs.
- **Meeting the 3G-4G Challenge**
  Maintaining Profitability in the Mobile Backhaul Through Ethernet
- **Return Of The Femtocell**
  Nothing has been left untouched in the current global economic downturn, and that includes femtocell deployments. It was just last year that femtocells were being proclaimed
- **Keeping Up With Complexity**
  The gap between abstraction and granularity is impossible to close if you can't do more exploration throughout the flow.
- **Differentiation and Co-existence in WiMax and LTE**
  Plenty of Opportunities for Differentiation and Co-existence in WiMax and LTE Designs
- **RF-Microwave Advances Heighten Power Consumption Concerns**
  LTE Advanced, much more computationally intensive than the current version, will require designs that reign in power consumption from the base station to the handset.
- **Your Light Bulb Is Calling**
  RF integration into SOCs and design of Smart Sensor Systems leads to projects such as HP's CeNSE (Central Nervous System for the Earth) project.
- **TI Buy Brings "Benefits of Scale" to National**
  Texas Instruments will seek to boost revenue growth rates after its acquisition of National Semiconductor is finalized, said TI CEO Richard Templeton. "We are not consolidating. We looked at (National's) revenue growth over the last two years, and realized that we could get those rates growing faster."
- **Creating a comfortable workspace for high-speed digital designers**
  Increased RF effects in the digital realm and more digital circuitry encroaching on the antenna requires greater emphasis on flexible simulation and measurement techniques.

more articles

From the Blogosphere

- **"Translator by Moth"**
  updated for v1.2 This article serves as the manual for the free Windows Phone 7 app called "Translator by Moth". The app is available from the following link (browse the link on your Window Phone 7 phone, or from your PC with zune software installed) http://social.zune.net/redirect?type=phoneApp&id=bcd09f8e-6211-e011-9264-00237de2db9e ...
  The Moth
- **Comment on Happy Birthday, Maurice Goldhaber by Fernando**

Blogs

Discourse on Embedded Signal Processing

ADI Offering Discounts on Blackfin Development Tools

Analog Devices is offering up to 60% discount off the cost of it's Blackfin development tools until...

Jill's Circuit

Impossible Astronaut and Supercomputers in the Desert

The premier of a science fiction favorite and the start of a supercomputing competition all take place...

Editor's Note

Hot Potatoes

Matching hardware to software, and software to hardware, is an interesting discussion. It's also one...

Koby's Kaos

Tarpits on the Moon

Our author finds himself stuck fast in the future...

RF & Microwave Systems Tech Videos

Broadcom Delivers 1000x Bandwidth t

Edward Doe
Broadcom Product Line Director

0:00 / 1:40

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500+ vendors of Microwave, RF, Test & Measurement products, and more!

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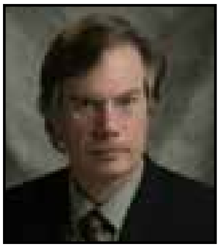
- **Wireless Backhaul Video**
  Switch brings increased bandwidth to 4G Mobile Networks

By John Blyler, Editor-in-Chief

New Publication Covers RFICs and MMICs



I'm excited to be once again covering the RF and microwave space. Writing for this important market is something that I've missed since the closure of Penton's Wireless Systems Design (WSD) magazine in 2004.

Since that time, much has happened in the world of wireless technology, especially in the area of semiconductor design, test and manufacturing. Many pundits have observed that the 1980s and 1990s were the decades of computing. In contrast, the 2000s and the 2010s have become the decades of wireless communications.

Today, I'm launching a new magazine and online site called "RF-Microwave Systems." The focus will be on the simulation, design, test and integration of RF and microwave subsystem at the IP, chip and package level. The print version of the publication will premiere at the IEEE-MTTS IMS event in June 2011.

Some have suggested that the RF and microwave space have too many publications. Others have noted that many of the existing publications are trying to cover too much, to be all things to all readers.

The decade of "all things wireless" needs coverage of specific simulation, design, integration and test issues facing RFIC and MMIC engineers and managers.

This is where the editors and publisher at Chip Design magazine are different. We are the only publication still dedicated to semiconductor development. We will bring that expertise to the emerging market of RFICs and MMICs. These devices are not only gaining importance in a wirelessly connected world, but they are also growing in complexity.

Today's communication trends in miniaturization, low power, mobility and ever-higher levels of performance have increased the demand for RF-microwave IC technology and coverage. Other factors driving these trends include tighter integration of RF and microwave front-ends with digital basebands, emerging IP subsystems, stacked dies on a single package, system-level modeling and increased analog integration - MEMS, sensors, ESD interposers and more - into CMOS.

I hope you'll join us as we cover the emerging wireless and telecommunication (LTE) markets for RFICs and MMICs devices. Please be sure to visit the online site for weekly updates, blogs, videos and more: www.chipdesignmag.com/rfmw Cheers – JB

John Blyler can be reached at: jblyler@extensionmedia.com

On behalf of the IMS2011 Steering Committee, I have the privilege of inviting you to IMS2011. I hope I will have the honor of welcoming you in Baltimore June 5th through 10th 2011 for the world's premiere technical conference on all things related to RF, microwave, and millimeter-wave technologies. Our theme for IMS2011 is Microwaves for the World. We will have technical sessions, panel sessions, workshops, and short courses on state-of-the-art technologies and techniques presented by leading experts from around the world. The emphasis will be on how our technology and profession has benefited the world.

Co-located with IMS2011 are the 2011 Radio-Frequency Integrated Circuits (RFIC) Symposium (www.rfic2011.org) and the 77th Automatic Radio-Frequency Techniques Group Conference (www.arftg.org). Of course, we also have the largest collection of exhibitors who showcase their products, equipment, expertise, and services. This opportunity for all members of our technical community to interact and network is what makes IMS and Microwave Week the unique experience that it is.

All registered attendees are encouraged to attend this year's Monday evening Plenary Session. The Keynote speaker, Professor J. David Rhodes, is known for his greater than 30-year involvement with microwave technology, his leadership in filter design and application, and his entrepreneurial achievements. His address is titled "Migration of WCDMA and 4G LTE into Existing Cellular Bands."

Microwaves for the World
IMS 2011 Baltimore

Our slogan this year is IMS2011 in Baltimore: A Perfect Match, which emphasizes in a way every microwave engineer can understand that Baltimore is an ideal IMS venue. The Baltimore Convention Center and major hotels are all within walking distance of the beautiful Inner Harbor. Baltimore makes a great destination for family and guests. And, in those rare instances when you need a break from IMS Technical and Social programs, you are sure to find something that interests you.

Our Steering Committee and colleagues at IEEE Meeting & Conference Management and MP Associates are committed to making this your best IMS experience ever.

See you in Baltimore,

Jeffrey M. Pond

THINGS TO NOTE FOR YOUR ULTIMATE MICROWAVE WEEK EXPERIENCE!

Registration

The Registration process is split into three tiers. The 1st tier is the Early Bird Registration period. It begins Tuesday, 1 February and will last through Friday, 20 May. This period provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird period is the 2nd tier or Advance Registration period. It extends from Saturday, 21 May through Friday, 3 June, just prior to the start of Microwave Week. The 3rd and final tier is the On-Site Registration period that will remain the same as in past Symposia, starting on Saturday 4 June, the first day of Microwave Week, and ending on Friday, 10 June.

For more information and to register visit http://ims2011.mtt.org/Registration/IMS_registration.html

RFIC Symposium

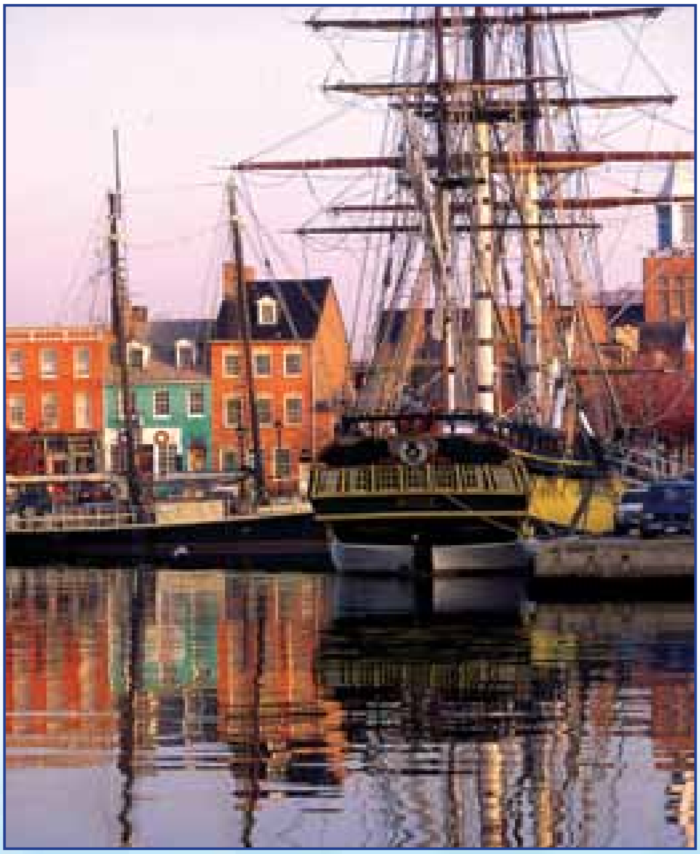
Running in conjunction with the International Microwave Symposium and Exhibit, the RFIC Symposium adds to the excitement of the Microwave Week with three days focused exclusively on RFIC technology and innovation.

The 2011 RFIC Symposium will start on Sunday, June 5, 2011 with half-day and full-day workshops covering a wide array of topics. Some of the topics include: New Architectures for Digitized Receivers, RFIC for Bio-Medical Applications, Imaging at mm-wave and beyond, Cognitive Radios and Spectrum Sensing, Advancements in Linear Power Amplifiers, Efficiency Enhancement Techniques for Power Amplifiers and Transmitters, Advancements and Challenges Toward Radio-in-package and Radio-on-chip, Re-configurability Requirements for Multi-standard, Low-Power Operation, and EMI compliant product design practices.

The conference also includes a Plenary Session, which is held on Sunday evening. Keynote addresses will be given by two renowned leaders from within the wireless industry. Both of them will share their views and insights on the direction and challenges that the RF IC design community is facing. The first speaker is the Chief Technical Officer and Co-Founder of Telegent Systems, Dr. Sam Sheng, who will discuss "RF Coexistence - Challenges and Opportunities." The second speaker is Mr. Ron Ruebusch, Vice President of R&D of Wireless Semiconductor Division of Avago Technologies. He will discuss "3G to 4G Transition – Challenges and Opportunities." In addition to the keynote addresses, the conference holds a student paper competition to encourage the publication of innovative research from university students. Consequently, best student paper awards are presented in the Plenary Session to acknowledge these contributions. The highly anticipated RFIC Reception will follow immediately after the Plenary Session, providing a relaxing time for all to mingle with old friends and catch up on the latest news.

On Monday and Tuesday, the conference will feature lunch-time panel sessions that traditionally draw strong debate between panel members as well as stimulating interaction between attendees and panelists. The Monday panel session is entitled "Software Defined Radios – Facts and Fantasies" while the Tuesday panel session is entitled "What is the limit of multi-radio integration... or rather, is it 'disintegration'?". Be sure to attend these lively and entertaining forums.

Technical papers will be presented during oral sessions throughout Monday and Tuesday. There will be a total of 130 papers presented in 23 technical focused sessions. On Tuesday's afternoon, our Interactive Forum session will feature poster sessions and give our attendee a chance to speak directly with authors regarding their work.



Monday IMS Plenary Session and Welcome Reception

The Plenary Session will be held Monday evening, 6 June 2011, in the Baltimore Convention Center beginning at 1740. All registered attendees are encouraged to hear Professor J. David Rhodes speak on "Migration of WCDMA and 4G LTE Into Existing Cellular Bands." The Welcome Reception will follow the Plenary Reception.

IMS Technical Sessions/Interactive Forum

The IMS2011 Technical Sessions will cover developments in microwave technology from nano-devices, RFID technologies, energy transmission through microwaves, magnetic resonance imaging (MRI) and many other system applications. To enhance interactivity, the technical papers are organized in to two 100 minute and two 80 minute sessions, leaving more than two hours for technical interaction at the lunch hour. The IMS Interactive Forum will include demonstrations, hardware, and simulations presented by authors. Authors will be available to discuss their work from 1200-1400 Wednesday and Thursday. All IMS Interactive Forum Sessions will be located in Exhibit Hall A.

Student Paper and Design Competitions

The Student Paper Competition Interactive Forum will be available from 1200-1400 in Exhibit Hall A on Tuesday along with the Student Design Competitions.

Panel Sessions

Panel Sessions present current opinions on hot topics. Order optional and convenient box lunches with your registration so you can keep up to date on the latest topics without skipping lunch!

Workshops & Short Courses

Workshops and Short Courses will be held Sunday, Monday and Friday of Microwave Week. The workshops will provide enhanced interactivity with significant and quality time spent on audience participation. Short courses were selected on the basis of both their instructional material as well as hands on exercises which should enhance the learning experience.

Crab Feast

IMS in Baltimore means it is Crab Feast time. It's an event not to be missed and will be held at the USS Constellation & Pier 1 on Thursday night at 1800.

MicroApps

Informative MicroApps seminars from vendors of products and services in the microwave industry will be presented daily in the MicroApps Theater. Do not miss the keynote talk by John Ocampo, Chairman of M/A-COM Technology Solutions, entitled "What Makes Successful Mergers," on Wednesday at 1700.

Exhibition

Don't miss this opportunity to meet and network with over 550 companies!

Exhibit hours have been scheduled to provide maximum interaction between conference attendees and exhibitor personnel:

Tuesday, 7 June	0900 to 1700
Wednesday, 8 June	0900 to 1800
Thursday, 9 June	0900 to 1500

Free Exhibit Only registration for Wednesday has returned. Come experience the many vendors and learn about recent advances within the Microwave industry. Be sure to be on the exhibit floor on Wednesday afternoon from 1715-1800 for the Industry Hosted Reception. Please come and visit as drinks and refreshments will be provided throughout the show floor.

Closing Reception

New for IMS2011 is a Closing Ceremony to be held Thursday afternoon between 1620 and 1720 in the Baltimore Convention Center. While enjoying some refreshments we will be privileged to hear Dr. Joseph Guerci speak on "Cognitive Radar". We will also be introducing the winners of the new Graduate Student Challenge, as well as the IMS2012 Steering Committee who will be enticing you with the great symposium they plan for Montreal in 2012.

ARFTG Conference

The ARFTG conference will be held on Friday, 10 June 2011 at the Hilton Baltimore Convention Center. The conference will include technical presentations, an interactive forum, and an exhibition; all to give you ample opportunity to interact with your colleagues in the RF and microwave test and measurement community. The conference theme is "Design and Measurement of Microwave Systems" and opens with an invited talk on the challenges and promises of modular microwave measurement systems. The contributed conference papers focus on nonlinear measurement systems, calibration issues, on-wafer measurements, uncertainty, broadband and millimeter-wave measurements, and other areas of RF and microwave measurement. Also, be sure to check out the joint ARFTG/IMS workshops on "Practical IMD, P1dB, Load Pull and Behavioral Modeling Measurements", "The Design Flow of Microwave Power Amplifiers: Challenges and Future Trends", and "Laboratory Class: Wafer-Level S-Parameter Calibration Techniques." An important part of any ARFTG Conference is the opportunity to interact one-on-one with colleagues, experts and vendors in the RF and microwave test and measurement community. Whether your interests include high-throughput production or one-of-a-kind metrology measurements, complex systems or simple circuit modeling, small to large signal measurements, phase noise or noise figure, DC to lightwave, you will find similarly interested technologists and maybe an expert. Starting with the continental breakfast in the exhibition area, continuing through the two exhibition/interactive forum sessions and the luncheon, there will be ample opportunity for discussion with others facing similar challenges. Attendees find that these interactions are often the best source of ideas and information for their current projects. So come and join us.

MICROWAVE WEEK AT A GLANCE

SUNDAY

0900 - 1200 AM Workshops & Short Courses

- WSA: Introduction to GaN MMIC Design (cont. in PM)
- WSB: Advancements and Challenges Toward Radio-in-Package and Radio-on-Chip (cont. in PM)
- WSC: Imaging at Millimeter-Wave and Beyond (cont. in PM)
- WSD: Re-Configurability Requirements for Multi-standard Low-power Operation (cont. in PM)
- WSE: Advancements in Linear Power Amplifiers for Cellular Infrastructure (cont. in PM)
- WSF: EMI Compliant Design Practices: Interference Anal., Floorplanning, Grounding Strategies, Chip-Package-Board Co-Design (cont. in PM)
- WSG: New Architectures for Digitized Receivers (cont. in PM)
- WSH: Design for Manufacturability and Self-Testability of RFICs (cont. in PM)
- WSI: RF Bio-Medical Electronics and Sensors (cont. in PM)
- WSJ: Systems & Circuits for Sensing, Co-Existence, and Interference Mitigation in SDR and Cognitive Radios (cont. in PM)
- SC-1: Techniques and Realizations of Microwave and RF Filters (cont. in PM)
- SC-2: Nonlinear Dynamics and Stability Analysis/Design of Microwave Circuits (cont. in PM)

Registration 0700 - 1800 (BCC: Pratt Street Lobby) • **RFIC Plenary** 1740 - 1900 (BCC: Ballroom III-IV) • **RFIC Reception** 1900 - 2100 (BCC: Ballroom I-II)

MONDAY

0900 - 1200 AM Workshops & Short Courses

- WMA: High Efficiency, Linear Power Amplifier Technology: Ka-, Q-band and Beyond (cont. in PM)
- WMB: Nanotechnologies for Microwave Interconnects and Packaging (AM only)
- WMC: Practical Compression, IMD, Load Pull and Behavioral Modeling Measurements (cont. in PM)
- WMD: Laboratory Class: Wafer-Level S-Parameter Calibration Techniques (cont. in PM) (BCC: Room 318 - 320)
- WME: Simulation- and Surrogate-Driven Microwave Design Technology (cont. in PM) (BCC: Room 321 - 323)
- WMF: Challenges and Techniques of Magnetic Resonance Imaging (MRI) Systems (cont. in PM)
- WMG: Recent Developments in Microwave Imaging and Detection (cont. in PM)
- WMH: Flexible, Autonomous RFID-Enabled Sensors: Novel Applications, Energy Harvesting and Integration Challenges (cont. in PM)
- WMI: Current state of Hexaferrite Materials and Their Applications (cont. in PM)
- WMK: High Power Effects on Passive Microwave Components (cont. in PM)
- SC-3: Noise in Electromagnetic Circuits and Systems (AM only)
- SC-4A: Low Phase Noise Oscillators: Theory and Design and Laboratory (cont. in PM)
- SC-5: Frequency Synthesizer Design Techniques (cont. in PM)

1200 - 1320 Panel Session

Panel Session: Software-Defined Radios - Facts and Fantasies (BCC: Room 307 - 308)

Registration 0700 - 1800 (BCC: Pratt Street Lobby) • **RFIC Symposium** 0800 - 1720 • **IMS Plenary** 1740 - 1900 (BCC: Ballroom III-IV) • **IMS Welcome Reception** 1900 - 2100 (BCC: Ballroom I-II)

TUESDAY

0800 - 0940 Early AM Technical Sessions	1000 - 1140 Late AM Technical Sessions	1200 - 1320 Panel Session
TU1A: Integrated and Tunable Filter Technologies (BCC: Room 310)	TU2A: Compact Reconfigurable and Tunable Filters (BCC: Room 310)	Panel Session: What Is the Limit of Multi-Radio Integration ... Or Rather, Is It 'Disintegration'? (BCC: Room 307 - 308)
TU1B: RF and Microwaves in Medicine: Monitoring and Imaging (BCC: Room 314 - 315)	TU2B: RF and Microwaves in Medicine: Medical Sensors and Devices (BCC: Room 314 - 315)	
TU1C: RFID Technologies and Applications (BCC: Room 316 - 317)		
	TU2F: New Concepts in Microwave Radiation Structures (BCC: Room 324 - 326)	
TU1G: Novel Semiconductor Devices and Ics (BCC: Room 327 - 329)	TU2G: Silicon CMOS RF and Microwave Circuits (BCC: Room 327 - 329)	

Registration 0700 - 1800(BCC: Pratt Street Lobby)• **RFIC Symposium** 0800 - 1140 • **Exhibition** 0900 - 1700 (BCC: Halls B-G) • **MicroApps Seminar** 0930 - 1650 (Exhibit Hall: Booth 413) • **IMS Student Design Competitions** 1200 - 1400 (BCC: Hall A) • **IMS Student Paper Contest** 1200 - 1400 (BCC: Hall A) • **RFIC Interactive Forum** 1200 - 1400 (BCC: Hall A) **Rump Session:** Microwave R&D Funding Policy & Trends 2000 - 2200 (Hilton: Key 5)

WEDNESDAY

0800 - 0940 Early AM Technical Sessions	1000 - 1140 Late AM Technical Sessions	1200 - 1320 Panel Session
WE1A: Advanced Synthesis and Design Techniques of Microwave Filters and Multiplexers (BCC: Room 310)	WE2A: Novel Technologies for Practical Filter Realizations (BCC: Room 310)	Panel Session: Commercial Viability of RF-MEMS: A Reality or a Dream? (BCC: Room 307 - 308)
WE1B: Novel Transmission-line Metamaterial Structures and Devices (BCC: Room 314 - 315)	WE2B: Planar and Substrate Integrated Waveguide Techniques (BCC: Room 314 - 315)	
	WE2C: Focus Session: Recent Developments in Photonics for RF Front-Ends (BCC: Room 316 - 317)	
WE1D: Advances in Ultra-Low-Power Transceiver Architectures (BCC: Room 318 - 320)	WE2D: Power Amplification Enhancement Techn. for Advanced Wireless Comm. Systems (BCC: Room 318 - 320)	
WE1E: Array and Power Combining Techniques (BCC: Room 321 - 323)	WE2E: Array and Module Integration (BCC: Room 321 - 323)	
WE1F: Special Session: 100 Years of Superconductivity - Existing & Emerging RF Applications of Superconductivity (BCC: Room 324 - 326)	WE2F: Focus Session: Retrospective and Outlook of Computational Microwave Engineering (BCC: Room 324 - 326)	
WE1G: Millimeter Wave Technologies and Components for System Integration (BCC: Room 327 - 329)	WE2G: THz Technologies and Applications (BCC: Room 327 - 329)	
WE1H: Special Session: Memorial Session for Theodore Saad (BCC: Room 309)	WE2H: Special Session: Memorial Session for Roger Sudbury (BCC: Room 309)	

Registration 0700 - 1800 (BCC: Pratt Street Lobby) • **Exhibition** 0900 - 1800 (BCC: Halls B-G) • **MicroApps Seminar** 0930 - 1650 (Exhibit Hall: Booth 413) • **IMS Interactive Forum** 1200 - 1400 (BCC: Hall A)

THURSDAY

0800 - 0940 Early AM Technical Sessions	1000 - 1140 Late AM Technical Sessions	1200 - 1320 Panel Session
TH1A: Advances in Signal Generation Technologies (BCC: Room 310)	TH2A: Innovative Planar Filters and Multiplexers (BCC: Room 310)	Panel Session: Microwave Photonics: A Growing or Shrinking Value Proposition? (BCC: Room 307 - 308)
TH1B: New Advances in Power Dividers and Hybrids for RF and Microwave Applications (BCC: Room 314 - 315)	TH2B: Advances in Passive Circuit Technology for Microwave System Applications (BCC: Room 314 - 315)	
TH1C: Focus Session: Microwaves Around the World - I (BCC: Room 316 - 317)	TH2C: Industrial Sensors Using Innovative RF Techniques (BCC: Room 316 - 317)	
TH1D: Signal Processing/Integrity Circuitry for Data Throughput up to 80 Gbit/s (BCC: Room 318 - 320)	TH2D: Focus Session: The Impact of Carbon Nanoelectronics on Radiofrequency Technology (BCC: Room 318 - 320)	
TH1E: Focus Session: Microwave Technologies for Space: Needs and Challenge (BCC: Room 321 - 323)	TH2E: Advances in Radar Systems for Sensing and Imaging (BCC: Room 321 - 323)	
TH1F: Advanced Packaging Materials and Techniques for Microwave and Millimeter-wave Applications (BCC: Room 324 - 326)	TH2F: Time-Domain Modeling: Advances and Applications (BCC: Room 324 - 326)	
TH1G: Power Amplifiers and Reconfigurable Networks for VHF and UHF (BCC: Room 327 - 329)	TH2G: High Linearity, High Efficiency Power Amplifier Techniques (BCC: Room 327 - 329)	

Registration 0700 - 1600 (BCC: Pratt Street Lobby) • **Exhibition** 0900 - 1500 (BCC: Halls B-G) • **MicroApps Seminar** 0910 - 1450 (Exhibit Hall: Booth 413) • **IMS Interactive Forum** 1200 - 1400 (BCC: Hall A)

FRIDAY

AM Workshops & Short Courses 0800 - 1200

- WFA: Wireless Power Transmission (cont. in PM)
- WFB: Piezoelectric RF MEMS for Communication and Defense Applications (AM only)
- WFC: The Design Flow of Microwave Power Amplifiers: Challenges and Future Trends (cont. in PM)
- WFD: Medical and Biological Microwave Sensors and Systems (cont. in PM)
- WFE: Electron. Steered Arrays for Radar, Comms and EW: Are They Affordable And Ready to Assume a Place in 21st Century Systems? (cont. in PM)
- WFF: Wireless Sensor Network Technologies for Emerging Applications (cont. in PM)
- WFG: Innovative and Highly Accurate Local Positioning Systems (cont. in PM)
- WFH: Recent Advances in Multi-Giga Bit Per Second (Gbps) Data Throughput Techniques for Ka-Band Space-to-Ground Links (AM only)
- WFI: Advances in RF Imaging Techniques (AM only)
- WFJ: Nanotechnology-Enabled RF and Cognitive Devices, Components and Systems (cont. in PM)
- WFK: Practical Design Approaches and Issues in Software Defined Radios (cont. in PM)

Registration 0700 - 0900 (BCC: Pratt Street Lobby) • **ARFTG Conference** 0800 - 1550 (Hilton: Holiday 1-3) • **ARFTG Interactive Forum** 0940 - 1040 and 1410 - 1450 (Hilton: Holiday 4-5)

5 June 2011

1320 - 1720 PM Workshops & Short Courses	Social Events
WSA: Introduction to GaN MMIC Design (cont. from AM)	
WSB: Advancements and Challenges Toward Radio-in-Package and Radio-on-Chip (cont. from AM)	RFIC Reception 1900 - 2100 (BCC: Ballroom I-II)
WSC: Imaging at Millimeter-Wave and Beyond (cont. from AM)	
WSD: Re-Configurability Requirements for Multi-standard Low-power Operation (cont. from AM)	
WSE: Advancements in Linear Power Amplifiers for Cellular Infrastructure (cont. from AM)	
WSF: EMI Compliant Design Practices: Interference Anal., Floorplanning, Grounding Strategies, Chip-Package-Board Co-Design (cont. from AM)	
WSG: New Architectures for Digitized Receivers (cont. from AM)	
WSH: Design for Manufacturability and Self-Testability of RFICs (cont. from AM)	
WSI: RF Bio-Medical Electronics and Sensors (cont. from AM)	
WSJ: Systems & Circuits for Sensing, Co-Existence, and Interference Mitigation in SDR and Cognitive Radios (cont. from AM)	
WSK: Half-Day Workshop: Efficiency Enhancement Techniques of Power Amplifiers and Transmitters for Mobile Applications (PM only)	
SC-1: Techniques and Realizations of Microwave and RF Filters (cont. from AM)	
SC-2: Nonlinear Dynamics and Stability Analysis/Design of Microwave Circuits (cont. from AM)	

6 June 2011

1320 - 1720 PM Workshops & Short Courses	Social Events
WMA: High Efficiency, Linear Power Amplifier Technology: Ka-, Q-band and Beyond (cont. from AM)	IMS Welcome Reception 1900 - 2100 (BCC: Ballroom I-II)
WMC: Practical Compression, IMD, Load Pull and Behavioral Modeling Measurements (cont. from AM)	
WMD: Laboratory Class: Wafer-Level S-Parameter Calibration Techniques (cont. from AM) (BCC: Room 318 - 320)	
WME: Simulation- and Surrogate-Driven Microwave Design Technology (cont. from AM) (BCC: Room 321 - 323)	
WMF: Challenges and Techniques of Magnetic Resonance Imaging (MRI) Systems (cont. from AM)	
WMG: Recent Developments in Microwave Imaging and Detection (cont. from AM)	
WMH: Flexible, Autonomous RFID-Enabled Sensors: Novel Applications, Energy Harvesting and Integration Challenges (cont. from AM)	
WMI: Current state of Hexaferrite Materials and Their Applications (cont. from AM)	
WMJ: Compact Equivalent Circuits and Table Based FET Models - Is There One Winner for Circuit Designers and Foundries? (PM only)	
WMK: High Power Effects on Passive Microwave Components (cont. from AM)	
SC-4A: Low Phase Noise Oscillators: Theory and Design and Laboratory (cont. from AM)	
SC-5: Frequency Synthesizer Design Techniques (cont. from AM)	
SC-6: National and International Spectrum Regulation for Microwave Professionals (PM only)	

7 June 2011

1420 - 1540 Early PM Technical Sessions	1600 - 1720 Late PM Technical Sessions	Social Events
TU3A: Microwave Ferrite Devices and Materials (BCC: Room 310)	TU4A: Tunable Passives and Acoustic Filters (BCC: Room 310)	Student and GOLD Receptions 1800 - 1930 (Hard Rock Café Baltimore)
TU3B: Measurement Techniques for Biological Tissues and Subjects (BCC: Room 314 - 315)	TU4B: 44: Focus Session: High Field Magnetic Resonance Imaging Systems (BCC: Room 314 - 315)	Women in Microwaves Reception 1800 - 2000 (Hilton: Lobby Bar)
TU3C Special Session: Historical Perspectives on Microwave Development in the Baltimore-Washington Area (BCC: Room 316 - 317)	TU4C: Advances in Low Noise IC Design and Measurements (BCC: Room 316 - 317)	Ham Radio Social 1800 - 2100 (Hilton: Key 12)
TU3D: Advances in RF MEMS Switches (BCC: Room 318 - 320)	TU4D: Advances in RF MEMS Tunable Filters (BCC: Room 318 - 320)	
TU3E: Nonlinear Circuit and System Simulation (BCC: Room 321 - 323)	TU4E: Efficient Wireless Transfer of RF Power (BCC: Room 321 - 323)	
TU3F: Analysis and Design of Novel Structures (BCC: Room 324 - 326)	TU4F: Waveguiding and Periodic Structures (BCC: Room 324 - 326)	
TU3G: Efficient Broadband Power Amplifiers (BCC: Room 327 - 329)	TU4G: GaN and LDMOS Linear Power Amplifiers (BCC: Room 327 - 329)	

8 June 2011

1420 - 1540 Early PM Technical Sessions	1600 - 1720 Late PM Technical Sessions	Social Events
WE3A: Broadband Measurement Techniques (BCC: Room 310)	WE4A: Advanced Circuit and Material Measurement (BCC: Room 310)	Industry Hosted Cocktail Reception: 1715 – 1800 (BCC: Halls B-G)
WE3B: New Trends in Passive Components (BCC: Room 314 - 315)	WE4B: Focus Session: Handset Impedance Tuners (BCC: Room 314 - 315)	MTT-S Awards Banquet 1820 - 2200 (Hilton: Key 7-12)
WE3C: Microwave Photonics Systems and Devices (BCC: Room 316 - 317)	WE4C: High Power Microwave Processing: Modeling and Applications (BCC: Room 316 - 317)	
WE3D: High-Power, High-Efficiency GaN Power Amplifiers (BCC: Room 318 - 320)	WE4D: Innovative GaN Power Amplifiers (BCC: Room 318 - 320)	
WE3E: Non-linear Modeling for Microwave Devices (BCC: Room 321 - 323)	WE4E: FET Modeling (BCC: Room 321 - 323)	
WE3F: Recent Advances and Applications of Space Mapping (BCC: Room 324 - 326)	WE4F: Computer-Aided Analysis for Electrically Large Distributed Networks (BCC: Room 324 - 326)	
WE3G: Advances in Millimeter Wave and THz Technologies (BCC: Room 327 - 329)		
	WE4H: Special Session: A Tribute to Professor Nathan Marcuvitz (BCC: Room 309)	

9 June 2011

1420 - 1540 Early PM Technical Sessions	1620 – 1720 Closing Ceremony	Social Events
TH3A: Multi-band and Multi-mode Planar Filters (BCC: Room 310)	CLOSING CEREMONY With a special Presentation "Cognitive Radar" by Dr. Joseph Guerci (BCC: Ballroom III - IV)	MTT-S Student Awards Luncheon: 1200 – 1400 (Hilton: Ballroom 6)
TH3B: Frequency Conversion and Control (BCC: Room 314 - 315)		Crab Feast 1800 - 2200 (USS Constellation & Pier 1)
TH3C: Focus Session: Microwaves Around the World - II (BCC: Room 316 - 317)		
TH3D: Advances in RF Nanotechnology (BCC: Room 318 - 320)		
TH3E: Advances in Communication, Positioning, and Direction Finding Systems (BCC: Room 321 - 323)		
TH3F: Accuracy Enhancement in Numerical Frequency Domain Techniques (BCC: Room 324 - 326)		
TH3G: Broadband/Multiband Power Amplifier Design Techniques (BCC: Room 327 - 329)		

10 June 2011

PM Workshops & Short Courses 1320 - 1720
WFA: Wireless Power Transmission (cont. from AM)
WFC: The Design Flow of Microwave Power Amplifiers: Challenges and Future Trends (cont. from AM)
WFD: Medical and Biological Microwave Sensors and Systems (cont. in PM)
WFE: Electron. Steered Arrays for Radar, Comms and EW: Are They Affordable And Ready to Assume a Place in 21st Century Systems? (cont. from AM)
WFF: Wireless Sensor Network Technologies for Emerging Applications (cont. from AM)
WFG: Innovative and Highly Accurate Local Positioning Systems (cont. from AM)
WFJ: Nanotechnology-Enabled RF and Cognitive Devices, Components and Systems (cont. from AM)
WFK: Practical Design Approaches and Issues in Software Defined Radios (cont. from AM)

Technical Track Key:
- General Interest
- Emerging Technical Areas
- Systems & Applications
- Active Components
- Passive Components
- μwave Field & Circuit Techn.

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By Jim Kobylecky, Managing Editor

Product News

AGILENT CONNECTS SYSTEM ARCHITECTS

Agilent Technologies Inc. released a new version of its system-level communications design environment. SystemVue now enables wireless system architects and system-on-chip designers to validate multiband, high-transistor-count wireless IC designs accurately against the latest communications standards. It now connects with Agilent's GoldenGate environment to help meet the challenging requirement of ETSI LTE/LTE-A and other emerging wireless standards, via an exclusive, fast circuit envelope (FCE) model or direct envelope-level cosimulation. The new FCE models execute 1,000 to 100,000 times faster than the original RFIC physical designs, with virtually no loss in accuracy at the system level. The new FCE models run natively in SystemVue, as part of the W1719 RF System Design Kit.

AWR INITIATIVE TOOLS UP GRADUATING ENGINEERING STUDENTS

AWR Corporation is continuing its AWR Graduate Gift Initiative for calendar year 2011. This initiative provides qualified electrical engineering graduates with a free, fully-functional, 1-year term license of AWR's Microwave Office and Visual System Simulator software suites - including AXIEM 3D planar EM simulator. The software gift, while restricted to the graduate's personal-use (node locked versus floating license), is not restricted to educational use but rather open for commercial use at the graduate's current/future employer. The Initiative is available to all qualified class of 2011 graduating students with BS, MS, or PhD Electrical Engineering degrees from universities, colleges and accredited learning institutions within AWR's University Program. Qualification terms are found on the AWR website at www.awrcorp.com/graduates/terms /

FREESCALE RF POWER LDMOS TRANSISTORS COVER FULL FREQUENCY BANDS

Freescale Semiconductor introduced two LDMOS RF power transistors that allow wireless base station amplifiers to cover all channels in an entire allocated frequency band. They deliver a compelling combination of high linearity, high efficiency, wide instantaneous bandwidth and high power that extend the instantaneous signal bandwidth to an industry-leading 160 MHz, making them ideal for these next-generation amplifier systems. The MRF8P20165WH/S for the 1930 to 1995 MHz PCS band and the MRF8P20140WH/S for the 1880 to 2025 MHz TD-SCDMA bands F & A, can support the corresponding wireless spectrum with one amplifier. This significantly reduces the number of power amplifiers needed for a multi-band base station and enables network operators to consolidate devices and equipment, resulting in lower operating expenditures.

TRIQUINT UNVEILS BROADBAND WCDMA SOLUTION

TriQuint Semiconductor, Inc. introduced a new member to its TRIUMF Module Family, the TQM7M9070. Its advanced integration technology offers 3G designers building global smartphones and other mobile devices a streamlined RF footprint, through support for multiple modulations and multiple bands in one module. It provides WCDMA/HSUPA modulation over multiple bands by enabling outstanding Power Added Efficiency (PAE) without requiring a DC to DC converter. Power amplifier PAE is a critical contributor to longer battery life and greatly enhances the user experience of mobile devices. Complementary to TQM7M9070, TriQuint offers a highly-efficient quad-band power amplifier module, the TQM7M5022R, for GSM/EDGE to support a complete amplification solution for any cellular multimode/multiband application.

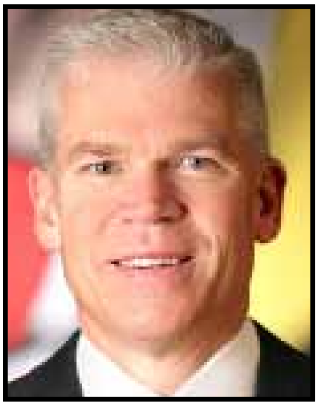
AGILENT EASES FIELD TESTING WITH 20-GHZ HANDHELDS

Agilent Technologies Inc. announced two field-ready instruments to install, maintain and troubleshoot RF/microwave systems, monitor the spectrum or manage interference in the field. The new analyzers make field testing easier by providing the performance of a benchtop instrument in a handheld device, along with a range of functionality for ensuring field-ready operation and automating routine tasks. The N9344C and N9343C HSAs provide fast and accurate measurement from 1 MHz to 20 GHz and 13.6 GHz, respectively. Both instruments are tunable to 9 kHz. Their rugged and fanless design handles tough field environments with automatic LCD brightness and keypad backlight control for clear screen viewing day or night. A built-in GPS receiver and GPS antenna provide precise location information. A unique Task Planner capability reduces test setup time by 95 percent.

By David Lammers, Editor-in-Chief, SemiMD

Business Focus: TI Buy Brings "Benefits of Scale" to National

Texas Instruments will seek to boost revenue growth rates after its acquisition of National Semiconductor is finalized, said TI CEO Richard Templeton. "We are not consolidating. We looked at (National's) revenue growth over the last two years, and realized that we could get those rates growing faster.



Rich Templeton

Texas Instruments' surprise move to acquire National Semiconductor brings "the benefits of scale" to the analog IC market, including the 300-mm wafer analog IC fabrication capabilities TI is bringing online, executives said

TI said it will spend $6.5 billion in the form of cash and debt to acquire National, a roughly 75 percent premium over National's valuation before the deal was announced late Monday (April 4).

The deal creates a 2,500 person sales force, 10 times as many salespersons out in the field as National could muster, said TI CEO Richard Templeton, who started his career at TI in sales after graduating from Union College with a degree in electrical engineering.

Don Mcleod, CEO of National, said "TI brings muscle, the benefits of scale" to National, a company which has seen a slow recovery in revenues since the end of the 2008-2009 downturn. National operates fabs in Greenock, Scotland, and South Portland, Maine, which TI will continue to operate.

It may take as long as the rest of this year before regulatory approval is gained in all of the many countries where the two companies do business, the executives said. Once joined, the combined operation will add TI's 14-plus percent analog market share and the 3-plus percent share held by National, Templeton said. The two companies together have $4 billion in cash, requiring "three to four billion" in borrowing after leaving some cash aside for operations.

Templeton said National's analog business will become a fourth unit within TI's overall analog operation, which now includes power management, high-volume analog (HVA), and high-performance analog (HPA).

Asked if TI would ditch some manufacturing facilities after the merger, Templeton said, "We are keeping everything." National's fab are running "in the 60 percent (capacity utilization) range," he said. The main goal of the merger is to generate more revenue across roughly the same fixed costs. "We are not consolidating. We looked at (National's) revenue growth over the last two years, and realized that we could get those growth rates growing faster."

Analog product portfolios "take a long time to build, and they don't change that fast," the TI CEO said. The merged analog operation will continue to run all of the processes developed by both companies. Since TI has processes and 300-mm manufacturing capabilities that National doesn't have, those will become available to National's design teams if they choose to use them, he said. "We won't have any requals – that takes time," he said.

National's average 60 percent fab utilization levels, and TI's plans to bring on 300-mm capacity at its partially filled Richardson fab near Dallas, provide an opportunity to ramp production. "With the current utilization levels, our intent is to fill those factories. If it makes sense to move (National) products to those 300-mm fabs, we will do it. Those are long-term assets, but we won't do any fab stuffing," Templeton said.

TI CFO Kevin March said TI is in the process of recertifying the clean room at its Miho, Japan fab, which accounted for roughly 10 percent of TI's production value last year. The facility, which manufactures analog and digital light processing (DLP) products, will have a "mini line" operating by mid-April, March said.

Templeton noted that National was "the original analog company" and that both staffs bring a "passion of innovation, a love for the analog business" to the merged company.

Templeton emphasized the value of TI's sales force, saying that the combined sales team "will turn its energy loose to hunt for every circuit on every board." He cited industrial analog an area where National has a relatively stronger presence with its lineup of high-voltage analog parts.

Originally published in SemiMD.

David Lammers has covered the semiconductor industry since 1980, including 19 years when he was based in Tokyo. He worked at the Associated Press Tokyo bureau, then spent 21 years at E.E. Times as Asia correspondent based in Tokyo (1985-1998) and bureau chief in Austin

BLOG

Keeping Up With Complexity

By Ed Sperling, Editor-in-Chief, System-Level Design (SLD) Community

There are two schools of thought in designing complex SoCs. One says that increasing complexity requires a higher level of abstraction. The other says providing enough detail to get the design right is the only effective way to do it.

There are staunch proponents of both approaches, but what has been missing are bridges to tie the higher level of abstraction to the more laborious—and much slower—gate-level details. Tools that allow more exploration on both sides are beginning to emerge, along with a recognition that they are definitely necessary to complete designs.

These bridging exploratory or path-finding approaches rely heavily on what-if questions. What if a certain piece of IP was used next to another piece of IP, for example? Would a different IP block work better? How about if the frequency of a core was changed or a different I/O was used? And what happens if the voltage in one area is lowered or raised?

These kinds of tradeoffs are common, but increasingly each step of the way can update other pieces along the design flow. At 45nm and beyond, there are many of these kinds of tradeoffs, and the number increases dramatically at 28nm and in 2.5D and 3D structures.

"There are some path finding methodologies available today," said Riko Radojcic, director of engineering at Qualcomm. "The part that is missing is incorporation or spatial awareness into these methods and tools, which is why it is especially important for 3D exploration. I started feeling the lack of this capability when we first looked at the tradeoffs between regular 'complex' design rules and 'gridded' design rules, and when we were looking at the tradeoffs associated with aggregating memories into a smaller set of larger instances and equipping them with redundancy versus having many small instances all over the place. In both cases we needed spatial awareness that was not easy to import up to the SoC level."

To read the full story, please visit: http://chipdesignmag.com/sld/blog/2011/03/31/keeping-up-with-complexity/

By Janine Love, Contributing Editor

The Race is on for RF MEMS

The technology is poised for high volume production but only if the models and architectures are in place.

RF MEMS finally seem poised to break into mass production across a range of applications, including mobile communications, test instrumentation, and, eventually, defense systems. But, if this technology doesn't step up soon, it could miss opportunities for significant market share.

In review, one might characterize the RF MEMS market as overhyped and suffering from reliability issues. Well, patience is beginning to pay off. Both Laurent Robin, analyst in MEMS devices, Yole Developpement, and Jérémie Bouchaud, Director – Principal analyst MEMS & Sensors IHS iSuppli, agree that reliability is no longer an issue.

"RF MEMS finally seem poised to break into mass production across a range of applications, including mobile communications, test instrumentation, and, eventually, defense systems."

Today's key players include Advantest, Omron, Radant, XCOM, Analog Devices, Wispry, and TDK-EPC. According to Bouchaud, much current effort focuses on reducing costs for RF MEMS in instrumentation and developing system architectures for antenna tuning in mobile handsets.

Both Robin and Bouchaud agree that RF MEMS technology has the best performance for antenna tuning. However, while Robin sees RF MEMS scoring market share here, Bouchaud is more cautious, "If one of the candidates with MEMS manages to commercialize their switch/varicap into cell phones in the next 18 months, a great new market opens for MEMS ($100s of million in 4-5 years). If none of these companies are successful in that time, then SOS, SOI, or ferroelectric technologies will share that opportunity."

To capture market share, RF MEMS engineers are challenged to achieve their cost/performance objectives. How are they getting it done? According to Bjorn Sjodin, VP of Product Management, COMSOL Inc., one of the biggest challenges is that the circuit model may not accurately represent reality. He says it is important to include several effects (including geometric and material nonlinear ones) in a simulation to achieve an accurate frequency response. (COMSOL Multiphysics and its MEMS module perform multiphysics analysis, including electromagnetic, structural, fluid, and acoustics simulations.) Sjodin finds that engineers can overcome discrepancies between measured and simulated results by including more physics phenomena in the simulation and allowing for nonlinear effects.

Robb Shimon, RF MEMS Technology Development Manager in the High Frequency Technology Center, Agilent Technologies agrees that the micro-scale material properties of common RF MEMS materials are not well understood, adding that models that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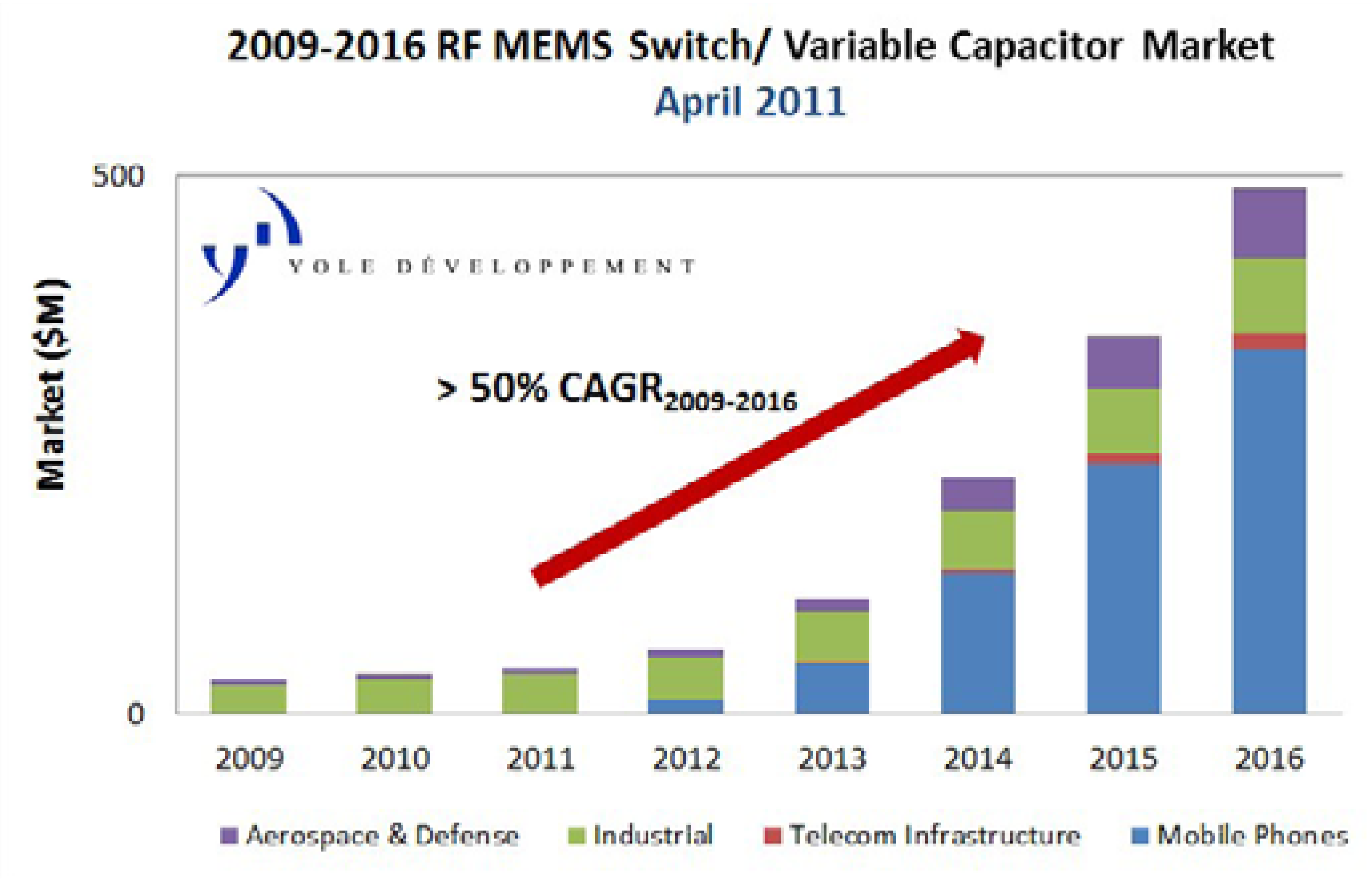

predict the behavior of RF MEMS devices with these properties are not well developed.

At Agilent, the team extracts an electrical model for each MEMS device state, and then uses this model set in a conventional electronic IC design software, such as its own ADS. "In all practical cases I can think of, the design of the RF MEMS device is a separate activity from the design of ICs containing the RF MEMS devices. During the device design phase, we use generic 3D multi-physics tools; during the IC design phase, we use electrical-only models, preferably extracted from fabricated devices, in standard IC CAD software," says Shimon.

At the moment, then, the remaining challenges for RF MEMS seem to be developing accurate models and creative architectures. Overall, though, despite years of development, it still looks to be a race against the clock.

Janine Sullivan Love is a contributing editor and technical writer. Janine is a member of NASW and ACS and began working as a writer in the RF and microwave field more than 15 years ago.

By Pallab Chatterjee, Regional Editor

New Directions in RFIC and MMIC

One of the historic drivers for advanced devices and circuits has been communications. These circuits have been based on Radio Frequency ICs (RFICs) and Monolithic Microwave ICs (MMICs) that have come to replace discrete device circuits. The predominant place these circuits have appeared the past 50+ years has been in broadcast, satellite and telecommunications applications.

As technology has progressed, the frequencies addressed by these circuits have also increased. Originally RFICs were operating in the MHz range, and the GHz+ range was for MMICs. Today's circuits have RFICs operating in the xxGHz range and the 100GHz+ through Terahertz applications are the domain of the MMICs. As these frequencies have increased, the lines between RFICs and MMICs have blurred a bit. There are two main differentiating factors between the two technologies. The first is process technology – RFICs tend to be built with mainstream mixed signal CMOS, Bipolar, or BiCMOS flows, where MMICs tend to be built with alternate materials such as III-V compounds, SOS, or graphene. The second is the design methodology – RFICs tend to be designed and their resulting products specified in the time domain using traditional analog / mixed signal tools, and MMICs tend to be designed and specified using S parameters in the frequency domain. A diagram of the functions areas and frequencies used by these designs is shown in figure 1.

"As these frequencies have increased, the lines between RFICs and MMICs have blurred ...."

Both of these products have been dominated by analog designs and analog function blocks. These blocks include amplifiers, filters, mixers, modulators, and antenna drivers. RFICs and MMICs have been the main stay of microwave & satellite based communication on both the transmit and receive ends. The sensor community also utilizes them for radar, x-ray (imaging) and at lower frequencies, ultra-sound applications. These products are also well known for radio and television broadcast, including high definition digital broadcast and tower technologies. The broadcast environment is one of the largest consumers of these products as RFICs are the mainstay of the audio & video source & mixing switching industry.

As digital signal speeds have moved up, and inter-chip and off-chip communications have become the norm, there is an increasing use of digital control blocks to implement these circuits. The increased use of high speed digital is also adding new functions to the RFIC and MMIC world. The biggest addition is the inclusion of SERDES and high speed bus transceivers to the world of RFIC. These blocks now routinely operate in the 5GHz-30GHz signal range with data recovery and AGC functions for interface with both electrical and optical signals. Also encroaching in the digital side, is the increasing use of eQAM blocks, for sending data over coax or fiber to the home, for the distribution of multi-channel broadband. Due to support of legacy set-ups and installations of cables, the need for digitally configurable and addressable RF transceivers is forefront rather than using standard products alone. This marketplace is

Participate in these Growing Online Communities for System Level Design, Low Power Engineering and Semiconductor Manufacturing and Design (SemiMD)

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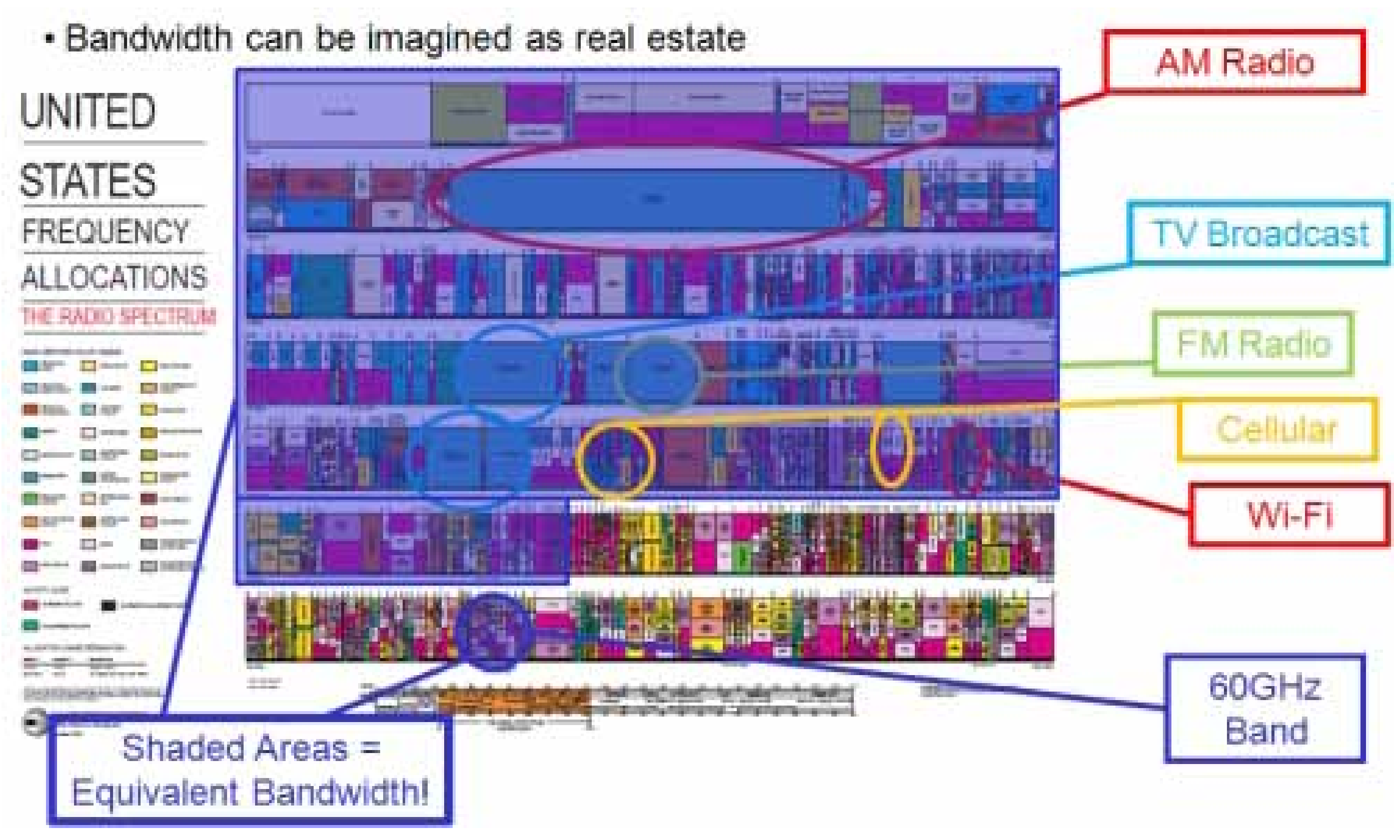

Figure 1: This diagram shows RF function areas and frequencies.

currently dominated by FPGA technology.

The mobile revolution is also driving this area. Wireless devices and communications standard have moved up to the 5GHz area and new technologies are targeting a 60GHz communication band. These devices are still being made with standard RFICs that utilize the high frequency operation from nano-geometry devices. Many of these functions have migrated from being standalone chips to being IP blocks that are implemented in mixed signal SOCs.

"The biggest addition is the inclusion of SERDES and high speed bus transceivers to the world of RFIC."

MMICs are dominating in the optical communication, high power RF and new imaging technologies. The ability to hit TeraHz speeds has created new applications for body and security imaging, as well as for ultrahigh speed secure data communication. At these new data rates, enabled by graphene & carbon nanotube transistors and AFD engineered III-V materials, new circuits addressing cloaking and other spatial effects are being investigated for the commercial marketplace.

Pallab Chatterjee is Coordinating Regional Editor of Chip Design. He has been and independent consultant in the EDA and Mixed Signal design space for over 20 years. Pallab holds a BSEE from UC Berkeley and an MSEE from San Jose State University.

By John Blyler, Editor-in-Chief

Noble Award Honors Silicon on Sapphire Founders

Turning silicon on sapphire (SoS) technology into commercially viable chips wins Peregrine Semiconductor founders the IEEE Noble Award at this year's MTTS event.

Dr. Mark L. Burgener, co-founder of Peregrine Semiconductor

This year's IEEE Daniel E. Noble Award will go to Dr. Mark L. Burgener and Dr. Ronald E. Reedy, co-founders of Peregrine Semiconductor. They will be honored for "basic research and development of silicon on sapphire technology culminating in high-yield, commercially viable integrated circuits." The Noble award is presented annually to those individuals who made a significant contribution to emerging technologies.

RF & Microwave Systems talked with Peregrine's founder, Ron Reedy, and Chief Marketing Officer, Rodd Novak, about the struggles to bring SoS technology to the commercial world. Here is a portion of that interview. – JB

RFMW: First of all, congratulations on the award. Making silicon on sapphire (SoS) a commercially viable process must have been full of challenges, from tool flows and manufacturability.

Reedy: We spent the first 10 years developing the process at multiple, different fabrication facilities (fabs). Surprisingly, there is a huge amount of effort that follows after the fab work, for example, learning to singulate sapphire. Since sapphire is a very hard material, it was difficult to singulate or dice up the wafers into chips. Other equally important questions arose, such as SoS packaging. Testing was also an issue, since sapphire's transparency does not work well with standard automatic optical inspection equipment.

We faced fewer challenges in the design tool flow area, since we used all of the standard industry tools. Further, all the processes were industry standard, but we did have to tweak the receipts to hone them for high yielding production. Simple production is not enough. If you can not yield it, you are not there. That is the very time consuming and expensive part.

"Our SoS wafers run down a CMOS line without any impairment to their fab."

We can make 10 million chips per week. I'm guessing that no more than 10 or 20 million silicon on sapphire chips had ever been shipped prior to our company entering the picture. We are doing in a week, what the whole industry struggled to do in a lifetime. Equally important, we are achieving yields that the market can afford to pay for the required device performance. Price is important, because you can price yourself out of the high performance analog market.

RFMW: Is your process easily transferrable between different foundries?

Novak: Yes. We use all standard processing equipment. Our SoS wafers run down a CMOS line without any impairment to their fab. Further, we have ported it to three fabs; Rohm (formerly Oki Semiconductor), MagnaChip Semiconductor, and UMC. In the last 10 months, we announced work with IBM. So the technology is very transferrable.

Perhaps a more important point is that we can transfer products between fabs, which is something very unique for RF front-end devices. In alternative technologies like Gallium Arsenide (GaAs), the fabs are so highly tuned in that it is nearly impossible to transfer a product from multiple fabs with the same performance level. Conversely, we are able to supply the market from multiple fabs, providing CMOS scaling as well as redundancy to the front end. Prior to that I think you'd find customers very wary of single sourcing an RF front end but not so wary of single sourcing a transceiver or a baseband. We are bringing that CMOS mentality up to the front-end.

"The beauty is that sapphire is a perfect substrate for RF performance."

RFMW: The recent tsunami in Japan has taught the technology world that single sourcing can still be risky.

Reedy: We are still dissecting the impact on the supply chain of the disruptions in Japan. Few vendors can see all the way down their supply chain. Everybody is holding their breath, worried that the natural disaster might have damaged a little known company that supplies a crucial chemical additive for 80 percent of the world supply of something. Diversity in the supply chain is important. People are rethinking the whole Just-in-Time manufacturing mentality because it is so highly tuned but not very robust. Most of the world's products are going through a specific fab with a specific process. That can be risky.

RFMW: How does silicon on sapphire work?

Reedy: In a typical CMOS process, the transistors are either deposited on or ion implanted into photographically defined areas. When you build up all the layers it turns into the magic of an integrated circuit. But underneath all of that, 99.9 percent of the thickness of that chip is a solid slice of silicon which is a semiconductor. Partial conducting things tend to behave in strange ways. You can turn them into transistors, but you can also turn them into current leakage paths.

In essence, our SoS process slides out all of the silicon substrate and slides in a nature's best inert dielectric insulating material called sapphire. That's not how you do it, but that is the end result. The beauty is that sapphire is a perfect substrate for RF performance. Layered up from there is a pure CMOS structure. No extra metal layer masks are involved, although we did have to tweak the typical CMOS process recipe to change how much energy we use in an ion implanter. If you implant too deep, the IC structure lands in sapphire and does nothing. Aside from a few tweaks, our process uses the same design tools, tape out and masks as a regular silicon substrate.

RFMW: CMOS also has the advantage of being a low power platform.

Reedy: CMOS was one of the most idiotic things that anyone had ever dreamed up. It is expensive, complicated, latches up, and requires twice as many steps to make as other material. But it has the magnificent feature of being extremely low power. CMOS was not really used until the IBM 386 started catching fire in the PCs. Then someone suddenly discovered power dissipation was a problem and CMOS became popular. CMOS on Sapphire turns out yet lower power while maintaining incredibly high performance. The problem with silicon on sapphire was that no one could produce it.

RFMW: Let's talk about production numbers for SoS devices.

Novak: We have shipped over 700 million devices to date, driven mainly by the handset market. Other important segments include space satellites, military-aerospace, test equipment, displays, and broadband markets. We have well over 1,000 customers right now in very unique markets.

The satellite market was about the only real success for silicon on sapphire technology, prior to our company entering the market. SoS was radiation tolerant and extremely low power. Space systems like satellites are very sensitive to power consumption. Further, if you can save on power, you also save on cooling. We continue to support that primary market in the K-U bands and below.

RFMW: You've been able to achieve high production numbers. Is volume really that critical in the niche market of RF and microwave systems?

Reedy: I'm a big admirer of what the GaAs guys have done, but in the end nothing on this planet is as manufacturable as silicon CMOS. As I've often said, soybean farmers can not make soybeans to the level of reliability that we can make SoS devices. We ship a million chips with the goal of zero returns. For the last three to six trailing months, I think we have had two electrical returns out of 100 some million handset devices. There is no way that individual ears of corn are that good.

In our business, volume drives innovation, not the other way around. People think that if you innovate something it drives the volume. That is not the case. Only high volume markets can rationalize the expense of these developments, such as liquid crystal displays in TVs.

RFMW: Earlier, you mentioned the importance of yield. How does volume relate to yield?

Reedy: You can not afford to get the yield up if you are not in high volume because it is very expensive to find every last one percent of a yield problem. You don't get high yield by accident. You get there kicking and screaming the whole way. But if it is a high volume market, then it pays for itself in that yield. All the other markets then get that same yield. That applies not only cost but reliability. It's been proven from the very earliest days of the integrated circuit that high yielding wafers are high reliability wafers.

RFMW: Anything in conclusion?

Reedy: I have a personal request concerning the Noble Award that Mark and I will receive at MTTS. It is really important for us that the entire team be recognized for this award. Both Mark Burgener and I understand the rules of the award that it is only given to individuals, not companies. In reality, our success was the result of hundreds of people over two decades at Peregrine. It is the entire company that contributed to the significant accomplishments, which the award will honor. There are two people – Mark and I - that will stand up and take receipt of it, but to us it is a company award.

RFMW: Thank you.

John Blyler can be reached at: jblyler@extensionmedia.com

Dr. Ronald Reedy was the founding CEO of Peregrine Semiconductor and now serves as Chief Operating Officer. He had led the microelectronics division at Navy Research and Development and is a co-inventor of UltraCMOS technology. Dr. Reedy received a B.S. and M.S.E.E. from the U.S. Naval Academy and a Ph.D. from the University of California, San Diego.

Dr. Mark L. Burgener was a co-founder of Peregrine Semiconductor and now serves as Vice-President of Advanced Products. He received an Associate's from Cuesta Community College, a Bachelor's in Physics at the University of California, Berkeley, and his Ph.D. at the University of California, San Diego. His Ph.D. thesis was focused on thin film silicon on sapphire electrical properties.

Rodd Novak is Chief Marketing Officer. Prior to Peregrine, Mr. Novak served in corporate marketing for both CTS Corporation and Northrop Grumman. Mr. Novak began his career as an electrical engineer with Comsat Laboratories and later moved to Xetron Corporation. Mr. Novak received a B.S.E.E. from the University of Cincinnati and an M.B.A. from Xavier University.

By Jay Alexander, Agilent Technologies

Creating a Workspace for High-speed Digital Designers

Smartphones and other edge devices rely on an evolving mix of radio-frequency (RF) and digital technologies. On the RF side, digital technology is moving closer to the antenna. In the digital realm, signals behave in unexpected ways as serial data reaches gigabit rates.

In cubicles around the world, these trends are creating varying levels of uncertaintyand discomfort for product developers. Fortunately, there are effective solutions that blend design tools, simulators, and real-world measurements into a virtual workspace that lets designers work with their preferred tools—digital, RF or both.

SCANNING THE ISSUES

In RF design, the encroachment of digital towards the antenna is being driven in part by low-power digital-signal-processing (DSP) engines. These devices enable complex modulation schemes and maximize data bandwidth. For digital designers working at gigabit rates, RF effects can cause a variety of signal-integrity problems. Both types of designers will continue to face the unexpected as smartphones gainever more functionality: multiple cellular standards and formats; Bluetooth; Wi-Fi;GPS;camera; music player; and so on.

Beyond designer discomfort, schedule delays are another undesirable side effect. These are especially problematic in a category such as smartphones, which saw sales growth of 40 percent in 2010. According to some forecasts, that volume could double by 2014.

The situation is equally troublesome in test and measurement. For example, it might seem simpler to deal with a single serial line rather than multiple parallel lines. To move equal amounts of data in the same time, however, serial connectionsmust run at much higher rates than do parallel links.As an added twist, links are again growing wider in standards that use multiple parallel high-speed serial lanes.

HIGHLIGHTING POSSIBLE SOLUTIONS

With high-speed digital circuitry, those who debug and fix glitches will benefit from a toolset that includes both measurement and simulation. To cover digital and RF issues, these tools must operate in the time and frequency domains. Applying measurement and simulation across both domainsprovides multiple views that can reveal underlying problems, suggest solutions, and lead to compliant designs.

One key to success is a combination of software and instrumentation that gives designers the ability to navigate the entire design cycle—design, simulation, analysis, debug, and compliance testing—while also managing signal-integrity issues. This range of tools should let the designer work where he or she ismost comfortable—in the time or frequency domain, and with measurements, simulations or a combination.

As an example, Agilent's approach lets designers shift between time and frequency—or straddle both—to pinpoint the underlying causes of difficult RF/digital problems. With these tools, designers can use measurement data to enhance RF and microwave simulations of tough modeling problems such as crosstalk in densely packed interconnects. They can also combine simulations with actual measurements to optimize performance before hardware is designed or fabricated.

If current technology trends hold, we can confidently assume there will be more RF effects in the digital realm and more digital circuitry encroaching on the antenna. Creating a comfortable place for RF and digital designers to work—and collaborate—starts with flexible measurement and simulation capabilities that span the time and frequency domains.

Jay Alexander is vice president and general manager of the oscilloscope business within Agilent's Digital Test Division. He earned a bachelor's degree in electrical engineering from Northwestern University and a master's degree in computer science from the University of Colorado. He is a licensed professional engineer and a Senior Member of IEEE, and holds 24 US patents.

By Janine Love, Contributing Editor

System-Level Simulation: RF Loses Its Mystery

Today's designers need tools that automatically bring RF blocks to be part of the main system design.

For years, radio-frequency (RF) simulation was typically performed separately and then ported into the system design. In contrast, today's designs require the RF blocks to be part of the main system design. While this change may have caused RF design to lose some of its mystique, system simulation has subsequently become much more complex. Fortunately, simulation software vendors are keeping pace.

RF and microwave simulation tools are evolving to consider the multiple effects inherent in highly integrated designs. In addition, they're offering options to interactively measure during simulation, reducing the need to wait for a final result before making design decisions. These features are combining to speed time to manufacturing. However, Ted Miracco, executive vice president and founder of AWR Corp., warns that we can no longer measure productivity simply by a simulator's solve time. Instead, Miracco argues that a measurement of productivity must encompass everything from schematic entry all the way through to design rule checking (DRC), layout versus schematic (LVS), and final manufacturing.

"Simulation needs to be tightly linked to the design environment and layout," observes Nebabie Kebebew, product marketing manager, Cadence. "Areas like modeling, synthesis, foundry kits, verification against wireless standards, layout, layout verification, links to test equipment, and links to other CAD tools are all part of the mix. This complete flow can be accomplished using a single toolset," adds Charles Plott, product marketing and planning manager, Agilent EEsof EDA Division, Agilent Technologies.

By way of encouragement, Markus Kopp, ANSYS® product manager, electronics, thinks that engineers should be aware of the vast improvements in the accuracy of simulations. "3D RF simulation can give absolute results that are as accurate as measurements," he observes. Kopp goes on to note that the state of the

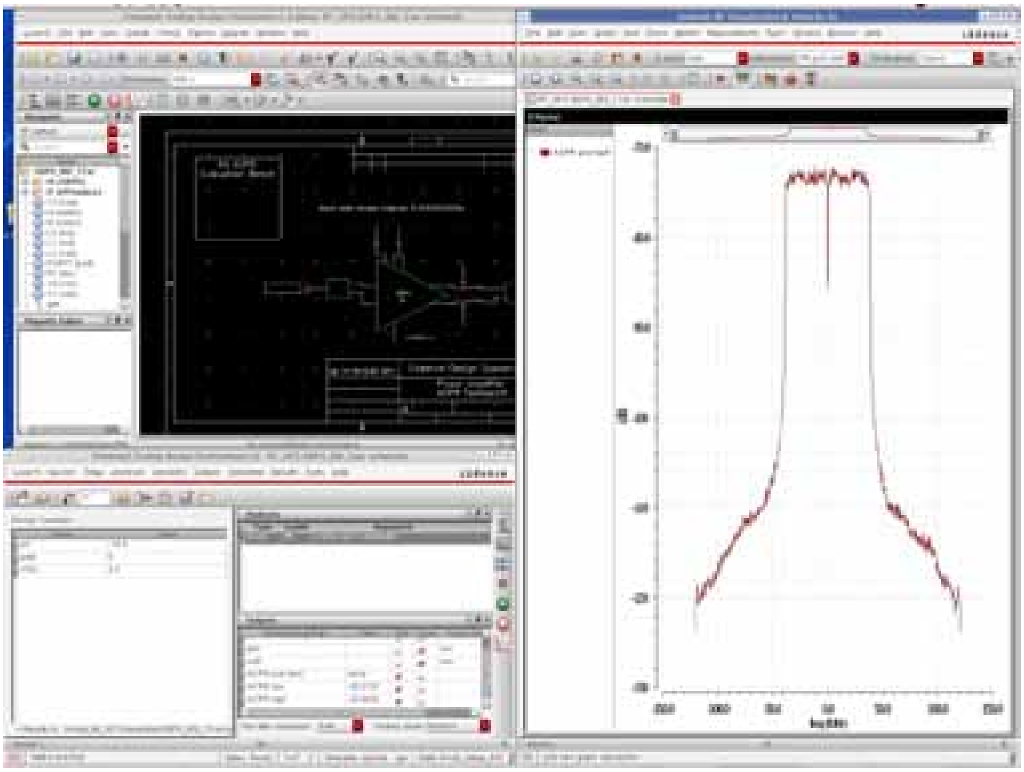

Figure 1: This screenshot is from Cadence's Virtuoso Accelerated Parallel Simulator RF for accuracy and productivity.

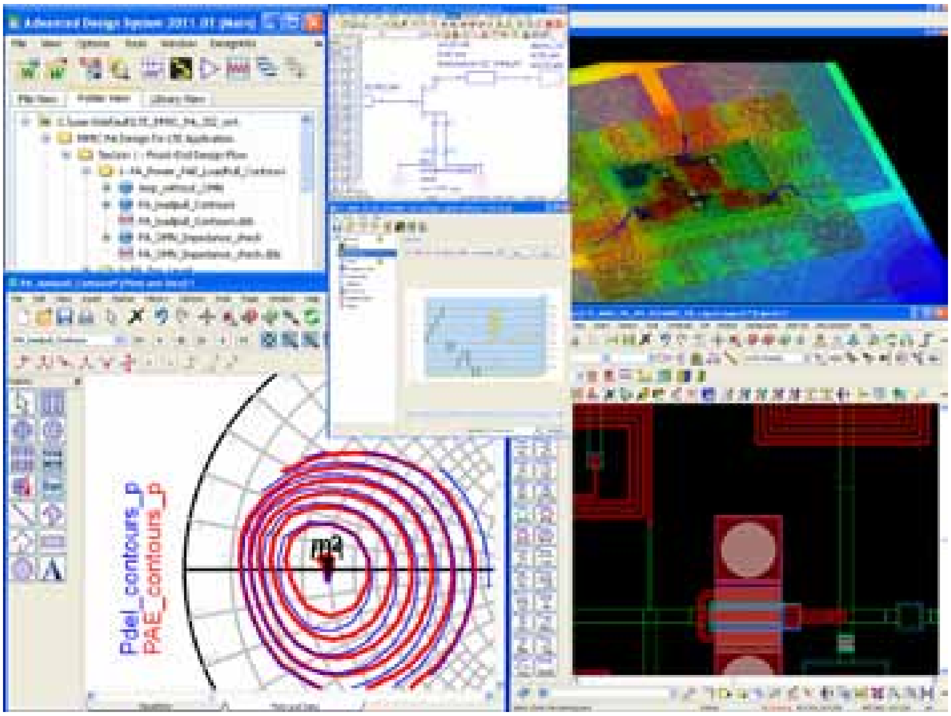

Figure 2: Agilent's ADS 2011 is optimized for functionality, usability, and multi-technology design.

art in simulation technology is no longer just modeling a component or circuit, but an entire system: "It is easily possible to model circuits that include 3D field simulations."

BIGGEST CHALLENGES

Given that RF simulation has grown to the system level, some of the biggest simulation challenges certainly include simulation speed and dealing with integration. Beyond that, 'RF simulation' is now encompassed into the larger system design. So some designers without RF expertise are being asked to model and design RF blocks. Making RF simulation easier while designs become more challenging has become a bit of a conundrum for simulation vendors.

"The biggest challenge today is making 3D full-wave electromagnetic (EM) simulations available to designers not versed in 3D modeling," agrees Kopp. He sees an increase in 3D simulation tools being used by engineers who aren't well versed in RF simulation technologies and concepts.

The impact of subcomponents in highly integrated designs is becoming more of a concern. "The biggest challenge is to do a full chip simulation and know what impact all of the subcomponents have on each other," says Cadence's Kebebew. "When I talk with designers, I find that often, they are not aware of the issues when they tape out. Then, it becomes a guessing game to pinpoint what the problem is."

Unfortunately, time isn't on the designer's side. So speed must be. To quickly achieve increasingly complex simulations, many engineers are taking advantage of multicore or high-performance-computing (HPC) cluster licenses to speed time to design. These new options allow quick and accurate results for multiple RF simulation needs, including linear, harmonic balance, transient, convolution, circuit envelope, data flow, planar EM, and full 3D EM. Agilent's Momentum product for EM simulation, for example, has been enhanced with new algorithms, multicore licenses, and compute farm licenses in order to accelerate simulation. And ANSYS HFSS has HPC options that enable parallel processing for complex models.

Beyond speed and integration issues, AWR's Miracco sees another problem looming for both commercial and aerospace/defense designers: thermal concerns. "Thermal simulations at the MMIC and module level are emerging as a critical simulation challenge. The need today is not only to simulate the junction temperatures of devices, but to make tradeoffs that might reduce temperatures and increase power-added efficiency and extend product MTBFs." Notably, AWR recently signed an agreement to integrate CapeSym's thermal-analysis software into its Microwave Office product.

LOOKING AHEAD

Kebebew sees a great deal of opportunity for RF functionality in the future, thanks to the growing worldwide adoption of 3G/4G protocols, home automation systems, and mobile connectivity. She sees this growing wireless market assisted by CMOS manufacturing supporting a "wireless transformation," where there will be a need to simulate more RF designs at the block level. "This will drive the need for more automation, better accuracy, and comprehensive analysis in RF simulation that is closely linked to the design process from specification to layout."

ANSYS' Kopp sees future challenges growing out of the tablet market, requiring the simulation of new, thinner RF and microwave devices. "These small, thin devices will present design problems where electromagnetic, thermal, and mechanical issues will need to be addressed simultaneously. This will mean that RF engineers need to be able to include thermal-simulation capability directly into their models, and that mechanical engineers will rely on input from RF and thermal engineers."

Today's RF simulation tools take advantage of computing resources, have increased analysis capabilities, are closely linked with other EDA tools, and are integrated into the design flow. They can automate measurement setup and circuit extraction, and they include comprehensive libraries for wireless designs. Clearly, today's designers require all of these features in order to take the mystery out of RF design and bring it into the overall communications design flow. If history is any indication, we can expect RF simulation tool vendors to continue to anticipate and keep pace with changing needs.

SOME TOOLS FOR RF SIMULATION:

MENTOR GRAPHICS:

- **IE3D Signal Integrity:** Full-wave 3D EM design and verification for high-frequency IC, MMIC, package, and PCB designs
- IE3D plus Expedition Enterprise: Provides multiple designers the ability to co-design RF, analog, and digital circuitry on the same PCB

CADENCE:

- **Virtuoso Spectre Circuit Simulator RF:** RF simulation with comprehensive analyses; includes noise-aware PLL analysis and RF measurement library
- **Virtuoso Accelerated Parallel Simulator RF:** high-performance, post-layout, and multicore RF simulation (see Figure 1)

ANSYS:

- **HFSS:** 3D full-wave frequency-domain solver
- **HFSS-IE:** integral equation solver for large, unbounded simulations
- **Designer RF:** for design of microwave circuits and systems

AGILENT:

- Advanced Design System (ADS; see Figure 2)
- **EMPro:** 3D EM simulation
- **Genesys:** RF and microwave simulation software
- **Momentum:** 3D planar EM simulator
- **GoldenGate Software:** RFIC simulation software

AWR:

- **Microwave Office:** RF/microwave software
- **AWR Connected for CapeSym SYMMIC:** electrical-thermal tool combination (see Figure 3)

Figure 3: AWR's Microwave Office & SYMMIC target electrical-thermal simulation.

Janine Sullivan Love is a contributing editor and technical writer. Janine is a member of NASW and ACS and began working as a writer in the RF and microwave field more than 15 years ago.

By Ashok Bindra, Contributing Editor

Portable Apps Drive Integration in Sub-Gigahertz Transceiver Chips

Advances in integrated, short-range radio-frequency (RF) transceivers are enabling the secure, robust, and reliable transmission of data with very low power consumption. Thanks to CMOS process technologies with shrinking transistor geometries, more and more functions are being integrated on the transceiver chip. An example is the 8-bit microcontroller for radio control and data management. In fact, the recent trend has been to put a complete radio transceiver on a single chip for short-range wireless applications, especially in the sub-1-GHz industrial-scientific-medical (ISM) bands.

Key vendors advancing the level of integration on RF transceiver chips for short-range wireless applications include Analog Devices Inc. (ADI), Silicon Laboratories, Semtech, and Texas Instruments (TI), to name a few. In partnership with third-party turnkey solution providers, these RF transceiver suppliers are delivering complete radio solutions for applications ranging from metering systems for electric, water, and gas utilities to home and building automation and industrial wireless control.

In the sub-gigahertz range, ADI (www.analog.com) has readied a new RF transceiver chip, labeled ADF7023-J. It has been optimized for Japan's ARIB STD-T96 protocol for wireless data transmission in the 902 to 958-MHz frequency range. Established by Japan's Association of Radio Industries and Businesses (ARIB), the ARIB STD-T96 is specified for the automatic transmission and measurement of data

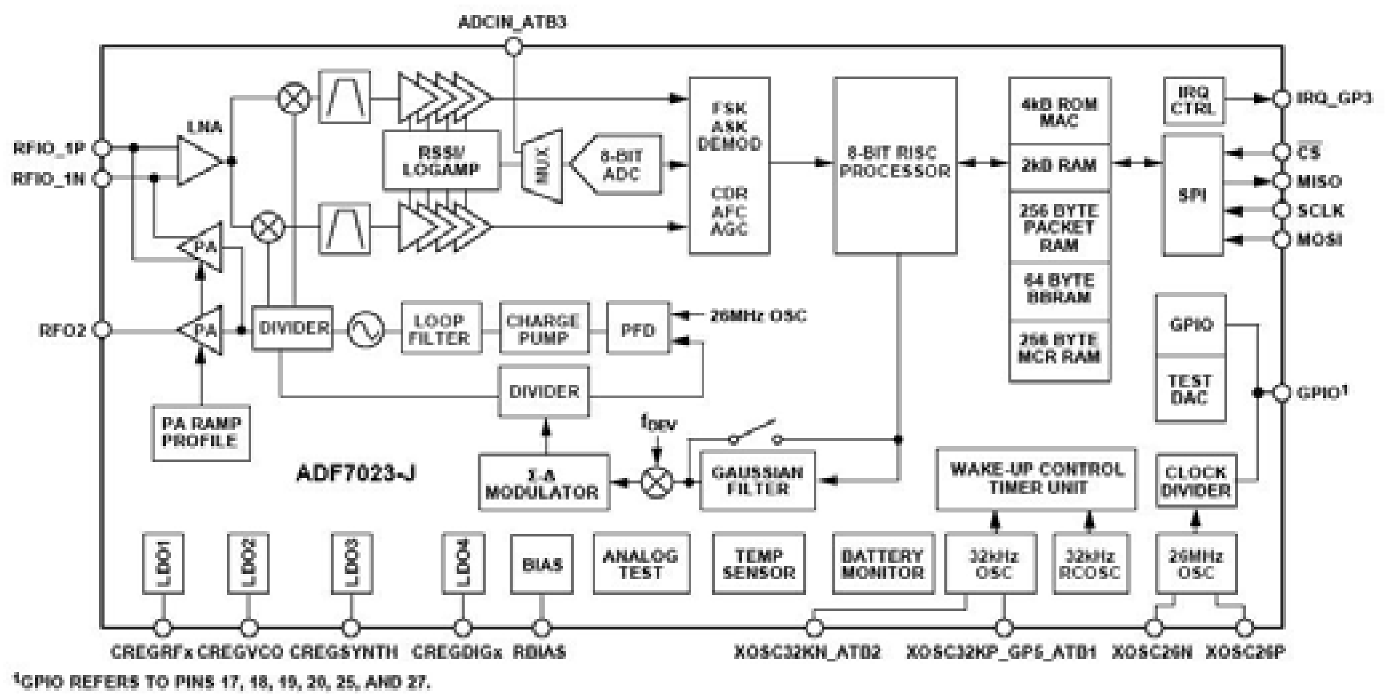

Figure 1: This sub-gigahertz transceiver chip comes with a built-in 8-bit microprocessor. An on-chip processor supports a number of RF functions, including radio control and packet management.

from remote sources by low-power radio equipment. The device, in fact, operates in both the 950-MHz and 915-MHz bands. It's implemented in a CMOS process and comes with a built-in, low-power 8-bit processor that supports a number of RF functions. Examples include radio control and packet management. The 8-bit processor is firmware-programmable with the ability to execute firmware modules or system-upgrade patches from internal RAM (see Figure 1).

This feature allows the factory to develop upgrade modules that the user can download in the field, explains Des O'Donnell, product marketing manager for ADI's RF Group. According to O'Donnell, this is a very useful feature in applications where industry standards may be in flux and products can be upgraded without silicon changes. "This eliminates the need to constantly iterate silicon to accommodate transient market requirements and allows designers to focus on real performance improvements," notes O'Donnell.

As a result, it provides designers with the flexibility to respond to protocol standard evolution and maintain system robustness. Because the ADF7023-J can be used in autonomous packet mode or bypass mode, it permits the user to work with an external controller for implementing enhanced protocols.

Other key features of the RF transceiver include low transmit and receive current, data rates in 2 FSK/GFSK up to 300 kbits/s, superior blocking resistance, and high receive sensitivity. The high blocking performance and receive sensitivity enable the transceiver to operate in environments where interfering signals are significantly stronger than the source signal.

Operating with a power supply range of 1.8 V to 3.6 V, the RF transceiver chip has low power consumption in both transmit and receive modes, enabling longer battery life. The device consumes 24.1 mA when transmitting at 10 dBm and is capable of outputting 13.5 dBm. "More important is the receive current consumption of 12.8 mA, as it is predominantly the receive current consumption which determines the battery life of the system," says O'Donnell. He adds, "For systems requiring higher output power, the device provides a biasing circuit for interfacing to an external power amplifier (PA)."

When compared to alternative solutions, the ADF7023-J RF transceiver offers better transmit filtering and lower phase noise. It also enables ARIB STD-T96 system designers to develop systems that transmit at maximum transmission power while meeting standard requirements with good margin.

The ADF7023-J is derived from a general-purpose sub-gigahertz transceiver, the ADF7023. It offers the flexibility to operate in multiple bands (862 to 928 MHz and 431 to 464 MHz) with different modulation schemes and data rates. "The ADF7023 family already has the lowest power consumption for the level of performance offered and this is just one of the features we intend to further improve," notes O'Donnell. It's suitable for circuit applications that operate under the European ETSI EN300-220, North American FCC (Part 15), Chinese short-range wireless regulatory standards, or other similar regional standards.

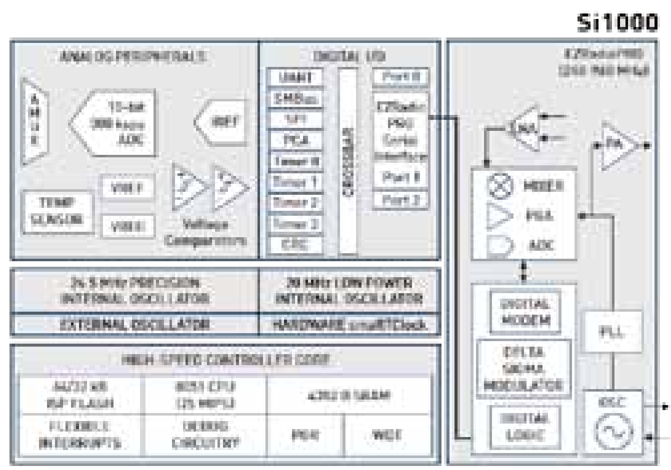

Figure 2: Fabricated using 0.18-µm CMOS, this wireless MCU combines a low-power 25-MHz 8051 processor core with a sub-gigahertz RF transceiver in the same package.

Using 0.18-µm CMOS technology, Silicon Laboratories (www.silabs.com) has developed a wireless MCU that combines an ultra-low-power, 25-MHz 8051 processor core with a high-performance, sub-gigahertz RF transceiver called EZRadioPro (see Figure 2). The RF transceiver and the microcontroller functions are on separate dies, but housed in a single 5 x 7-mm package. To keep current consumption low for battery-powered applications, the EZRadioPro transceiver (Si4432) incorporates on-chip low dropout (LDO) voltage regulators. This also permits a wide operating supply voltage range of 1.8 to 3.6 V. In addition, the microcontroller die incorporates the switch-mode

DC-DC converter that's used to power both the MCU and radio functions of the wireless MCU, labeled the Si10xx.

With smaller geometries, the RF transistors operate on lower voltages to keep current consumption low. On-chip LDOs ensure that the supply voltages are within tolerance. The partitioning of functions on-chip is dictated by gate speed, RF performance, and nonvolatile memory, says Keith Odland, Silicon Labs' microcontroller product marketing manager. It is the process node that optimizes all of these functions, adds Odland.

The EZRadioPro transceiver Si4432 incorporates a PA to deliver output power of up to 20 dBm with low current consumption. On the receive side, it includes a low-noise amplifier (LNA), mixer, and analog-to-digital converter (ADC), along with other required features to operate continuously over a frequency range of 240 to 960 MHz. Also included are built-in features, such as a wake-up timer, low battery detector, transmit and receive data FIFOs, power-on reset circuit, and general-purpose digital I/Os.

Antenna design for the end application is crucial, states Ross Sabolcik, Silicon Labs' director of marketing for wireless products. "Getting the right antenna that meets the end requirements is critical," asserts Sabolcik. Consequently, he adds, EZRadioPro provides a flexible antenna interface. Also, there are application notes that guide the user in getting the right antenna for the end solution.

To provide cost-effective, turnkey wireless-networking solutions for bidirectional and one-way link applications, the company has been collaborating with module makers like California Eastern Laboratories (CEL), Hope Microelectronics, IMST, and Telit Wireless Solutions. Target applications include smart meters, in-vehicle anti-theft alarm systems, home automation systems, HVAC control units, residential security systems, high-speed data acquisition systems, and wireless toys. Telit, for instance, is combining Silicon Labs' Si443x transceivers with an MCU, matching network, and software to deliver a complete module for one- or two-way data exchange with gas, water, heat, and electricity meters and concentrators.

Operating in the 868-MHz band with ultra-low power for maximum battery life, the Telit module, labeled ME50-868, features wireless M-Bus transfer technology. It is compliant with EN13757 parts 4 and 5 of the wireless M-Bus standard. This pre-certified RF module comes in a land-grid-array (LGA) format. The ME50-868 is pin-to-pin compatible with Telit modules in the ZE, NE, and LE families. With a link budget of 122 dB, the module provides a range of 2000 meters.

"The combination of short-range and cellular capabilities is the key technology for future machine-to-machine (M2M) applications. Companies using short range for their smart meters do not have to buy expensive SIM cards to transmit their data; they can use the free data transmission via radio frequencies," says Felix Marchal, global VP sales at Telit Wireless Solutions. "Companies using Telit's gateway solution to combine their short range with cellular data transmission can fully overcome the short-range limitations. Such integration provides companies a crucial solution at low cost and energy efficiency to meet all customer requirements."

Using standard 0.18-μm CMOS technology, Semtech (www.semtech.com) has released an integrated RF transceiver capable of operation over a wide frequency range, including the 433, 868, and 915-MHz license-free ISM bands. Its highly integrated architecture allows for a minimum of external components while maintaining maximum design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set, according to Marc Pegulu, director of Semtech's wireless and sensing product line. The SX1231 offers the unique advantage of programmable narrowband and wideband communication modes without the need to modify external components. According to Pegulu, the SX1231 also offers low power consumption while delivering high RF output power and channelized operation for maintaining links over an extended range. The transceiver chip guarantees a range of about 600 meters.

To enable reliable transmission over hundreds of meters, the transceiver chip offers a high link budget of 137 dB with receive sensitivity of -120 dBm, along with transmitter output power of 17 dBm. When combined with on-chip digital filtering and a low-phase-noise

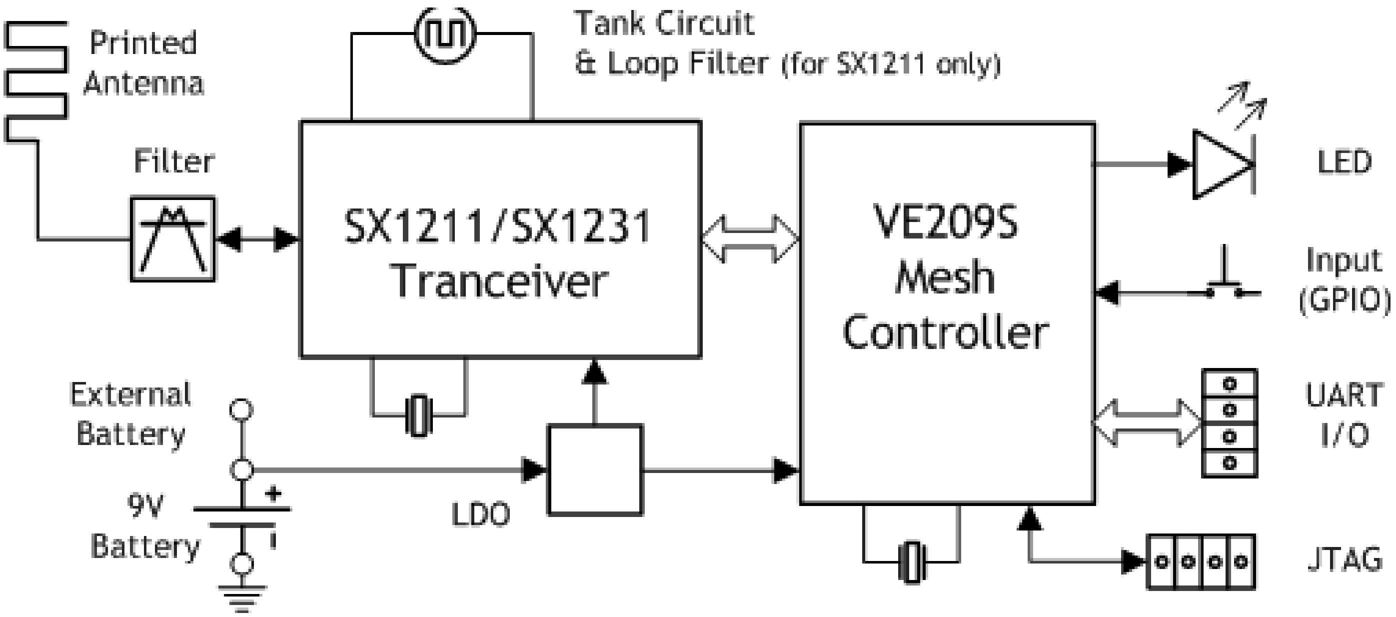

Figure 3: A typical VEmesh unit (gateway or node) uses Virtual's mesh controller with Semtech's RF transceiver.

phase-locked loop (PLL), the transceiver performs well even in the presence of interference, explains Pegulu. Typical receive-mode current consumption for the SX1231 is rated at 16 mA while transmit-mode consumption is 95 mA (typical) at 17 dBm output power. Typical current consumption in sleep mode is rated at 0.1 µA.

Like others, Semtech is working with module makers to offer a complete solution for these applications. Recently, the supplier partnered with Israel's Virtual Extension. They combined the sub-gigahertz, ISM-band transceiver chip, the SX1231, with Virtual's IP-based mesh controller, the VE209S, to develop a wireless mesh-network platform. Called VEmesh, this wireless network provides reliable bi-directional communication and impressive range and coverage for the distributed monitoring and data collection of smart lighting, smart metering, sensor systems, and a wide range of remote-control applications (see Figure 3).

For optimal performance in the presence of obstructions and propagation interference, the VEmesh architecture combines frequency hopping with flooding technology. In this topology, all nodes within the range re-transmit simultaneously. Transmissions from different paths sum up at the receiver.

Others in the race to deliver integrated sub-gigahertz transceiver chips for short-range communication links include TI (www.ti.com) and Nordic Semiconductor (www.nordicsemi.com). TI recently demonstrated a narrowband RF transceiver at Embedded World in Nuremberg, Germany. Featuring range significantly beyond 10 km (137-dB link budget) and more than 60-dB adjacent-channel rejection, the CC112x family provides a solution for ISM frequency bands at 169, 433, 868, 915, and 950 MHz. The CC112x family targets low-power wireless applications in alarm and security, automatic meter reading, industrial monitoring and control, and home and building automation. TI is working closely with module maker Radiocrafts to launch the first complete module based on the CC112x.

Ashok Bindra is a veteran writer and editor with more than 25 years of editorial experience covering RF/wireless technologies, semiconductors and power electronics. Prior to becoming an editor, Bindra worked in industry as an electronics engineer. He holds an M.S. degree from the Department of Electrical and Computer Engineering, Clarkson College of Technology (now Clarkson University), and an M.Sc (Physics) from the University of Bombay, India. He can be reached by email at bindra1[at]verizon.net.

By David Lester, Freescale Semiconductor

LDMOS RF Power Transistors Face up to 65:1 Impedance Mismatches

Specialized applications can turn ordinary RF power devices to dust.

Today's RF power transistors are assumed to be able to operate without failure into a 10:1 voltage-standing-wave-ratio (VSWR) impedance mismatch. This condition would usually indicate a major problem somewhere in the transmission chain. However, some applications present far worse impedance mismatches as part of normal operation and would turn most RF power devices to dust. These applications—plasma generators, laser exciters, RF heating and sealing equipment, magnetic resonance imaging (MRI), and RF plasma lighting systems—encounter conditions in which nearly all of the RF power they generate is reflected back to the amplifier.

When all of the power generated by their RF power transistors reaches the load, RF power amplifiers (PAs) operate most effectively, have optimal reliability, and have the longest operating lifetimes. Under ideal conditions (a VSWR of 1:1), all of the power reaches the load with none reflected back to the amplifier. This rarely, if ever, occurs in fielded systems, but impedance mismatches of 2.5:1 are expected. A 5:1 or 10:1 ruggedness rating for the RF power device is adequate.

A "classic" MRI system is depicted in Figure 1a. MRI systems are based on powerful magnetic fields to align the magnetization of atoms in the body. Very high RF fields generated by the PAs alter the magnetization alignment. This causes the nuclei to produce a rotating magnetic field that can be detected by the scanner and recorded to construct an image of the scanned area.

RF plasma lighting systems (see Figure 1b) are used as one of several techniques to generate light by exciting a plasma inside a closed transparent bulb with an RF source, which was, until recently, a magnetron. A waveguide constrains and focuses the RF field into the plasma container. The gas is ionized, and free electrons (which are accelerated by the electrical field) collide with the gas and metal atoms. Some electrons in the gas and metal atoms are excited by these collisions, increasing their energy state. When the electron falls back to its original state, it emits visible light.

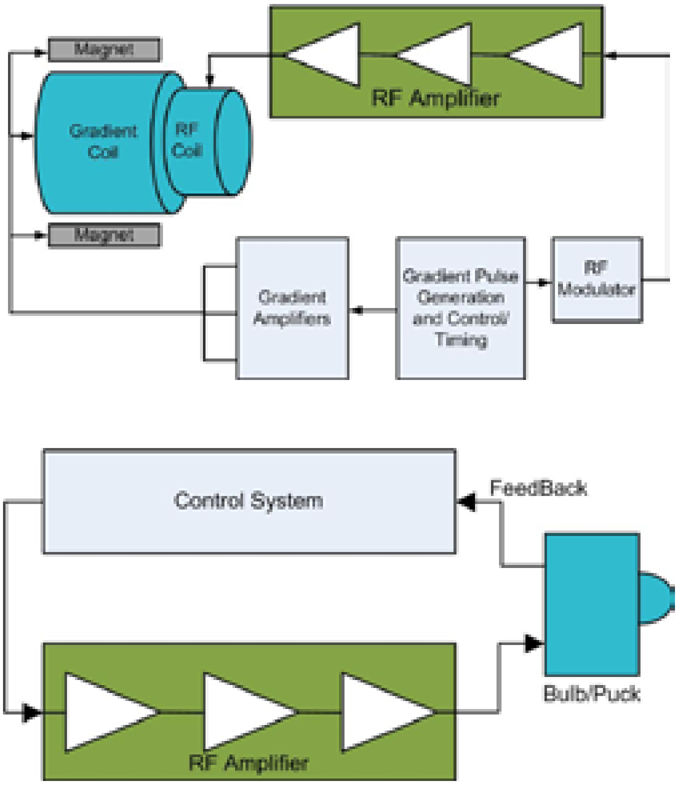

Figure 1. A typical MRI system (a) employs RF amplifiers to produce high electromagnetic fields. An RF plasma lighting system (b) uses RF PAs to produce energized plasma.

RF heating systems have been used for many years to seal plastic packages, dry food products during production, and a variety of other applications. They also rely on high-power amplifiers. Plasma generators and CO_2 lasers use RF or microwave energy for system ignition.

These systems are far more demanding than comparatively tame wireless base station amplifiers, both in terms of absolute power level and the ability to deliver that power under adverse conditions. Consequently, they require very rugged devices that can operate reliably under adverse conditions. Until recently, the only devices robust enough to withstand these conditions were silicon bipolar junction transistors (BJTs) or traveling-wave-tube amplifiers (TWTAs). Progress in the aforementioned applications continues to move forward. But silicon BJT is rapidly being displaced as development is focusing on other semiconductor technologies—principally LDMOS and GaN. The TWTA is still employed in some defense systems and communications satellite transponders. As it is comparatively expensive and has a finite operating lifetime (one-tenth that of a semiconductor device), the TWTA is also being displaced by newer semiconductor technologies.

The extremely rugged LDMOS FETs developed by Freescale, for example, have specific properties designed to handle impedance mismatches encountered in the applications described previously. These mismatches are orders of magnitude greater than those encountered in more "mainstream" applications. The first of this new family of devices was Freescale Semiconductor's 50-V MRFE6VP6300H/S. It operates over the 1.8- to 600-MHz frequency range with 300 W CW output power, 80% efficiency, and 25 dB of power gain.

The device can deliver its full rated power, even with a 65:1 mismatch and when driven by twice its rated input power. As a result, the MRFE6VP6300H/S became the first LDMOS contender for use in high-VSWR applications, where the gain, efficiency, reliability, and proven track record of the LDMOS topology are key selection factors. The increase in supply voltage from 28 to 50 VDC is a major determinant in allowing the devices to achieve such high power levels under hostile operating conditions. However, this isn't the only reason, as other proprietary techniques developed by the company together are equally important.

While an output power of 300 W is suitable for many systems, even higher power levels may be desired to allow LDMOS devices to move into other applications. To serve these needs, Freescale developed the 1250-W MRFE6VP61K25H/S and 600-W MRFE6VP5600H/S 50-V LDMOS devices for operation from 1.8 to 600 MHz (see Figure 2). The MRFE6VP61K25H/S has more than 22dB of gain and efficiency greater than 74% and the MRFE6VP5600H has more than 24dB of gain and efficiency greater than 74% under similar conditions.

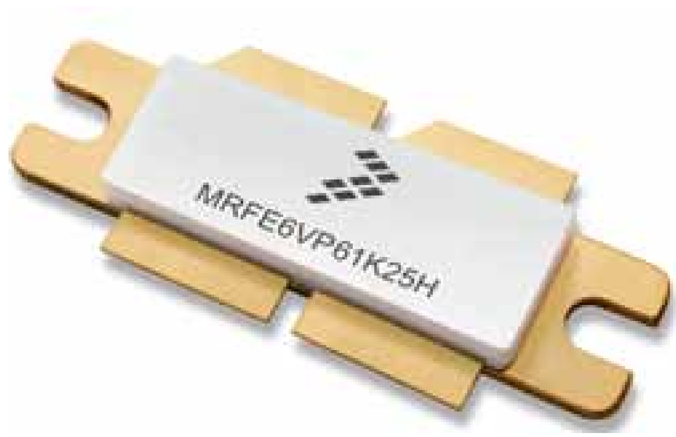

Figure 2. The MRFE6VP61K25H/S delivers 1250 W into a 65:1 VSWR even under 3-dB overdrive conditions.

All three devices employ electrostatic-discharge (ESD) protection. It allows for an ample gate-source voltage range (-6 to +10 VDC), enhancing performance when operating in high-efficiency modes such as Class C. They can be used in push-pull or single-ended configurations. The MRFE6VP6300H is housed in a NI-780-4 package and the other two devices are housed in the larger NI-1230 package. Both package types offer an earless option for applications in which the flange is soldered down. They are in full production and designers can avail themselves of reference designs and other support tools at www.freescale.com/rfpower.

David Lester is technical marketer for Freescale Semiconductor's RF Division with responsibility for industrial, scientific, and medical applications. He earlier provided expertise to the company's cellular products and sensor divisions. David has 25 years of experience in the set-top box industry and 9 years of experience in digital video and conditional access systems.

By Cheryl Ajluni, Contributing Editor

Return Of The Femtocell

Resolving key issues are critical for the femtocell industry to take its rightful place on the road to 4G.

Nothing has been left unscathed in the current global economic downturn, and that includes femtocell deployments.

It was just last year that femtocells were being proclaimed a 2009 "killer app," along with LTE and WiMAX. But what was once viewed as the next great thing has instead faced a tough road with more than a few large-scale deployments by major mobile operators being put on hold. Despite the slowdown, femtocells remain a viable part of the road to 4G. According to Aditya Kaul, senior analyst at ABI Research, while the pace of adoption has been slow, "deployments in 2010 will pick up." In fact, ABI Research forecasts that the total available femtocell market in 2010 will reach 2.3 million units and rise to 40 million units by 2014.

Adding fuel to the slow-burning fire of the femtocell market is movement on the part of carriers, which may signal that things are heating up once more. Comcast, for example, announced that it is testing WiMAX femtocells. And across the globe, China Mobile has partnered with Nokia Siemens Networks to test a TD-LTE femtocell. This year, six major network operators have launched femtocell services that cover the USA, Europe and Asia.

Such activities bode well for the emerging femtocell market, but do little to address designer's challenges at a system level. From a technical perspective, femtocells are no more complex than a full macro base station, yet they demand the integration level of a WLAN in order to meet various cost, power and footprint requirements. And, since femtocell products are likely to appeal to many different users around the world, each with potentially different needs and requirements, different models will need to be developed. Each model (e.g., a W-CDMA, WiMAX or LTE femtocell) will have its own unique design requirements and challenges determined by the standard it supports. Such challenges make designing femtocell products a difficult and risky proposition, and demand solutions that can ease the burden on the system designer.

As Caroline Gabriel of Rethink Research, explains "The femtocell market is starting to mature. While the sophisticated early entrants wrote their own solutions, this is bringing an inevitable demand from developers for more complete system solutions that reduce risk, enable differentiation and speed time-to-market. This is a value chain dynamic that other semiconductor markets such as Wi-Fi and DSL also experienced as they hit the mass-market."

picoChip is working on just such a solution—an end-to-end femtocell reference solution for both HSPA and LTE that's aimed at tackling the designers' system-level challenges, including interference management, security, timing, and provisioning. The solution integrates optimized versions of Continuous Computing's protocol stacks with picoChip's SoC products (Figure 1). It also includes sophisticated femtocell management software for the complex control functionality required by femtocells.

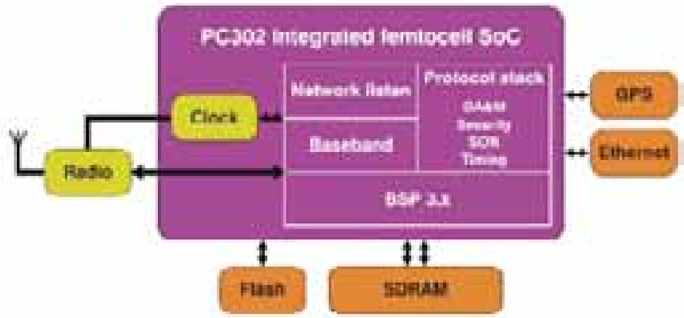

Figure 1. The four-user PC302 residential femtocell is the first in picoChip's PC3xx family of highly integrated baseband SoCs. It implements a complete 3GPP Release 7 access point, is compliant to TR25.820 and the newly standardized Iuh interface, and is built using an advanced 65-nm manufacturing process.

Of course, even the availability of a complete femtocell solution with things like automated interference management and network self organization, does not exempt the designer from having to consider some fairly difficult issues during femtocell design. Some of these issues include:

Power Consumption: By definition, femtocells are low-cost, low-power wireless access points that operate in licensed spectrum to connect standard mobile devices to a mobile operator's network using residential DSL or cable broadband connections. Power is an especially critical concern since in a residential situation the end user has to pay the bill for the electrical energy consumed by the femtocell base station. Its power consumption therefore, has to be low enough to not significantly impact the user's bill. Various low-power design techniques such as comprehensive power-down modes and clock gating, as well as effective power management can be employed to achieve this goal.

Interference: Because femtocells utilize spectrum currently employed by macro networks, interference can result between cells (e.g., a macrocell with a femtocell or a femtocell with another femtocell, when two units are in close proximity). Interference affects operators as well as consumers who will likely move their femtocells around or place them next to other devices.

There are a couple of ways to mitigate the risk of interference. The first, cognitive radio technology, essentially allows the femtocell's radio to constantly monitor its RF environment and set itself up accordingly. Another option calls on the femtocell to intelligently set its output power when it's in the presence of nearby femtocells. In this case, each femtocell would need to transmit at lower power to avoid same-frequency interference. To avoid interference with signals from neighboring macrocell base stations operating on an adjacent channel, the femtocell can be designed to measure the power in the adjacent channel downlink and set its own power accordingly.

Standards: These are key to taking a technology from a niche application to wide-scale adoption. The question with regard to femtocell technology is which standard—a proprietary approach, an existing standard from the telecom industry (e.g., the session initiation protocol (SIP)/IP multimedia subsystem standard for integration used in LTE networks), or some other standard altogether?

The Femto Forum, 3GPP and the Broadband Forum think they have the answer. It's the world's first femtocell standard and they created it together. The standard, part of 3GPP's Release 8 and interdependent with Broadband Forum extensions to its Technical Report-069 (TR-069), was officially released in April and paves the way for not only the development and production of large volumes of standardized femtocells, but also for ensuring interoperability between different vendors' access points and femto gateways. It covers four main areas: network architecture (the Iuh), radio & interference aspects, femtocell management/provisioning via the popular TR-069 protocol, and security (e.g., IKEv2 and IPsec).

Handovers: These can be tricky, especially in the case of femtocells where precise timing and synchronization is need to properly manage handovers with the macro network. The process is complicated by the fact that there may be millions of femtocells deployed and end-users may move them around their homes, entering into areas where the signal strength from the macrocell is greater than that of the femtocell. Unfortunately, existing macrocell RF planning techniques offer no real solution. Instead, femtocell handovers require sophisticated algorithms capable of ensuring that the network quality is not impacted by inefficient handovers and wasted capacity.

These issues are just some of the challenges system designers face when developing femtocell products today. Addressing them, whether by using the techniques suggested or through a complete femtocell solution like the one picoCell is working on, will be critical to ensuring not only successful femtocell products, but a successful femtocell industry that can take its rightful place on the road to 4G.

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By Nebabie Kebebew, Cadence Design Systems Inc.

RFIC Complexity Demands an Advanced RF Analysis and Design Environment

It is possible to enable first-pass silicon realization for RFICs.

In the design of an analog/radio-frequency integrated circuit (RFIC) for applications that meet the modern-day consumer's desires and requirements, engineers must confront changes in the complexity of the specifications, silicon process technologies, and methodologies required. The complexity of an RFIC design comes, in part, from the wireless transformation that's taken place with the advent and adoption of wireless protocols—particularly the baseband, which covers 3G and 4G (LTE and WiMAX)—along with the cost-effective CMOS silicon manufacturing process needed to realize the silicon.

Wireless technologies and handheld gadgets like the smartphone have changed the way we live. Consumer demand for mobility and connectivity is at the heart of today's technological innovation. Satisfying such demands requires higher levels of integration and lower power consumption—especially for RFICs that plug into mobile devices. This, in turn, drives the need for the continuous reduction in CMOS silicon geometry size from 180, 130, and 90 nm just a few years ago to today's advanced nodes at 65, 45/40, and 32/28 nm.

COMPLEXITY

The sheer complexity resulting from multiple wireless protocols, high-frequency systems with many radio elements, and advanced-node technologies presents significant challenges for the everyday RFIC designer. For instance, large RFICs like wireless transceivers contain analog and digital functions that include data converters (DACs and ADCs), voltage-controlled oscillators (VCOs), phase-locked loops (PLLs), mixers, filters, amplifiers, and automatic-gain-control (AGC) loops. Characterizing such functions requires detailed simulation that takes days or even weeks.

This complexity is exacerbated by the parasitic effects introduced during layout. Simulating multiple radio elements that are cascaded to form a complete transceiver chain increases the simulation time exponentially. This forces the design team to make a difficult choice: delay the schedule to ensure first-pass silicon success, or compromise the required, exhaustive RFIC simulation and introduce the risk of respins.

ADVANCED ANALYSIS

The exhaustive simulation of an RFIC requires a simulator with unique and comprehensive analysis capabilities that's integrated with the design environment. The simulator has to converge on accurate results and provide capacity and performance. Only such an advanced simulator can reduce runtime from days to hours and minutes when handling the large numbers of transistors and parasitic elements introduced from layout, bond wires, and device models.

The analysis techniques in an RF simulator should be in both the time and frequency domains with engines that can handle both the nonlinear and linear behavior of RF circuits. For faster simulation results, an oscillator's phase noise, a mixer noise figure, and the effects of harmonic distortion and gain compression are best simulated and reported in the frequency domain. Other behaviors (switching, initial startup, and transceiver response to instantaneous events like frequency hopping) need to be analyzed and reported in the time domain.

To verify the functionality of a digitally modulated RF circuit, the design team needs a mixed-signal circuit simulator with RF analysis. RFICs that operate at high frequencies are susceptible to coupling between passive devices, layout parasitics, substrate coupling effects, and IC packaging and noise from the power supply. Hence, characterizing these effects accurately with an electromagnetic simulator is an imperative step toward ensuring first-pass silicon success.

DESIGN ENVIRONMENT

To meet the productivity metric, the design team requires a holistic RF design environment to manage and control the simulation and facilitate collaboration between designers and layout engineers. Key capabilities of such an advanced design environment include the following: easy setup of RF and other complex measurements; the ability to analyze these measurements over a variety of conditions and corners; and the ability to quickly generate the physical layout. To ensure that the RFIC is meeting its intended specifications, the ability to extract the parasitic and easily verify the "real" RF circuit in the context of the earlier measurements is necessary as well.

There are many facets to the challenges faced by RFIC designers. The exponential growth in RF functionality dictated by the wireless transformation demands an advanced RF analysis and design environment to help the design team achieve first-pass silicon success.

Nebabie Kebebew is a senior product manager for Custom IC Simulation products in the Silicon Realization Group at Cadence Design Systems, Inc. She has worked on analog circuit design, digital ICs and analog/RF design methodology. She received a BSEE from California Polytechnic University and an MSEE from University of Southern California in Communications System Design.

Differentiation and Co-existence in WiMax and LTE

By Cheryl Coupé, Embedded Editor

In his article "The Era of Wireless Broadband," EE-Catalog editor Cameron Bird compares expectations and realities of WiMax and LTE deployments. While forecasts ebb and f low, a clear global directive is yet to emerge. Fortunately, designers still have plenty of opportunities to differentiate product offerings that support both standards. Recent design advances support both LTE and WiMax wireless access technology on the same platform, which will help operators that need the f lexibility to support either co-existence or migration, and can help reduce costs with components that are common to both standards. EECatalog talked to Declan Byrne, director of marketing for the WiMAX Forum, about the opportunities designers have to differentiate products and take advantage of commonalities.

EECatalog: What are the opportunities for designers to improve on existing equipment, such as base stations, that underlie WiMAX and LTE?

Declan Byrne, WiMAXForum: Designers have tremendous opportunity to innovate and differentiate their base stations in any number of well-understood ways, beyond the scope of simple interoperable specification. Vendors develop implementations that optimize base station air interface resource scheduling to maximize air interface throughput efficiency, Quality-of-Service, reduce terminal power consumption, improve mobility success and efficiency, and reduce inter-cell interference, among other considerations.

Designs can also differentiate through the sophistication of antenna implementation, interference mitigation and inter-cell coordination, and a wide range of channel coding and signaling selection. There are many similar examples across the board. The air interface and network interoperable specifications set a minimum performance communications model, as a base. These specifications also provide a toolkit of interoperable features and functions that designers can use as building blocks, picking and choosing pieces that enhance their specific implementation. Finally designers can add their own solutions on top of all of that, enhancing the products in ways not necessarily defined or even envisioned by the interoperable specifications.

To read the entire story, please visit: www.chipdesignmag.com/rfmw

By James Nelson and Mark Andrews, TriQuint Semiconductor

Microwave Links Offer an Elegant Backhaul Solution

Wireless carriers must increase backhaul capacity while managing capital and maintaining customer satisfaction.

Truly high-speed wireless data is now being brought to smartphone users via HSPA+, LTE, and WiMAX. It's finally making possible what carriers have been promising for years: streaming video, painless web browsing, and fast file uploads and downloads. The consumer never sees (or probably even knows or thinks about) the other half of the network, in which the traffic from each cell site is sent to a central point. There, it's merged with the rest of the global communications matrix. Nevertheless, without this inelegantly named 'backhaul' system, there would be no second "wireless revolution:" the ongoing global connectivity bonanza that's driving communications to a level that's never been possible before.

Considering the massive amounts of data generated by these newly enabled services, the obvious transmission choice for backhaul is optical fiber. But most cell sites aren't near a fiber node. And some may never be close enough to capitalize on the bandwidth that nodes afford. In these and other cases, microwave point-to-point (PtP) links that operate in bands from 3.5 to 86 GHz will be an excellent solution. Their data rates rise from today's 750 Mbits/s per radio to achieve even higher throughput.

Microwave radios have been employed by telephone companies to send voice, video, and data for decades. They remain one of their key assets. The radios also are used in applications as diverse as traffic webcams and radio and TV electronic news gathering (ENG) in the broadcast industry. However, they haven't been used as much for cellular backhaul (at least in the U.S., where T1 lines are typically employed).

The opposite is true in Europe, where PtP links power more than 70% of wireless backhaul and globally account for about 50%. While T1 lines are expensive in the U.S., they're even more expensive elsewhere (or not available), making microwave an appealing choice. However, this scenario is changing fast in the U.S. because T1 lines are ill suited for IP-based packet communications (wireless data). Additionally, their bandwidth simply cannot handle the data onslaught that "4G" services are creating. Add to that the cost and time required to deploy T1 or all-fiber systems, which typically exceed that of microwave radio solutions, and one can quickly grasp how network operators will meet backhaul capacity requirements in the future.

To illustrate the intensity of this data deluge and how much more intense it will soon become, consider Cisco's Visual Networking Index (a respected source of wireless industry statistics). Cisco projects that mobile-data traffic will increase at an annual rate of 92% to yield a 26-fold increase by 2015. It will reach 6.3 exabytes per month that year, which is 6.6 million terabytes (see Figure 1). The company projects that mobile-network connection speeds will rise by a factor of 10 by the end of 2015. Tablets alone, which only recently exploded into the market, will create 248 petabytes of data per month (about the same as last year's total global mobile-data traffic).

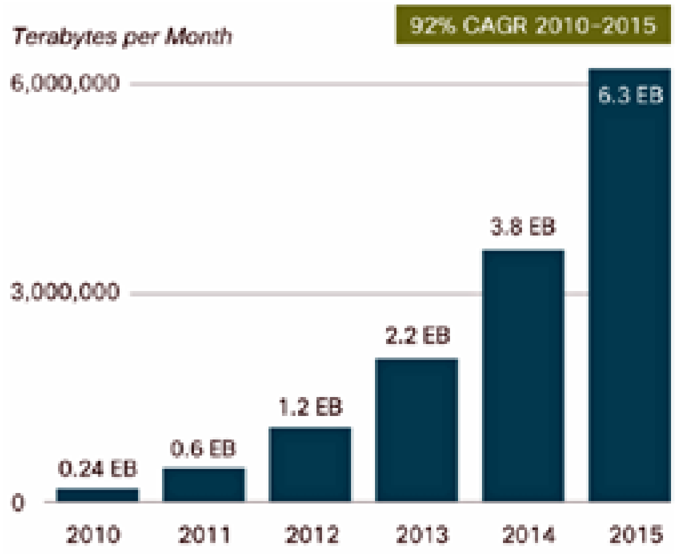


Figure 1: Cisco forecasts mobile-data traffic of 6.3 exabytes per month by 2015. Source: Cisco Visual Networking Index

These are astronomically large amounts of data. Only fiber and microwave PtP links have the intrinsic backhaul capacity to satisfy such gigantic data-transport requirements. In short, fiber will be used where it's available. Where it isn't, microwave PtP links will supply the solution. Where a fiber node can be reached via a single microwave "hop," both technologies will be employed.

The plot thickens, as carriers are adding large numbers of microcells and picocells to complement their traditional macrocells to fill coverage gaps. This trend creates its own backhaul challenge. The potential revenue bonanza it presents has gotten the interest of cable MSOs with their installed base of hybrid fiber coax (HFC). They already generate about $200 million in backhaul revenue and serve more than 11,000 cell sites in the U.S. Another company has developed a system based on IEEE 802.11n (WiFi) operating at 5 GHz. It forms a PtP or meshed PtP using "smart" high-gain antennas and beamforming.

Meanwhile, manufacturers of microwave radios have been honing their products to deliver more compact, cost-effective solutions that deliver higher power and consume as little power as possible. The latter goal is extremely important, as carrier electricity bills are already one of the largest operational costs for most networks. Two of the key elements in achieving these goals can be found in radios' RF amplifiers and RF power transistors.

Figure 2: This 2.5-W packaged power amplifier is designed for 10/11-GHz PtP microwave radio.

For example, TriQuint Semiconductor continues to expand its line of packaged RF power devices dedicated to microwave PtP applications. Recently, the company introduced three new RF power amplifiers (PAs) for PtP radio bands at 10, 11, 13, 15, and 23 GHz. They combine high RF power output, linearity, and gain with low power dissipation. The product line complements the company's optical-modulator driver amplifiers for 10, 40, and 100-Gbit/s fiber-optic systems that also are targeted for backhaul applications.

The new TGA2535-SM is a 5 x 5-mm, QFN-packaged PA that operates from 10.0 to 11.7 GHz (see Figure 2). It provides saturated output power of 34 dBm (2.5 W) with a third-order intercept point of 43 dBm and 25 dB of small-signal gain. It operates at a quiescent bias condition of 6 VDC at 1300 mA. Additionally, the TGA2524-SM is housed in a 3 x 3-mm QFN package. It operates from 12 to 16 GHz and delivers 26.5 dBm (500 mW) of saturated power with a third-order intercept point of 37 dBm. It provides small-signal gain of 23 dB at a quiescent bias condition of 5 VDC at 320 mA. Finally, the TGA4533-SM is housed in a 4 x 4-mm QFN. It operates from 21.2 to 23.6 GHz and delivers 32 dBm (1.6 W) of saturated power with a third-order intercept of 41 dBm. It offers small-signal gain of 22 dB and operates with a quiescent bias point of 6 VDC at 900 mA, offering superior linear performance for a packaged 1-W PA.

Increasing data rates—and the growing numbers of smartphones, tablets, and, no doubt, other devices still in the concept stage—require wireless carriers to increase backhaul capacity while managing capital and operating expenditures and maintaining customer satisfaction. While optical fiber will play a key role in the solution, microwave PtP radio will be equally important. RF amplifiers and other product innovations will continue to meet the challenges posed by new generations of PtP microwave radios as they evolve to serve this growing market. More information about TriQuint's PtP devices can be found at www.triquint.com.

James Nelson joined TriQuint Semiconductor in 1999 and is currently product marketing manager for point-to-point/microwave radio solutions. He earned his MSEE degree from Texas A&M University.

Mark W. Andrews is strategic marketing communications manager for TriQuint Semiconductor Networks & Defense/Aerospace RF solutions. He also produces technical and corporate industrial video, Internet-based communications, and multi-media markeitng outreach programs for the company.

By Sherry Hess, AWR Corporation

Turn Up the Heat with an Electrical-Thermal MMIC Design Flow

Integrated tools enable high power RF designers to optimize electrical performance and thermal operating properties.

High-power and heat often go hand-in-hand. If you agree with this statement, then how well do you think you know and understand thermal influences on monolithic microwave integrated circuit (MMIC) designs?

Let's take this quiz and find out: (True or False)

1. Substrate vias are often thermally ineffective.
2. A thin epi-layer can have a big effect on junction temperature.
3. A passivation layer can influence junction temperatures.
4. Pro-rata steady-state thermal analysis is not a reliable predictor of duty cycle performance.

> **"Take this quiz and find out: (True or False)"**

If you answered "True" to all of these questions – well-done! (If not, you might find these application notes quite helpful: http://www.capesym.com/thermal_software.html)

Indeed, most high-power power amplifier (PA) designers do know these hidden, best practice techniques; however, the lessons usually come from trial and error as well as being burned (yes, pun intended). In other words, high-power RF components – like PAs – not only produce high-power but also generate significant heat as a byproduct. Thus, long before a MMIC goes into production, it is better to know how the thermal profile will affect the electrical performance of the device.

Up until now, a dedicated MMIC electrical-thermal co-design flow largely did not exist. So, when it came to an electrical-thermal design flow, the MMIC designer had two choices:

Run electrical simulations and ignore thermal altogether (aka "Buyer beware"); or

Run two disparate point tools – one thermal and one electrical – and evaluate results independently (i.e. "Not my problem").

Neither of these options is attractive, as they leave the door open for failure given the cause and effect nature of electrical-thermal interactions when the PA is operational.

For example, with integrated transceiver design, balancing thermal effects of the PA on the receiver LNA electrical performance with a small die size can be a chicken or the egg exercise in the best case scenario and a shot-in-the-dark in the worst case. When an integrated

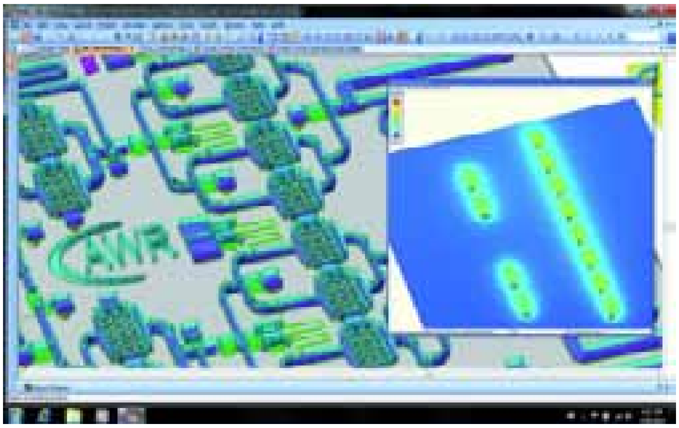


Figure 1: Electrical-thermal co-design analysis for MMICs.

electrical-thermal co-design flow is used, the real world behavior of the MMIC is fully in the control of the designer. The advantages are then two-fold:

Faster design turn-around since the MMIC designer is not dependent upon someone else to run simulations.

Quicker 'what-if' electrical-thermal simulations to determine the optimum design such as the most compact active designs possible for a particular application (bias/power level/efficiency).

Imagine what's possible now when thermal sweeps can be analyzed as a function of PA bias and the loop can be closed between thermal and electrical effects, not as a manual exercise, but by directly exchanging data between simulations. Furthermore, take DC analysis and chip layout into thermal simulations and back again to the electrical domain for subsequent harmonic balance, transient or even system simulations—a whole new world of design possibilities is uncovered.

"What was not thought possible before or simply ignored previously is now a solid reality. "

With AWR Connected™ for SYMMIC (see Figure 1), a viable electrical-thermal co-design solution targeted at MMIC designers exists. This product flow makes it possible to take AWR's Microwave Office™ electrical designs into CapeSym's SYMMIC software package for additional thermal analysis and vice-versa. Together, AWR and CapeSym provide high-power RF designers with the ability to obtain optimal electrical performance with proper consideration given to thermal operating properties as well – resulting in next-generation RF products and systems designed more robustly and reliably.

Oh, and also imagine what else is no longer possible — magic smoke (blue smoke) escaping during test (see Figure 2)! With an electrical-thermal co-simulation design flow, MMIC designers no longer need to

Figure 2: Blue smoke on a macro-scale.

wait until the device is built to find out that transistors often operate at very different temperatures in a MMIC, and as a result can and often do cause electrical performance problems for the circuit.

Catch a demo of AWR Connected for SYMMIC electrical-thermal co-design flow on AWR.TV, or better yet, download an evaluation copy at awrcorp.com and try it for yourself.

Sherry Hess brings to AWR more than 15 years of EDA experience in domestic and international sales, marketing, support, and management. Sherry holds BSEE and MBA degrees from Carnegie Mellon University in Pittsburgh, Pennsylvania.

By Edward Doe, Product Line Director, Network Switch, Broadcom Corporation

Meeting the 3G/4G Challenge

Maintaining Profitability in the Mobile Backhaul Through Ethernet

The impact on bandwidth demand in the mobile backhaul is tremendous. In 2010, mobile traffic was approximately 240,000 Terabytes/month. With the transition to 4G, this figure is expected to increase to 6,300,000 terabytes/month by 2015. To put the problem into perspective, consider that all of the mobile traffic carried in 2010 will be carried within the first two weeks of 2015.

Existing mobile backhaul networks, typically built on legacy Time-Division Multiplexing (TDM) technology are reaching capacity and carriers are scrambling to upgrade to much more efficient Ethernet-based networking to manage the massive new bandwidth requirements.

Ethernet as the standard medium for the backhaul of 3G and 4G services is rapidly taking hold, as evidenced through announcements from operators such as Verizon Wireless. "Ethernet backhaul is something we have been working very hard to get," stated Verizon Wireless CTO and Senior Vice President David Small at the recent FierceWireless Path to 4G conference .

THE OBSOLESCENCE OF TDM

Meeting mobile bandwidth demands is proving difficult for the existing TDM-based infrastructure. As a technology, TDM does not scale well with bandwidth: to double bandwidth, the size of the network must double as well. This means that as traffic volume increases, the cost to transport that traffic rises at a similar rate. At this point, it costs more to build out TDM infrastructure than the network can hope to generate in subscriber revenue.

Ethernet offers a proven means for addressing the performance and economic challenges brought on by the explosive growth of mobile traffic. Ethernet technology provides cost-effective connectivity that scales to rising bandwidth demand (i.e., 10/100/1G/10/100G). Advances in Ethernet technology enable Ethernet-based equipment to provide up to 1000x the bandwidth of a TDM-based connection for a significantly lower cost, allowing manufacturers to drive down equipment costs even as bandwidth throughput increases. With Ethernet technology, Service providers are able to operate networks at a level that yields consistent profit margins and reduce capital expenditure (CAPEX) on mobile backhaul equipment by up to 50 percent.

Because of its high value-proposition and ability to scale, Ethernet is well-suited to lead the transition of the mobile backhaul over from TDM and manage the bandwidth needs of consumers as the transition to 4G progresses. In terms of market share, Infonetics predicts that by 2014 the $8B expected to be spent on new network equipment in this space will be entirely Ethernet-based. Ethernet will also bring substantial annual operating expenditure (OPEX) savings to service providers of up to 75% as compared to T1 leased line costs.

This shift should not be surprising, given Ethernet's consistent history of replacing existing infrastructure as bandwidth needs increase. Ethernet quickly replaced ATM in DSL access concentrators, as well as ATM and other protocols in the aggregation and transport networks. It is now time for the same changes to take place in the mobile backhaul.

Edward Doe serves as Associate Director, Switch Products, for the Infrastructure & Networking Group (ING) at Broadcom Corporation. In this role, Doe is responsible for Service Provider product management in the StrataXGS Product Line.

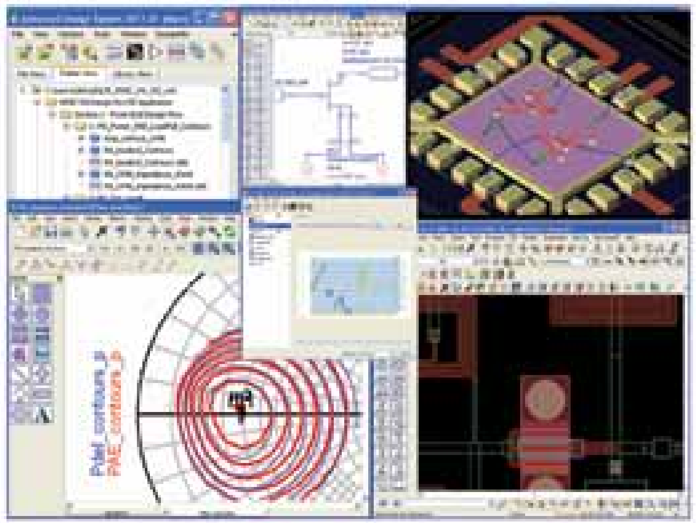
Industry Leading Solutions for engineers engaged in the high-frequency modeling, design and test of RF and microwave System-on-Chips (SoCs)

Featured Products

Agilent Technologies

AWR Corporation

Agilent Advanced Design System



Advanced Design System (ADS) is the leading electronic design automation software for RF, microwave, and high-speed digital applications. It helps uncover and resolve integration issues early in the design process, before fabrication of wireless components.

Multi-Technology Co-Design

Multi-technology design allows multiple IC's combined with laminate and packaging PCB to all be designed together. Tradeoffs can be made interactively on the IC, laminate, packaging and print circuit boards being designed or co-designed. Using ADS 2011, engineers can design individual RF and microwave integrated circuits with different technologies (e.g., GaAs, SiGe, GaN, and Silicon CMOS).

The Industry's Leading Technology, and Much More

ADS puts an unparalleled suite of simulation technology at your fingertips including: S-parameter, AC analysis, harmonic balance, high-frequency SPICE, convolution, circuit envelope, high-speed channel, Agilent Ptolemy system dataflow, Momentum 3D planar EM, and full 3D EM finite element method.

ADS has high quality models for every microwave and RF design application and a variety of design libraries for standards compliant design. Adding to this is X-parameters, which provide breakthrough, nonlinear model extraction from both Agilent instruments and ADS. Agilent also works with top GaAs, GaN, InP, SiGe and Silicon foundries to develop and support process design kits for RFIC and MMIC design.

FEATURES & BENEFITS

- **Multi-Technology Co-Design** — the industry's first and only true multi-technology design environment
- **High Speed Digital** — IBIS-AMI SerDes model simulation and the industry's first Power Integrity solution for heavily perforated power ground planes
- **Integrated Electromagnetic Solvers** — for faster, more accurate simulations; and a new use model that makes it easier to setup and run 3D planar and full 3D electromagnetic simulations
- **New Load Pull Data Controller** — from load pull data to design and simulation in a couple of clicks
- **New Layout Improvements** — layout capacity and performance to handle growing complexity

TECHNICAL SPECS

- Complete schematic capture and layout environment
- Innovative and industry leading circuit and system simulators
- EDA and Design Flow Integration with companies such as Cadence, Mentor, and Zuken
- Largest number of process design kits (PDKs) developed and maintained by leading foundry and industry partners
- Optimization Cockpit for real-time feedback and control when using any of 12 powerful optimizers

AVAILABILITY

March 2011

APPLICATION AREAS

MMIC, signal integrity, RFIC, RF & Microwave Board, RF System in Package and RF module

CONTACT INFORMATION

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Agilent Electromagnetic Professional

Electromagnetic Professional (EMPro) is Agilent EEsof EDA's software simulation design platform for analyzing the 3D electromagnetic (EM) effects of components such as high-speed and RF IC packages, bondwires, antennas, on-chip and off-chip embedded passives and PCB interconnects. EMPro features a modern design, simulation and analysis environment, high capacity simulation technologies and integration with the industry's leading RF and microwave circuit design environment, Advanced Design System (ADS) for fast and efficient RF and microwave circuit design.

Key Benefits of EMPro Simulation Software

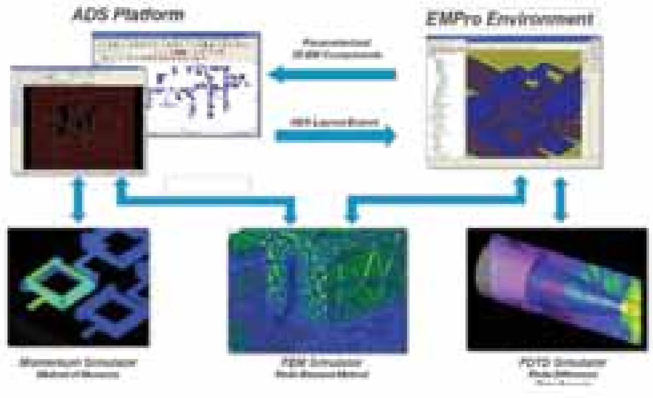
Design Flow Integration: Create 3D components that can be simulated together with 2D circuit layouts and schematics within ADS, using EM-circuit cosimulation.

Broad Simulation Technology: Set up and run analyses using both frequency-domain and time-domain 3D EM simulation technologies: Finite Element Method (FEM) and Finite Difference Time Domain (FDTD).

Efficient User Interface: Quickly create arbitrary 3D structures with a modern, simple GUI that saves time and provides advanced scripting features.

FEATURES & BENEFITS

- Modern, efficient 3D solid modeling environment: EMPro provides the flexibility of drawing arbitrary 3D structures and the convenience of importing existing CAD files.
- Time- and frequency-domain simulation technology: 3D structures can be analyzed in EMPro using the same FEM simulator available in ADS.
- Parameterized 3D EM component generation: Parameterized 3D components created in EMPro and placed on a layout in ADS can be used to simulate the combination of the 2D layout and the 3D EM component.



TECHNICAL SPECS

- Finite Element Method (FEM) simulation engine
- Finite Difference Time Domain (FDTD) simulation engine
- Direct and Iterative solvers for different applications
- Compliance Testing option available for regulatory analyses such as Specific Absorption Rate (SAR)
- Graphical Processor Unit (GPU) Acceleration option available for dramatic speed & capacity improvement

AVAILABILITY

January 2011

APPLICATION AREAS

IC packages, Multilayer RF modules, RF components, Aerospace/Defense, RF shielding, High-speed connectors, Handset antennas, and more.

CONTACT INFORMATION

Agilent Technologies

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Agilent Technolgies, Inc.

GoldenGate RFIC Simulation and Analysis Software

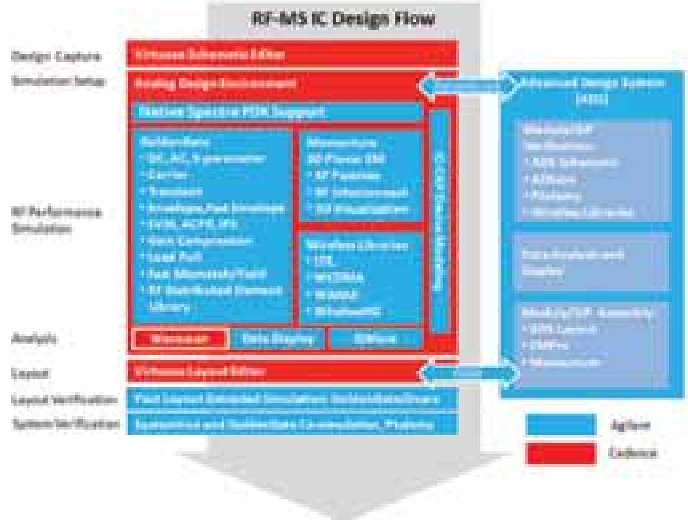
Agilent GoldenGate provides the framework for RF-mixed signal (RF-MS) designers to rapidly simulate circuits, verify specs and validate potential yield of complex highly integrated RFICs. Designers can confidently simulate blocks, combinations of blocks and full receive/transmit chains to understand the influences introduced by noise, distortion, parasitics and numerous other effects confronted in modern RF-MS IC design. Additionally, designers can analyze the manufacturability of circuits using industry standard techniques such as Process and Mismatch Monte Carlo as well as unique Agilent statistical mismatch and process analyses.

These tools provide a comprehensive circuit simulation verification and analysis methodology that has been seamlessly integrated into the Cadence Analog Design Environment. Designers can move smoothly through schematic capture, test bench setup, simulation and analysis to achieve insight into design performance and manufacturability prior to tape out, avoiding costly mistakes and design re-spins.

Agilent's extensive suite of RF-MS simulation, verification and analysis capabilities from system to silicon ease the design challenges. Adding GoldenGate to the design flow reduces costly design iterations, improves productivity, shortens the design cycle, and increases the probability that you can achieve success in the shortest time possible.

FEATURES & BENEFITS

- Best performance, capacity and accuracy to complete your RFIC designs on time with the highest level of designer productivity
- Delivers increased manufacturability using powerful Monte Carlo, Corners and Yield analysis capability
- Uniquely verifies 3G and 4G RF performance using standards-based system level test benches



- **Fast Yield Contributor** — Improve yield by optimizing only what really matters. Determine device, circuit and block yield contributions at any stage of the RFIC design flow.
- **Fast Circuit Envelope Analysis** — Accelerate RF functional path simulations an order of magnitude with broader support for RFIC centric source configurations for models including memory effects.

AVAILABILITY

March 2011

APPLICATION AREAS

RFIC

Modeling and Design

CONTACT INFORMATION

Agilent Technologies

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AWR Corporation

AWR Microwave and RF Design Software Suite

AWR, the innovation leader in high-frequency electronic design automation (EDA), is a provider of software solutions that quicken the pace at which high-tech products like cell phones and satellite systems are developed. When AWR software is part of the design process, engineers can deliver cutting-edge products faster, more reliably, and at a lower cost.

FEATURES & BENEFITS

- **Microwave Office™ software has all the tools essentials for high-frequency IC, PCB and module design:**
  - Linear and non-linear circuit simulators
  - EM analysis
  - Integrated schematic and layout
  - Statistical design
  - Parametric cell libraries
  - Design rule check (DRC)
- **Visual System Simulator™ is software for the design of today's complex communications systems for such standards like:**
  - LTE
  - DVB-H/DVB-T
  - WiMAX/802.16d-2001/802.16e-2005 (mobile and fixed)
  - CDMA2000
  - GSM/EDGE
  - WLAN/802.11a/b/g
  - 3G WCDMA FDD
  - IS95
- **AXIEM® is electromagnetic (EM) software developed for 3D planar applications like RF PCBs and modules, LTCC, MMIC, and RFIC designs. Capabilities include:**
  - Microwave Office seamless integration
  - Proprietary full-wave planar EM solver technology
  - Advanced hybrid meshing technology
  - Numerous source/excitations
  - Parametric studies, optimization, and tuning
  - 3D visualization and animation
  - Antenna analysis and post-processing
- **Analog Office® software targets analog and radio-frequency integrated circuit (RFIC) designs. It provides RFIC designers with the essential tools and technology to take designs from system-level to final tape-out:**
  - Design capture
  - Synthesis
  - Simulation
  - Optimization
  - Layout
  - Extraction
  - Verification

AVAILABILITY

AWR software is available today via a free 30-day trial. Visit www.awrcorp.com to get started.

APPLICATION AREAS

MMIC, RFIC, RF PCB, HF Modules, et al

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