8F-1, No.186, Jian-yi Road, ChungHo City, Taipei County, Taiwan Zip 235
TEL: (886)-2-8227-1799 FAX: (886)-2-8227-1798
E-mail: Sales@ChipSiP.com
http://www.ChipSiP.com

APPROVAL

CUSTOMER:

PART NUMBER: CT47568126A-G4

DESCRIPTION: Combo Memory (Green MCP)
NAND Flash 256Mb (x8) + DDR2 SDRAM 512Mb (x16)
Outline:13.0x10.0x1.4mm, Pitch:0.8mm, FBGA 110Balls

CUSTOMER'S P/N:

CHECKED BY:

APPROVED BY:

DATE:

Approved Signatures	鉅景科技 股份有限公司
	Contact Person:

1. INTRODUCTION

CT47568126A-G4 is a Multi Chip Package Memory (MCP) that integrated 256M bits NAND Flash and 512M bits DDR SDRAM by advanced SiP (System-in-a-Package) technology. CT47568126A-G4 offers space saving advantage that could miniaturize your portable device. And it is conformed with RoHS regulations.

1.1 APPLICATION

- DSC
- DV
- PMP

1.2 FEATURE

PRODUCT LIST

- CT47568126A-G4
  - NAND FLASH: 256M bits (32Mx8bit)
  - DDR SDRAM: 512M bits (32Mx16bit)

POWER SUPPLY

- NAND FLASH
  - 3.3V
- DDR SDRAM
  - 2.5V

PACKAGE

- Solder Ball Material: 96.5%Sn / 3%Ag / 0.5% Cu
- FBGA 13.0 x 10.0 x 1.4mm, 110 Balls
- Ball Pitch: 0.8 mm

Temperature

- Operating: 0 to +70 °C
- Storage: -55 to +150 °C

NAND FLASH Features

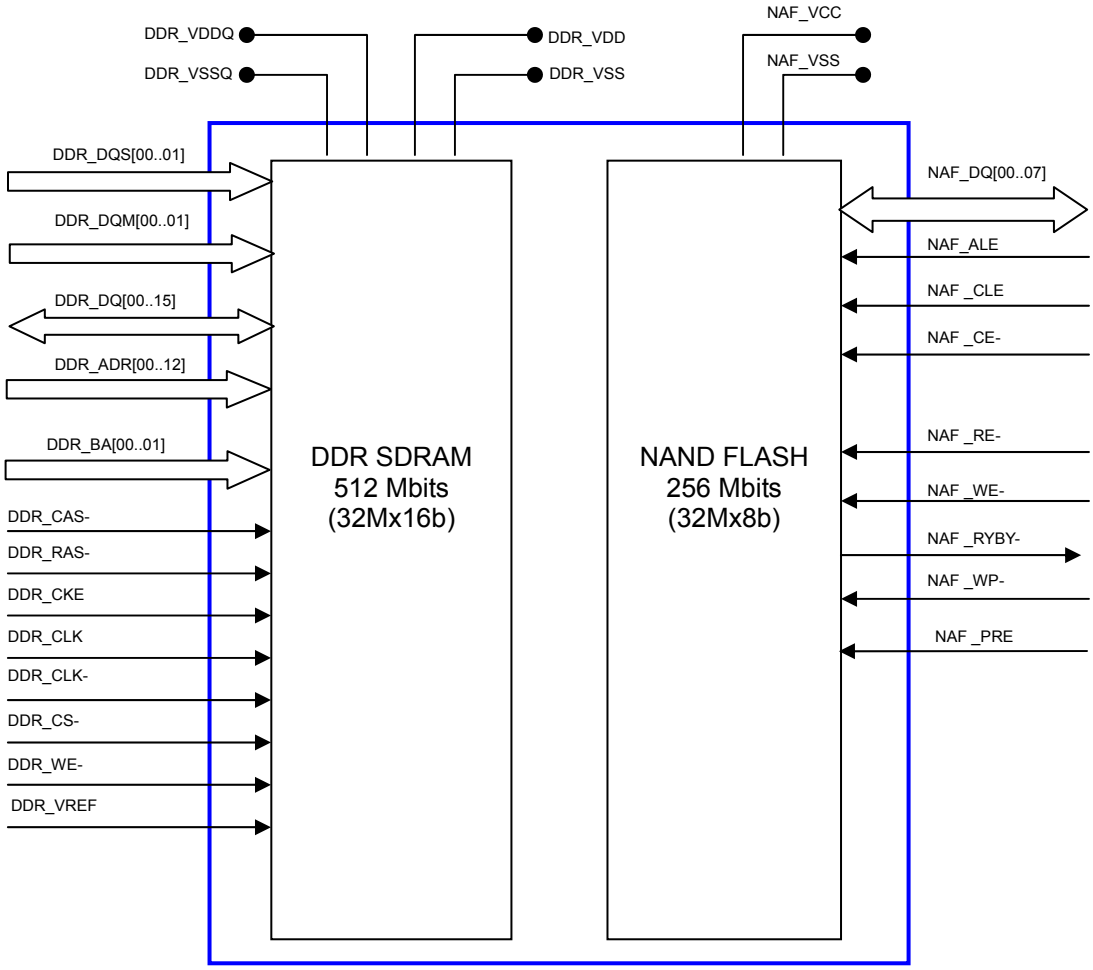
- Organization
  - Memory Cell Array
    X8: (32M + 1024K) bit x 8 bit
  - Data Register
    X8: (512 + 16) bit x 8 bit
- Auto Program and Erase
  - Page Program
    X8: (512 + 16) Byte
  - Block Erase
    X8: (16K + 512) Byte
- Automatic Page0 Read at Power-UP Option
  - Boot from NAND support
  - Automatic Memory Download
- Support Sequential Row Read
- Page Read Operation
  - Page Size
    X8: (512 + 16 spare) Byte
  - Random Access: 12μs (Max.)
  - Sequential Access: 50 ns (Min.)
  - Page Program Time: 200μs(typ)
- Fast Write Cycle Time
  - Program Time: 200μs (Typical)
  - Block Erase Time: 2 ms (Typical)
- Command /Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Command Register Operation
- Intelligent Copy-Back
- Reliability Performance
  - Endurance cycles: 100K Program/Erase Cycle(Typical)
  - Data retention: 10 years

DDR SDRAM Features

- High speed data transfer rates with system frequency up to 200MHz
- Data Mask for Write Control
- Four Banks controlled by DDR_BA00 & DDR_BA01
- Programmable DDR_CAS- Latency: 2, 2.5, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  2, 4, 8 for Sequential Type
  2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8096 cycles/64 ms
- Available in 110 Ball FBGA
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DDR_DQS[00..01]) for input and output data, active on both edges
- On-Chip DLL aligns DDR_DQ[00..15] and DDR_DQS[00..01] transitions with DDR_CLK transitions
- Differential clock inputs DDR_CLK and DDR_CLK-
- Power Supply 2.5V ± 0.2V
- Power Supply 2.6V ± 0.1V for DDR400
- t_{RAS} lockout supported
- Concurrent auto precharge option is supported

2. FUNCTION DIAGRAM

2.1 CT47568126A-G4



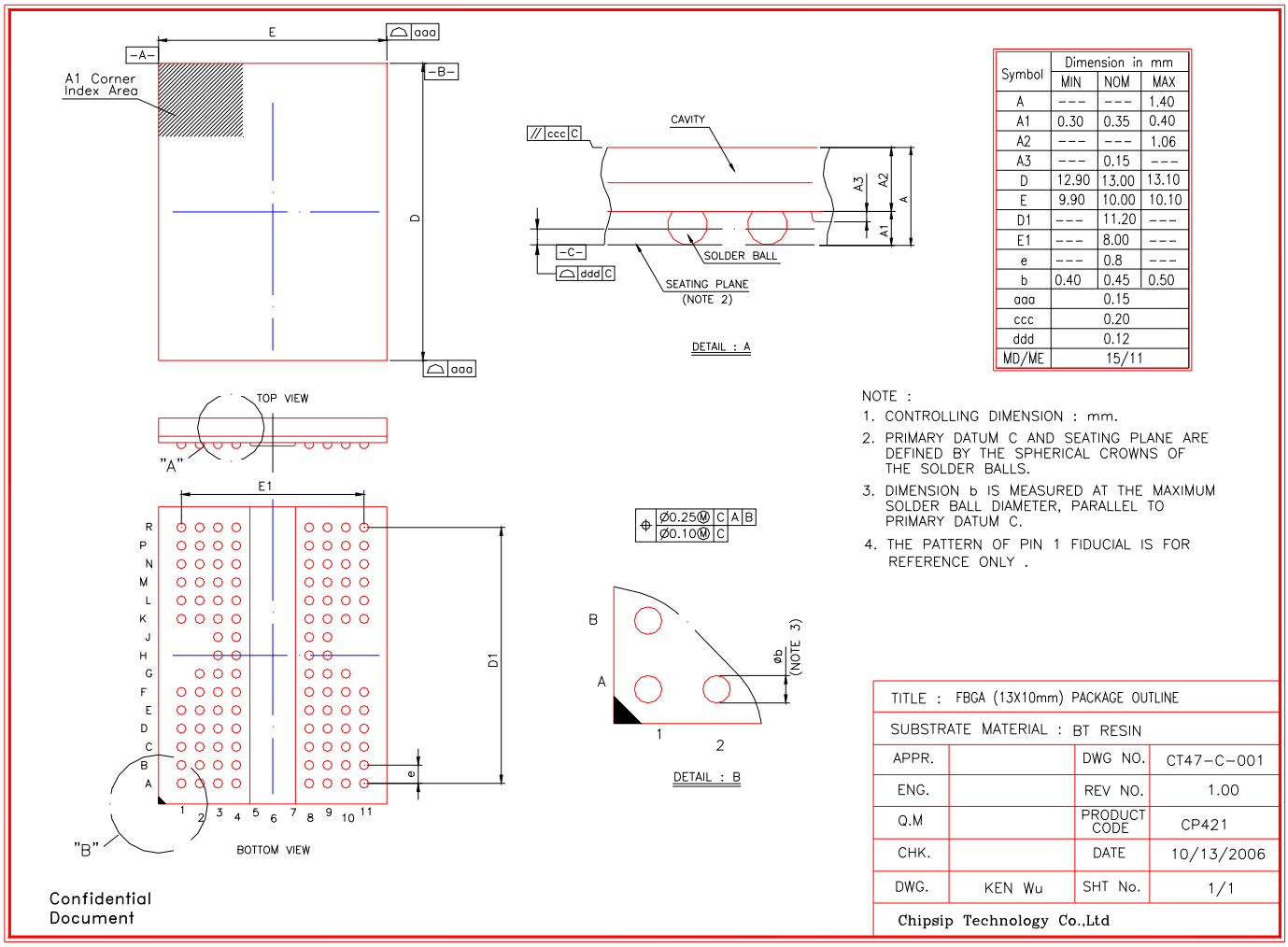
3. PIN CONFIGURATION

3.1 CT47568126A-G4 PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	DDR_DQ15	DDR_VSS				DDR_VDD	DDR_DQ00	NC	NC
B	NC	NC	DDR_DQ14	DDR_VSSQ				DDR_VDDQ	DDR_DQ01	NC	NC
C	NC	NAF_WP-	DDR_VDDQ	DDR_DQ13				DDR_DQ02	DDR_VSSQ	NC	NC
D	NAF_WE-	NAF_ALE	DDR_DQ11	DDR_DQ12				DDR_DQ03	DDR_DQ04	NAF_RE-	NAF_RYBY-
E	NAF_CLE	NC	DDR_DQ10	DDR_VSSQ				DDR_VDDQ	DDR_DQ05	NC	NAF_CE-
F	NC	NAF_VSS	DDR_VDDQ	DDR_DQ09				DDR_DQ06	DDR_VSSQ	NAF_VCC	NC
G		NC	DDR_VSSQ	DDR_DQ08				DDR_DQ07	DDR_VDDQ	NC	
H			DDR_VREF	DDR_DQS01				DDR_DQS00	DDR_VDD		
J			DDR_DQM01	DDR_VSS				NC	DDR_DQM00		
K	NC	NAF_VSS	DDR_CLK	DDR_CLK-				DDR_WE-	DDR_CAS-	NAF_VCC	NAF_PRE
L	NC	NC	DDR_ADR12	DDR_CKE				DDR_RAS-	DDR_CS-	NC	NAF_DQ04
M	NC	NAF_DQ03	DDR_ADR09	DDR_ADR11				DDR_BA00	DDR_BA01	NC	NAF_DQ05
N	NC	NAF_DQ02	DDR_ADR07	DDR_ADR08				DDR_ADR10	DDR_ADR00	NC	NAF_DQ06
P	NC	NAF_DQ01	DDR_ADR05	DDR_ADR06				DDR_ADR01	DDR_ADR02	NC	NAF_DQ07
R	NC	NAF_DQ00	DDR_VSS	DDR_ADR04				DDR_ADR03	DDR_VDD	NC	NC

TOP VIEW

6. PACKAGE DIMENSION (110 Ball FBGA, 10x13x1.4mm)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	---	---	1.40
A1	0.30	0.35	0.40
A2	---	---	1.06
A3	---	0.15	---
D	12.90	13.00	13.10
E	9.90	10.00	10.10
D1	---	11.20	---
E1	---	8.00	---
e	---	0.8	---
b	0.40	0.45	0.50
aaa	0.15		
ccc	0.20		
ddd	0.12		
MD/ME	15/11		

NOTE :
1. CONTROLLING DIMENSION : mm.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

Confidential Document

TITLE : FBGA (13X10mm) PACKAGE OUTLINE			
SUBSTRATE MATERIAL : BT RESIN			
APPR.		DWG NO.	CT47-C-001
ENG.		REV NO.	1.00
Q.M		PRODUCT CODE	CP421
CHK.		DATE	10/13/2006
DWG.	KEN Wu	SHT No.	1/1
Chipsip Technology Co.,Ltd			