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APPROVAL

CUSTOMER:

PART NUMBER: CT48248NS246F1

DESCRIPTION: Combo Memory (Green MCP)
NAND Flash 1Gb (x8) + DDR2 SDRAM 1Gb (x16)
Outline:15.0x15.0x0.9mm, Pitch:0.65mm, VFBGA 112Balls

CUSTOMER'S P/N:

CHECKED BY:

APPROVED BY:

DATE:

Approved Signatures	鉅景科技 股份有限公司
	Contact Person:

1. INTRODUCTION

CT48248NS246F1 is a Multi Chip Package Memory (MCP) that integrated 1G bits NAND Flash and 1G bits DDR2 SDRAM by advanced SiP (System-in-a-Package) technology. CT48248NS246F1 offers space saving advantage that could miniaturize your portable device. And it is conformed with Green regulations.

1.1 APPLICATION

- DSC
- DV
- PMP

1.2 FEATURE

PRODUCT LIST

- CT48248NS246F1
  - NAND FLASH: 1G bits (128Mx 8-bit)
  - DDR2 SDRAM: 1G bits (8M x 8-Bank x 16-bit)

POWER SUPPLY

- NAND FLASH
  - 3.3V
- DDR2 SDRAM
  - 1.8V

PACKAGE

- Solder Ball Material: 98.5%Sn / 1%Ag / 0.5%Cu
- VFBGA 15.0 x 15.0 x 0.9 mm, 112 Balls
- Ball Pitch: 0.65 mm
- Weight: 0.3g

Temperature

- Operating: -10 to +85 °C
- Storage: -55 to +125 °C

NAND FLASH

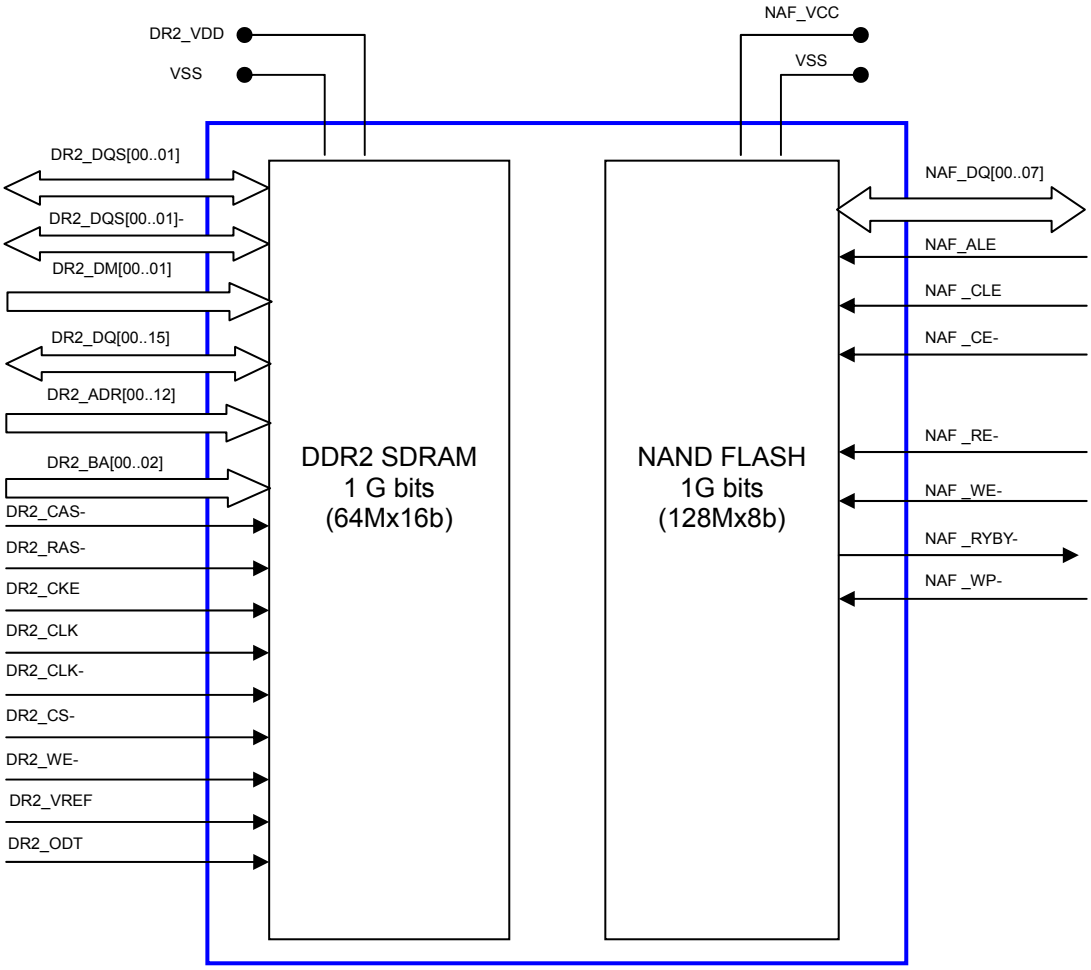
- Voltage Supply
  - 3.3V Device: 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (128M + 4M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read : 25μs(Max.)
  - Serial Access :30ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 200μs(Typ.)
  - Block Erase Time : 2.0ms(Typ.)
- Command/Address/Data Multiplexed NAF_DQ[00..07] Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles(with 1bit/528Byte ECC)
  - Data Retention : 10 years
- Command Driven Operation

DDR2 SDRAM

- Power Supply: DR2_VDD, DR2_VDDQ = 1.8 V± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- DR2_CAS- Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DR2_DQS[00..01] and DR2_DQS[00..01]-) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DR2_DQ[00..15] and DR2_DQS[00..01] transitions with clock
- Differential clock inputs (DR2_CLK and DR2_CLK-)
- Data masks (DR2_DM[00..01]) for write data
- Commands entered on each positive DR2_CLK edge, data and data mask are referenced to both edges of DR2_DQS[00..01]
- Posted DR2_CAS- programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus DR2_CAS-Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (DR2_ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18

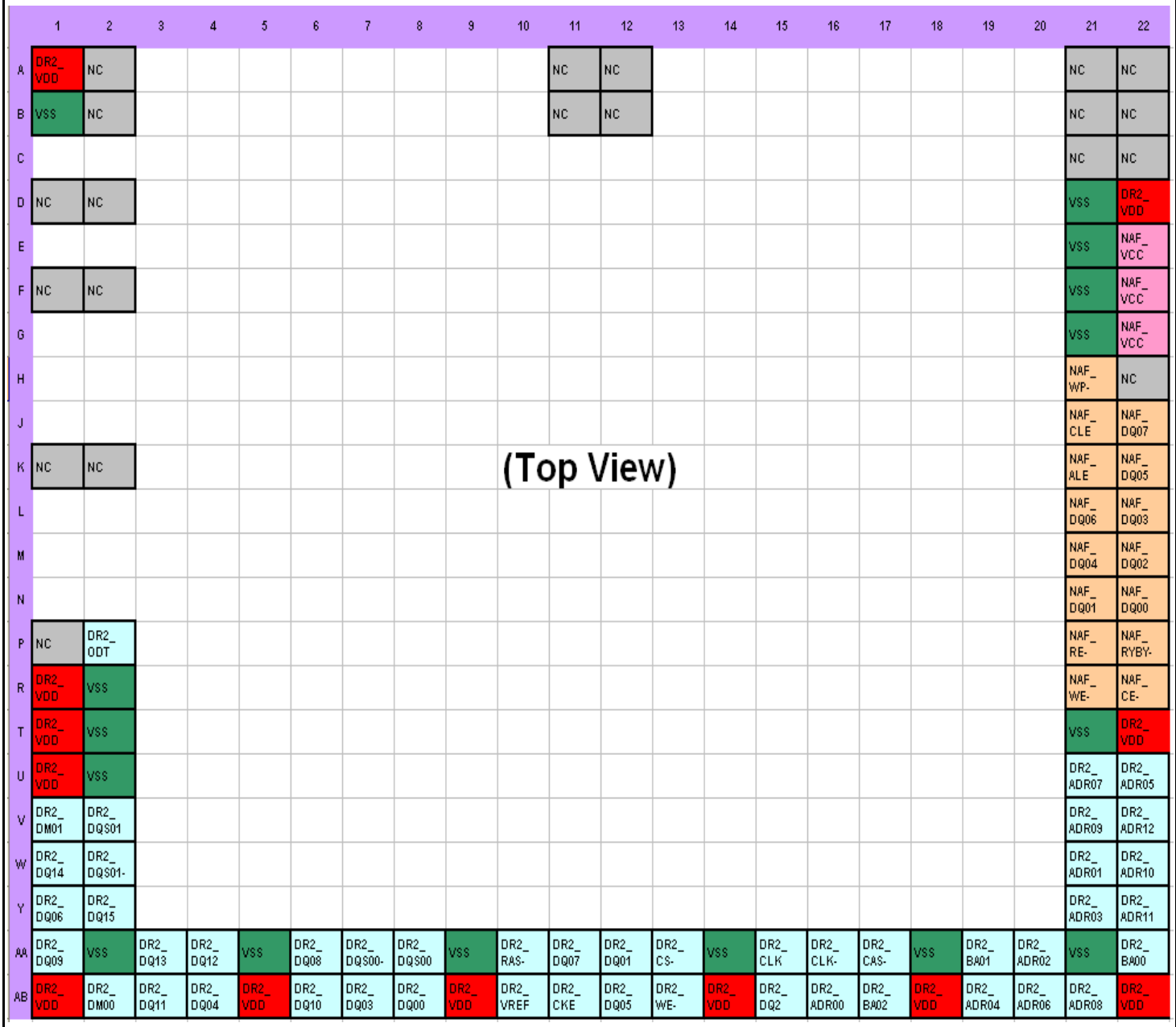
2. FUNCTION DIAGRAM

2.1 MCP



3. PIN CONFIGURATION

3.1 CT48248NS246F1 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	DR2_VDD	NC									NC	NC									NC	NC
B	VSS	NC									NC	NC									NC	NC
C																					NC	NC
D	NC	NC																			VSS	DR2_VDD
E																					VSS	NAF_VCC
F	NC	NC																			VSS	NAF_VCC
G																					VSS	NAF_VCC
H																					NAF_WP-	NC
J																					NAF_CLE	NAF_DQ07
K	NC	NC																			NAF_ALE	NAF_DQ05
L																					NAF_DQ06	NAF_DQ03
M																					NAF_DQ04	NAF_DQ02
N																					NAF_DQ01	NAF_DQ00
P	NC	DR2_ODT																			NAF_RE-	NAF_RYBY-
R	DR2_VDD	VSS																			NAF_WE-	NAF_CE-
T	DR2_VDD	VSS																			VSS	DR2_VDD
U	DR2_VDD	VSS																			DR2_ADR07	DR2_ADR05
V	DR2_DM01	DR2_DQS01																			DR2_ADR09	DR2_ADR12
W	DR2_DQ14	DR2_DQS01-																			DR2_ADR01	DR2_ADR10
Y	DR2_DQ06	DR2_DQ15																			DR2_ADR03	DR2_ADR11
AA	DR2_DQ09	VSS	DR2_DQ13	DR2_DQ12	VSS	DR2_DQ08	DR2_DQS00-	DR2_DQS00	VSS	DR2_RAS-	DR2_DQ07	DR2_DQ01	DR2_CS-	VSS	DR2_CLK	DR2_CLK-	DR2_CAS-	VSS	DR2_BA01	DR2_ADR02	VSS	DR2_BA00
AB	DR2_VDD	DR2_DM00	DR2_DQ11	DR2_DQ04	DR2_VDD	DR2_DQ10	DR2_DQ03	DR2_DQ00	DR2_VDD	DR2_VREF	DR2_CKE	DR2_DQ05	DR2_WE-	DR2_VDD	DR2_DQ2	DR2_ADR00	DR2_BA02	DR2_VDD	DR2_ADR04	DR2_ADR06	DR2_ADR08	DR2_VDD

6. PACKAGE DIMENSION (112 Ball VFBGA, 15x15x0.9mm)

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOR.	MAX.
TOTAL THICKNESS A	---	---	0.9
STAND OFF A1	0.16	---	0.26
SUBSTRATE THICKNESS A2		0.21	REF
MOLD THICKNESS A3		0.37	REF
BODY SIZE D		15	BSC
BODY SIZE E		15	BSC
BALL DIAMETER		0.3	
BALL OPENING		0.275	
BALL WIDTH b	0.27	---	0.37
BALL PITCH e		0.65	BSC
BALL COUNT n		112	
EDGE BALL CENTER TO CENTER D1		13.65	BSC
EDGE BALL CENTER TO CENTER E1		13.65	BSC
BODY CENTER TO CONTACT BALL SD		0.325	BSC
BODY CENTER TO CONTACT BALL SE		0.325	BSC
PACKAGE EDGE TOLERANCE aaa		0.1	
MOLD FLATNESS bbb		0.1	
COPLANARITY ddd		0.08	
BALL OFFSET (PACKAGE) eee		0.15	
BALL OFFSET (BALL) fff		0.08	

NOTES:
1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.