IR SILICON POWER CHIPS
APPLICATION NOTE

INTRODUCTION

This application note describes the prepassivated high power thyristor and diodes available from International Rectifier in die form.
The nomenclature guide, provided at the end of each die bulletin, allows to identify the part number for the requested device.
International Rectifier employs two different passivation processes to manufacture his diffused high power devices, diodes and thyristors:
. the organic passivation (silicone rubber);
. the glass passivation.
The organic passivation allows to test till the breakdown the chips at room and at high temperature, it offers very high working temperature capability.
Great care must be taken to avoid that, during working conditions, the chip temperature does not exceed the max junction temperature limit because materials progressively decrease their passivant properties.
Organic passivation is applied on high power round die.
The glass passivation provides a great stability of blocking voltage characteristic and a level of hermeticity with relatively high mechanical strength; it is chosen for a wide range of medium power thyristors, rectifiers and fast recovery diodes (square and rectangular).
Using the above process it is possible to have high voltage and highly reliable devices at a very competitive price (see also reliability section).

Characteristics

Features and sizes of thyristors and diodes presently available from International Rectifier in die form are described in the specification and characteristics table.
Because of electrical probe limitations some characteristics, like power dissipation, surge capability and thermal resistance, largely dependent from users' assembly technique, cannot be tested in chip form nor guaranteed.
When high current tests are performed the Kelvin probes have to be applied.

Packing and Shipping

High Power semiconductor chips from International Rectifier are shipped in plastic containers (waffle packs and blister) to protect them during shipment.
Standard orientation for glass passivated die:

SCR : cathode side up,
Diodes: anode side up.

Standard orientation for rubber passivated die:

SCR : cathode side up,
Diodes: cathode side up.

For opposite orientation contact factory.
Wafers are shipped in plastic slotted boxes (25 wf max each box).
Either waffle packs and boxes are vacuum sealed in plastic bags to prevent metallization oxidation;
They are labelled with indication of part number, quantity, lot number, and rated voltage.
Each lot of chips shall come from a single homogeneus lot of wafers, in multiples of waffle packs or boxes.
When this is not possible, a maximun of two homogeneous lots shall be used with a minimum of 200 pcs from the smaller lot.

Handling and Storage

Once bags are opened, and prior to assembly, the chips must be stored in a clean, dry, inert atmosphere such as nitrogen.
They should be handled with teflon -

tipped vacuum pencils to prevent mechanical damage of the organic passivation that can compromise the reverse blocking reliability.
In particularly metal tweezers can induce scratches and bare fingers transfer grease and oil compromising the bonding and soldering quality.

Metallization
Refer to Nomenclature Guide for available metal options.
Different metallization surfaces are available to meet specific assembly requests:
In the cathode side we have:
. Multi-layer metallization Al-Ni-Au or Cr-Ni_Ag, used as the most external metals for solder preform mounting.
. Thick Al-metal for ultrasonic wire bonding or compression bonding.
In the anode side we have:
. Multi-layer metallization Cr-Ni_Ag, used as the most external metals for solder preform mounting.
. Nichel plated moly disk or simply rough moly disc for round die from 14 mm to 52 mm diameter.
(In the interest of product improvement, International Rectifier reserves to make design or processing changes without notification).

Glass Passivated Wafer Sawing
When entire wafers are supplied, the reject die after probing and visual inspection are inked to be recognised and scraped.
Position for black ink dots are indicated in each part number bulletin.
Glass passivated slices are designed to be compatible with standard wafer sawing technique used in semiconductor industries.
Several types of adhesive tapes can be used to mount the wafer before cutting.
MOAT rectifiers are separated sawing through silicon and we suggest to use resinoid blades with 35 μm thickness.
Table speed can be adjusted up to 75 mm/sec. and spindle rotation can be 45000 rpm.
SCR and Mesa rectifiers are separated sawing through three different layers: in order glass-silicon-glass.
We suggest to use diamond blades with 100 μm thickness and recommend to limit table speed to a maximum of 15 mm/sec; spindle rotation can be 30000 rpm.
We suggest not to use scribe and break technique to separate SCR and Mesa diode wafers.

Chips assembling
a) Round Die
a1) Compressed
High power dice are suitable to be assembled in ceramic puk, stud compressed packages and in high power compressed modules.
Depending on the dice size a rated mounting force can be applied.
a2) Stud brazed
High power gold plated chips on cathode side and nichel moly on the anode side, are suitable to be soldered in reverse and direct way on brazed stud.

The chips should not be cleaned before assembly.

b) Square and Rectangular Die
b1) Soldering on Silver metallized surfaces
The glass passivated Square and Rectangular chips silver plated are suitable for solder preform mounting on hybrid circuits.
Substrate: any of the commonly used header or substrate material such as copper, nickel-plated copper, gold-nickel-silver plated molybdenum, metallized beryllia, alumina DBC, aluminum nitride, IMS are acceptable.
A wide range of Pb-Sn, Pb-In or Pb-Sn-Ag soft solder preforms are suitable for mounting.
J-alloy (Sn-Sb-Ag) coupled with die scrubbing can also be used with excellent performances in terms of reduced solder voids.
The chips are also suitable for mounting

with solder cream and no acid flux.
Any subsequent cleaning procedure is allowed only with solvents or chemicals not deteriorating the glass passivation.
Conductive epoxy can also be used but this technique gives poor thermal resistance capability and therefore it has to be considered only for special applications with low dissipation requirements.
Soldering temperature profile and peak temperature can be defined by the user; we suggest not to exceed 400 °C (750 F), and to have H_2 or forming gas in the conveyor belt furnace. A typical soldering profile is shown in fig. # 1.

b2) Bonding Al metallized surfaces
In case of aluminium metallization, ultrasonic wire bonding can be used with wire diameter up to 20 mils.
High purity wires (five 9's) are recommended.
During ultrasonic bonding a rigid clamping of the substrate, on which the die is mounted, is necessary and great care must be taken to avoid cracking of the chip surface, caused by the machine.
Excellent performances at thermal fatigue can be reached using multi-wire connections coupled with stitch bonds of the wires (see also reliability section).

Coating and Encapsulation
Prior to encapsulation, if solder paste has been used, the chip/assembly must be cleaned or must be kept in a moisture free environment, as leakage is particularly sensitive to surface moisture.
No cleaning is recommended if solder preform has been used in H2 or other forming gas atmosphere.
After soldering – bonding steps we suggest to coat the die with a potting rubber or a silica gel.
High electronic grade compound and elasticity of the coating are recommended to reduce the possibility of contaminate and stress the die.
A great care must be taken in case of packaging processes involving direct contact of hard moulding material onto the silicon die.
If the final package is plastic, be certain to chose material compatible with the chip passivation and the coating compound.

CHIP CERTIFICATION
Quality
All power chips are required to meet the same standards as those assembled in our discrete devices and/or power modules.
The purpose of the procedure for the quality assurance and certification at International Rectifier Corporation Italy is to define the test procedures, the methods and systems of data acquisition. These are applicable during the chip manufacturing process in order to meet continuously the user's quality expectations.
The limiting characteristics of these chips, electrical and mechanical, are described in the specification tables. The testing flow and the Quality Master Plan are strictly integrated with manufacturing.
The records are regularly and properly filed on the production floor so to be easily traceble and available on request.
V_{RRM}/V_{DRM}, Ir, @ 25°C,@ Tj max and switching parameter are 100% tested .
Other static and dynamic parameters (t_q, t_{rr}, Qrr, **V**tm) are sampled and a statistical Process Control (SPC) system has been introduced as a powerful tool of investigation and data analysis in order to verify the level of conformity of the diffusion batches for both bare chips

Reliability
Information and data coming from IR's tests on complete devices are available and can help customer needs.
Extensive tests are performed either for the qualification of new products and as regular on-going monitoring of devices in production.
HTRB, Temperatyre Cycling, HTS, Power Cycling, Moisture Resistance are examples of stress tests in place.
As a reference, we show here below some

results of the high power thyristors.

Fig.2: HTRB

The purpose of HTRB is to stress the device with applied bias in the blocking mode while at elevated junction temperature.

This will accelerate any blocking voltage degradation process.

The primary failure mode for HTRB stress If the degradation occurs at the header/die interface, then the thermal impedance will begin to increase well before any electrical effect is seen.

The mechanical stresses from the application of power can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of shorted gates or degraded breakdown characteristics.

The following graphs show the V_T evolution during the test performed on SCR assembled on Hockey Puk (series ST230/1200V).

Our devices can survive after several thousand cycles even when stress tests force very high ΔTj.

First catastrophic failure (V_T open-circuit or V_{DR}/V_{RR} downgraded) arise well above the limit reached by most of competitors.

Claims

Claims can be accepted only for unused chips (not 100% tested at incoming inspection or packaged) and must be accompained by a detailed inspection report with fault indications and any conditions (material and process) if used.

Chips must be returned using the same IR packaging. Only claims for die shipped within twelve months will be accepted.

is a gradual degradation of the breakdown characteristics. It is related to the presence of foreign materials and polar ionic contaminants. These materials, migrating under application of electric field at high temperature, can perturb the electric field termination structure.

The following graphs show the typical trends of the sensitive parameters $I_{DRM}$and I_{RRM} of the devices on HTRB tests at Tj=125 °C @ V_{DR} /V_{RR} = 1200 Vpk .The parts are well stable during the 1000 test hours and stay very well below bulletin limits.

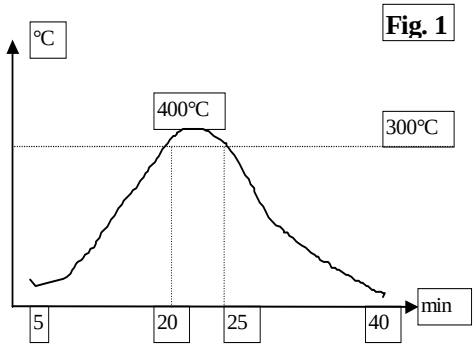
Such data are indicative but no warranty is offered due to the wide range of package conditions and operating applications.

Fig.2: Power Cycling

The purpose of power cycling is to simulate the thermal and current pulsing stresses which devices will encounter in actual circuit applications when either the equipment is turned on and off or the power is applied to the device in short bursts interspersed with quiescent, low power periods. The simulation is achieved by the on/off application of power to each module and forcing the device cooling during the off period.

The primary failure mode for power cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue, due to the thermo-mechanical stresses from the heating and cooling, will cause electrical
or thermal performance to degrade.

Fig. 1



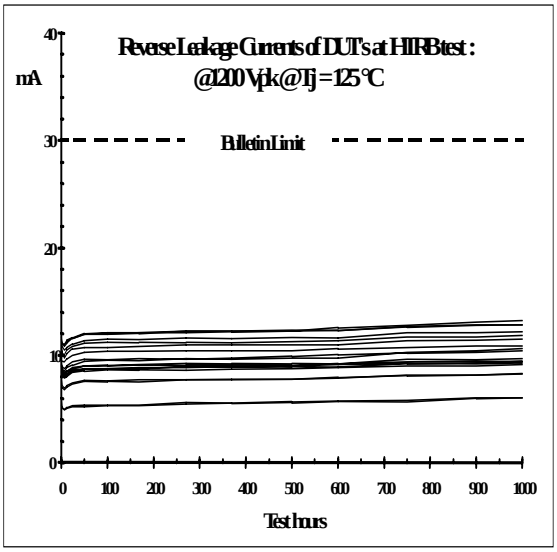


Fig 2a Reverse Leakage Currents during HTRB test period on SI23012, lot WRE1, sample size 9

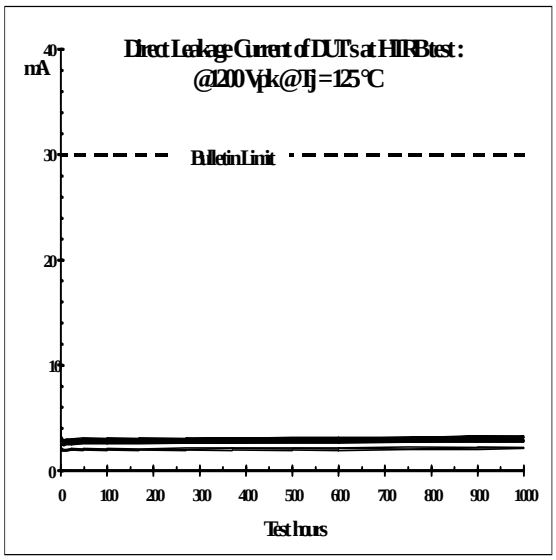


Fig 2b Direct Leakage Currents during HTRB test period on IRKT1912, lot WRE1, sample size 9