PIC16F/LF1938/1939 Silicon Errata and Data Sheet Clarification

The PIC16F/LF1938/1939 family devices that you have received conform functionally to the current Device Data Sheet (DS41364**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16F/LF1938/1939 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16F/LF1938/ 1939 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
PIC16F1938	`10 0011 101x xxxx`	1
PIC16F1939	`10 0011 110x xxxx`	1
PIC16LF1938	`10 0100 101x xxxx`	1
PIC16LF1939	`10 0100 110x xxxx`	1

Note 1: The Device ID is located in the last configuration memory space.

2: Refer to the *"PIC16F193X/LF193X and PIC16F194X/LF194X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
ADC	Analog-to-Digital Converter	1.1	ADC Conversion does not Complete.	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	2.1	PWM 0% Duty Cycle Direction Change.	X
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	2.2	PWM 0% Duty Cycle Port Steering.	X
Timer1	Timer0 Gate Source	3.1	Toggle Mode Works Improperly.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: ADC

1.1 Analog-to-Digital Converter (ADC)

Under certain device operating conditions, the ADC conversion may not complete properly. When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/$\overline{\text{DONE}}$ bit does not get cleared and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

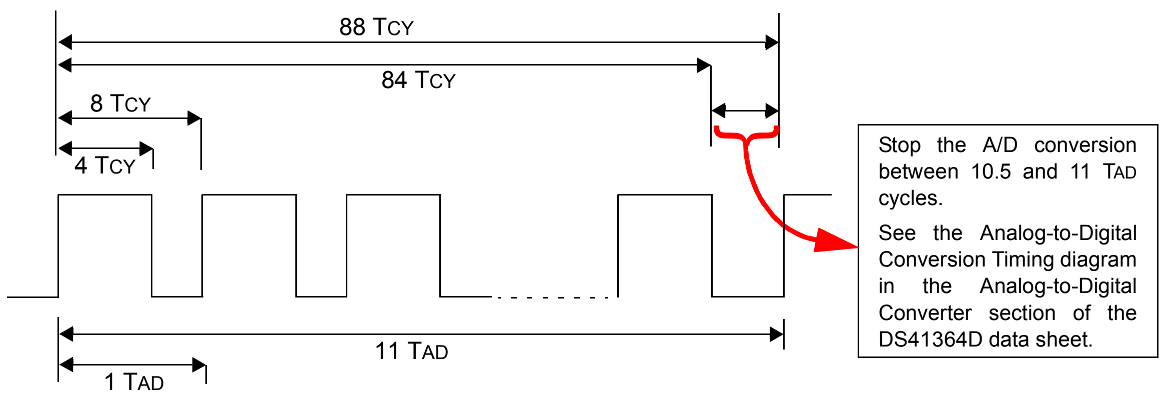
Work around

Method 1: Select the dedicated RC oscillator as the ADC conversion clock source, and perform all conversions with the device in Sleep.

Method 2: Provide a fixed delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/$\overline{\text{DONE}}$ bit in software. The GO/$\overline{\text{DONE}}$ bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the DS41364D data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note:	The exact delay time will depend on the choice of FOSC and the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS FOR OTHER FOSC AND TAD COMBINATIONS

FOSC	TAD	Instruction Cycle Delay Counts
32 MHz	FOSC/64	172
	FOSC/32	86
16 MHz	FOSC/64	172
	FOSC/32	86
	FOSC/16	43
8 MHz	FOSC/32	86
	FOSC/16	43

Affected Silicon Revisions

A1							
X							

2. Module: Enhanced Capture Compare PWM (ECCP)

2.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A1							
X							

2.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A1							
X							

3. Module: Timer1

3.1 Timer1 Gate Toggle Mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41364**D**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

In Table 29-2, Oscillator Parameters, the HFINTOSC and MFINTOSC internal calibrated oscillator frequency tolerances should be +/- 3.0% when V_{DD} is equal to, and above 2.5V and when temperatures are equal to, and above 60°C, yet still equal to, or below 85°C, as shown below.

TABLE 29-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ T_A ≤ +125°C

Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
OS08	HF_{OSC}	Internal Calibrated HFINTOSC Frequency(2)	±2%	—	16.0	—	MHz	0°C ≤ T_A ≤ **+60°C**, V_{DD} ≥ 2.5V
			±3.0%	—	**16.0**	—	**MHz**	**60°C ≤ T_A ≤ 85°C, V_{DD} ≥ 2.5V**
			±5%	—	16.0	—	MHz	-40°C ≤ T_A ≤ +125°C
OS08A	MF_{OSC}	Internal Calibrated MFINTOSC Frequency(2)	±2%	—	500	—	kHz	0°C ≤ T_A ≤ **+60°C**, V_{DD} ≥ 2.5V
			±3.0%	—	**500**	—	**kHz**	**60°C ≤ T_A ≤ 85°C, V_{DD} ≥ 2.5V**
			±5%	—	500	—	kHz	-40°C ≤ T_A ≤ +125°C
OS10*	$T_{IOSC\ ST}$	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	μs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	20	30	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

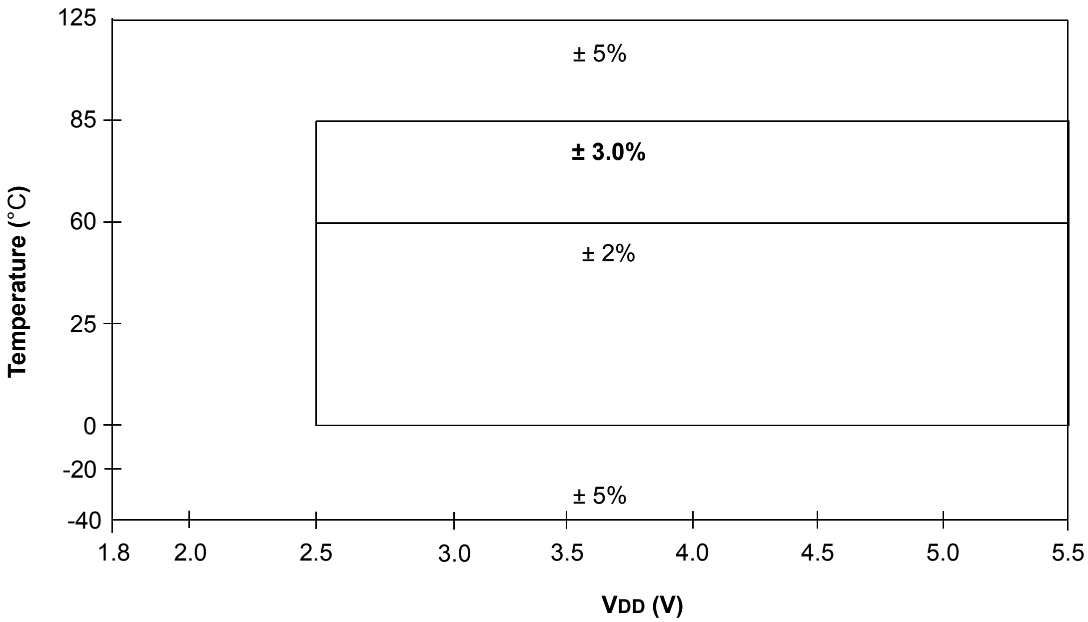
2: To ensure these oscillator frequency tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

3: By design.

2. Module: Electrical Specifications

In Figure 29-3, HFINTOSC Frequency Accuracy Over Device VDD and Temperature, the oscillator accuracy should be +/- 3.0% when VDD is equal to and above 2.5V and when temperatures are equal to and above 60°C, yet still equal to or below 85°C, as shown below.

FIGURE 29-3: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (05/2010)

Initial release of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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