

Low Power with Fast Wake-Up and Single Power Supply for Voice-Input Remote Controls

Product Overview

The CX20823 mono ADC is a single-channel ADC that optimizes system cost and performance for near field voice input applications. The low-power device includes an audio ADC and integrated power management that allows the device to operate from a battery power supply directly. A very low-power disable state of <1 μ A extends battery life, and a fast wake-up time of <50ms ensures capture of all voice commands. The low cost and optimized performance make the CX20823 ideal for voice-input remote controls for SmartTVs, STBs, and Smart appliances.

To reduce system cost, the CX20823 has integrated power management capability that allows the device to operate from a single power supply input that can be floating from 1.71V to 3.6V. Hence, the device can operate directly from 2AA batteries. The CX20823 also includes a programmable, low-noise microphone bias voltage output to power the microphone directly. These power management features eliminate the requirement for an external LDO to power the ADC and the microphone, reducing system cost.

An ENABLE pin on the device is used to completely power down the device and microphone, and allows the device to enter an extremely low power state as it consumes less than 1μ A and extends the battery life of the remote. Coupled with this very low power standby state is the ability for the device to wake up in <50ms. The very fast wake-up time ensures that the initial voice command of the user is properly processed.

The CX20823 is available in a 3x3mm, 20-pin, QFN package.

Key Features

- Low-power audio ADC with 94dB SNR and –80dB THD
- Support for audio line input
- Power consumption:
 - < 1µA in standby</p>
 - < 8mW all-on</p>
 - Resume play from standby in <50ms

- Integrated LDOs allow operation from a single, floating battery supply directly (VDDMIC) 1.71V to 3.6V
- I²S voltage level can be independent from the chip power supply
- Differential or single-ended microphone/line inputs with low-noise programmable gain pre-amp—PGA gain 6dB to 24dB in 1dB steps
- Low-noise microphone bias voltage; programmable up to 90% of VDDMIC
- On-chip frac-N PLL for flexible clocking options
- Two programmable biquads that are configurable as Q-notch, high pass, low pass, or other type of filters
- DRC with gain
- DC blocking filter
- Two-wire I²C slave control interface
- Configurable I²S audio data interface supports:
 - Master and slave configurations
 - Sample rates of: 8kHz, 16kHz, 24kHz, 32kHz, and 48kHz
 - Sample widths of: 8, 16, and 24 bits
 - I²S, left-justified, right-justified, PCM, and TDM modes
- 3x3mm, 20-pin QFN package

System Block Diagram



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Electrical Specifications

Test Conditions:

- AVDD18 = 1.8V
- VDDMIC= 2.8V
- DVDD1 2 = 1.2V
- 25°C
- fin = 1kHz
- fs = 16kHz
- 24-bit audio data

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Input full-scale signal level	Single-ended PGA gain = 0dB	-	0.5	-	Vrms
MIC PGA input-referred noise floor	A-weighted PGA gain = 24dB	-	–115	-	dBV
ADC SNR	A-weighted PGA gain = 0dB	-	94	-	dB
ADC THD+N	–1dBFS PGA gain = 0dB	-	-80	-	dB
Micbias Voltage level	-	0.65x VDDMIC		0.9x VDDMIC	V
Micbias current sourcing capability	-	-		3	mA
Micbias output integrated noise	A-weighted	-	–110	-	dBV
MCLK frequency	-	6		50	MHz

Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Digital core supply VDDCORE (internally generated)	0.9	1.0	1.1	V
Analog supply AVDD (internally generated)	1.62	1.8	2.0	V
VDDMIC (Micbias/LDO supply)	1.71		3.6	V
VDDIO	1.62		3.6	V

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