Device
Engineering
Incorporated

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DEI1166
OCTAL GND/OPEN INPUT, PARALLEL OUTPUT INTERFACE IC

FEATURES

- Eight GND/OPEN discrete inputs
  - Meet electrical requirements for ABD0100 GND/OPEN discrete input.
  - Hysteresis provides noise immunity.
  - Internal pull up resistor with 1mA source current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160D, Section 22, Cat A3 and B3.
- 3.3V or 5V TTL/CMOS compatible digital IO
  - 8 tri-state outputs
  - /CS & /OE control inputs
- Logic Supply: 3.3V or 5V
- Analog Supply: 5V to 18V
- 24L TSSOP package

PIN ASSIGNMENTS

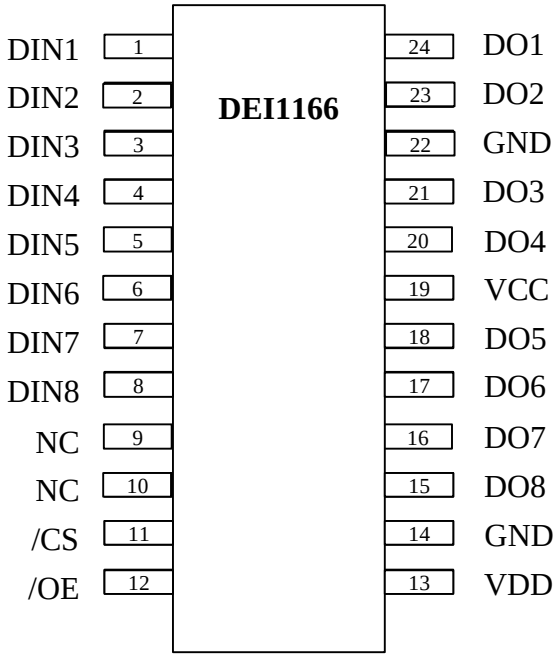

Figure 1 DEI1166 Pin Assignment (24 Lead TSSOP)

Table 1 Pin Descriptions

Pins	Name	Description
8-1	DIN[8:1]	Discrete Inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The threshold and hysteresis characteristics are determined by the applied VDD voltage.
9-10	NC	Not Connected.
11	/CS	Chip Select Logic Input. Low input selects the device.
12	/OE	Output Enable Logic Input. Low input when /CS is low will enable the tri-state outputs.
13	VDD	Analog Supply. +5 to +18V
14	GND	Analog Ground.
19	VCC	Logic Supply. +3.3V or +5V
22	GND	Logic Ground.
15,16,17,18,20,21,23,24	DO[8:1]	Logic Outputs. Eight tri-state data outputs.

FUNCTIONAL DESCRIPTION

The DEI1166 is an eight-channel parallel-output discrete-to-digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via a parallel 3-state output.

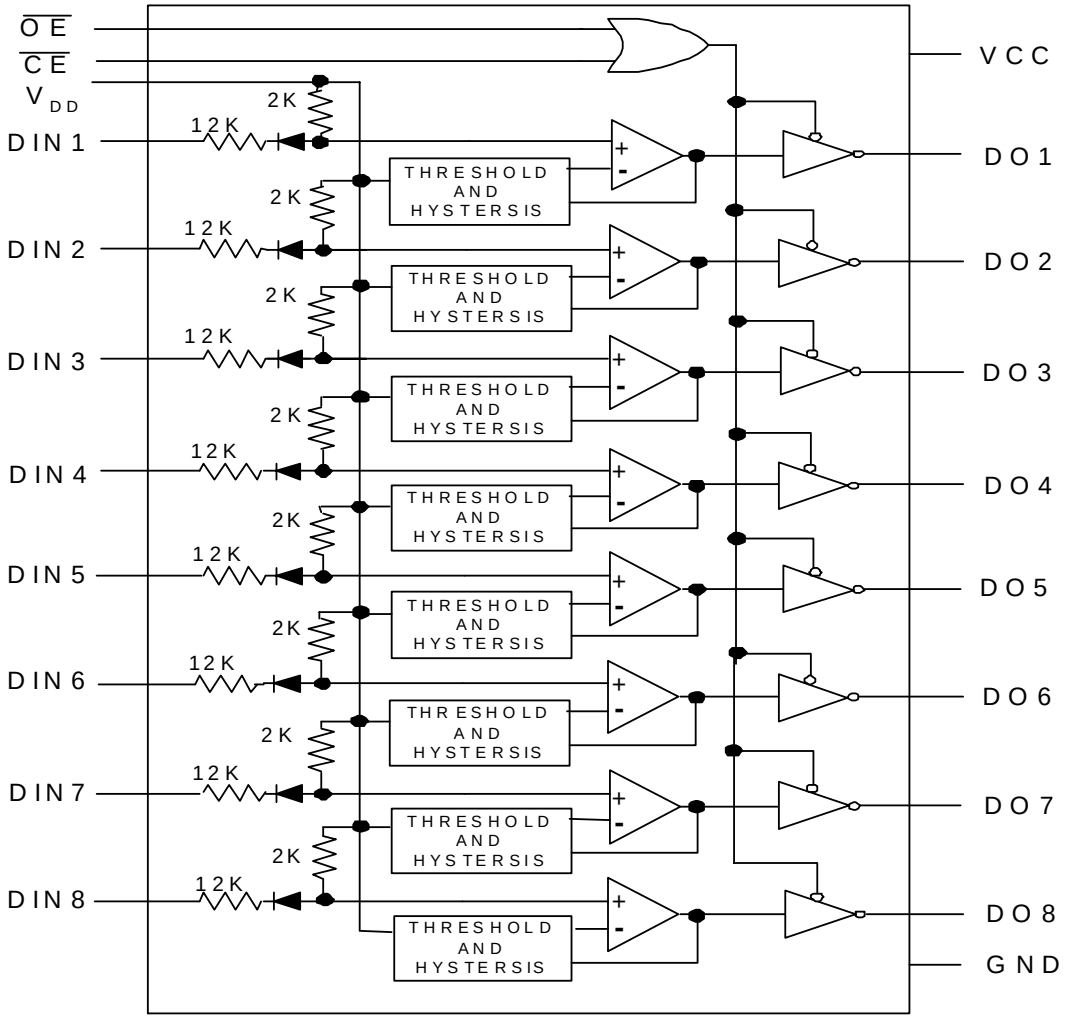

Figure 2 DEI1166 Function Diagram

Table 2 Truth Table

/CE	/OE	DIN[8:1]	DO[8:1]
L	L	Open	L
L	L	Ground	H
H	X	X	High Z
X	H	X	High Z

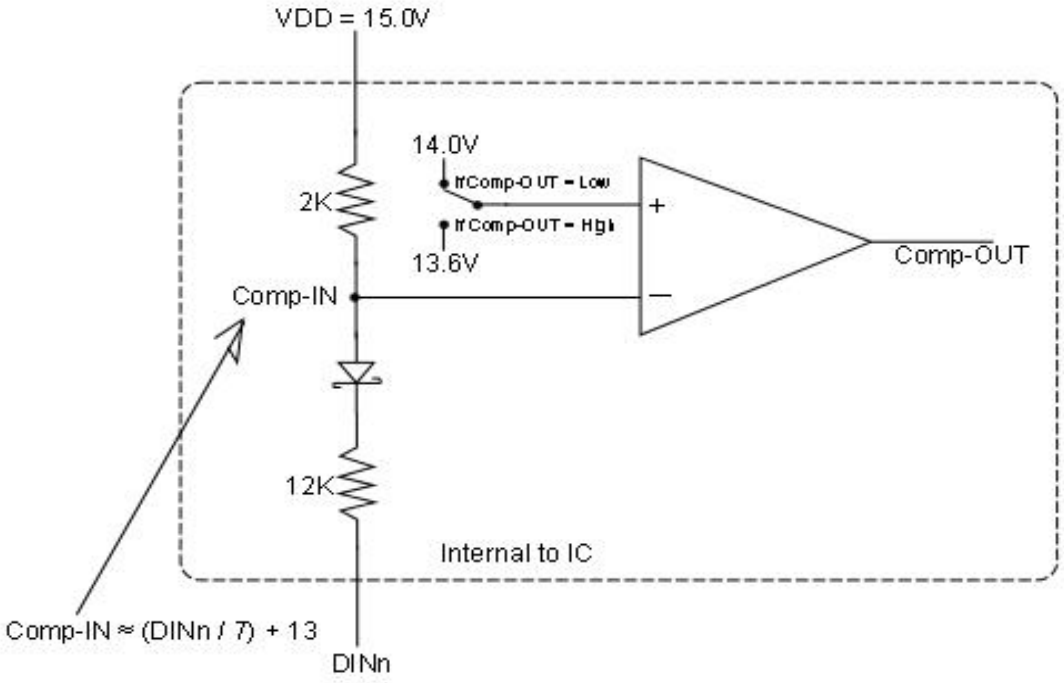

Figure 3 Discrete Input Circuit

DIN[8:1] INPUT STRUCTURE

Each of the eight discrete inputs consists of the circuit in Figure 3. This circuit compares two voltages, one generated internally, and one a function of an external pin, DIN. The voltage applied to DIN divided by 7, and offset by +13V, so the input at DIN must be approximately 7V, so that the internal voltage to the comparator, Comp-IN, is 14V, 7 / 7 +13. The comparator will change states, and also change the internal reference from 14V to 13.6V. This reinforces the switching (hysteresis), such that the DIN input must be lowered from 7V to 4.2V to again switch the comparator.

The actual switch limits are dependent on VDD, as shown below, but are independent of VCC. The divider ratio remains fixed, however, the offset changes proportional to VDD.

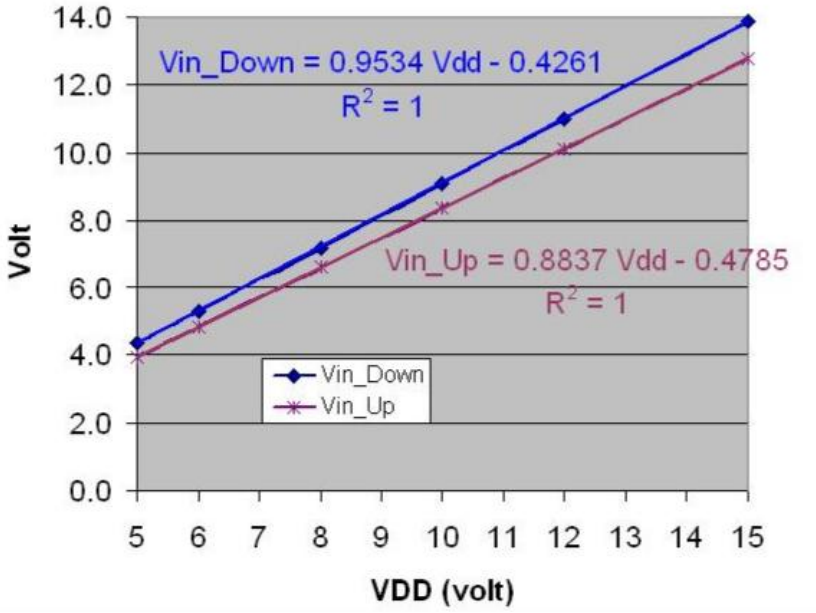

Figure 4 DIN Threshold vs. Vdd

Figure 5 depicts the resistance value that when applied between the input and ground, causes the comparator to switch. Lower effective R_Din values can be achieved by adding an external diode isolated pull-up resistor to Vdd (or higher) supply.

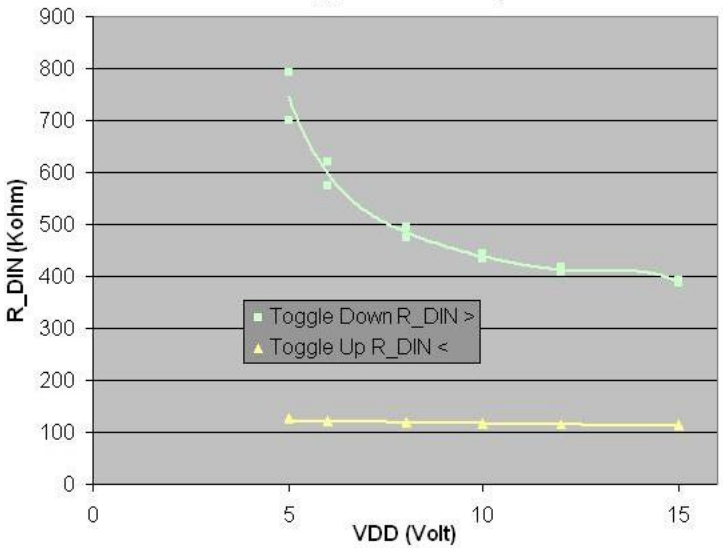

Figure 5 Input switching resistance

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LIGHTNING PROTECTION

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160D, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.

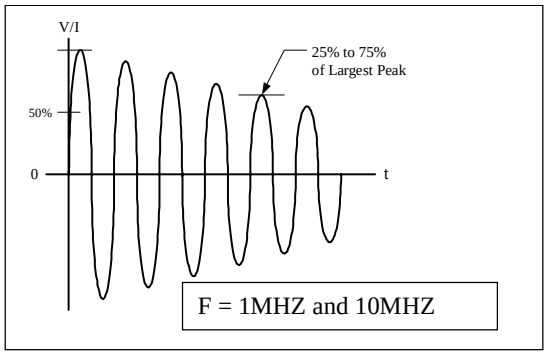

Figure 6 Voltage / Current Waveform 3

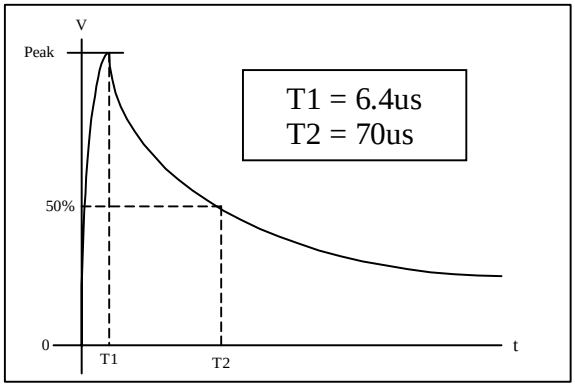

Figure 7 Voltage / Current Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25 Ohms
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ohms
- Waveform 5A Voc / Isc = 300V / 300A => 1 Ohm

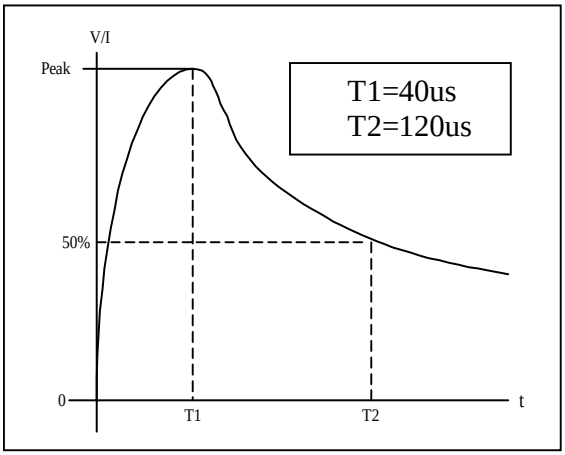

Figure 8 Voltage / Current Waveform 5A

NOTE

It is possible to achieve higher level lightning immunity by adding a 1K Ohm series resistor and a Transient Voltage Suppressor (TVS) to clamp the inputs below 600V. The 1K Ohm resistance reduces the input threshold. For example, with Vdd = 15V, the thresholds become:

Max LH threshold = 15.3V
Min HL threshold = 11.3V

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNITS
Vcc Supply Voltage		-0.3	+7.0	V
Vdd Supply Voltage		-0.3	20	V
Operating Temperature Plastic Package		-55	+125	°C
Storage Temperature Plastic Package		-65	+150	°C
Input Voltage DIN[8:1]	Continuous DO160D, Waveform 3, Level 3 DO160D, Waveform 4 and 5, Level 3	-5 -600 -300	+40 +600 +300	V V V
Logic Inputs		-1.5	VCC + 1.5	V
DO[8:1]		-0.5	VCC + 0.5	V
Power Dissipation @ 85 °C: (> 10 Sec) 24L TSSOP			0.8	W
Junction Temperature: Tjmax, Plastic Packages			145	°C
ESD per JEDEC A114-A Human Body Model Logic and Supply pins DIN pins			2000 1000	V
Peak Body Temperature -G Package			260	°C

Notes:
1. Voltages referenced to Ground
2. Stresses above absolute maximum ratings may cause permanent damage to the device.

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	5.0V±10%, 3.3V±10% 5.0 to 18V
Logic Inputs	/CS, /OE	0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40V
Operating Temperature -TES -TMS		 -55 to +85 ºC -55 to +125 ºC

Table 5 DC Electrical Characteristics

Symbol	Parameter	Test Conditions	VCC (V)	LIMITS		Unit
				-55 to +85°C	**-55 to +125°C**	
LOGIC INPUTS AND OUTPUTS VDD = +5.0V to 18V						
V_{IHmin}	Min High level input voltage		3.0 5.5	2.0 2.0	2.0 2.0	V
V_{ILmax}	Max Low level input voltage		3.0 5.5	0.8 0.8	0.8 0.8	V
V_{OHmin}	Min High level output voltage	$\|I_{OUT}\| < 20uA$	3.0 5.5	VCC – 0.1	VCC – 0.1	V
		$\|I_{OUT}\| < 4.5mA$	4.5 5.5	3.2 4.5	3.0 4.3	V
V_{OLmax}	Max Low level output voltage	$\|I_{OUT}\| < 20uA$	3.0 5.5	0.1 0.1	0.1 0.1	V
		$\|I_{OUT}\| < 4.5mA$	4.5 5.5	0.33 0.33	0.40 0.40	V
I_{OZmax}	Max 3-state leakage current	Output in Hi Impedance state. Vout = 0V and 5V	5.5	±5.0	±10.0	uA
I_{IILmax}	Max |I| input current	VIN = 0V	5.5	-280	-300	uA
DISCRETE INPUTS VDD = +14V						
V_{IHmin}	Min High level input voltage		3.0 to 5.5	13.3	13.5	V
V_{ILmax}	Max Low level input voltage		3.0 to 5.5	11.5	11.5	V
$V_{Ihst-min}$	Min input hysteresis voltage		3.0 to 5.5	1.0	1.0	V
I_{IHmax}	Max High level input current	Vin = 18V Vin = 40V	3.0 to 5.5	10 40	10 40	uA
I_{ILmax}	Max |I| Low level input current	Vin = 0V	3.0 to 5.5	-1.3	-1.3	mA
I_{ILmin}	Min |I| Low level input current	Vin = 0V	3.0 to 5.5	-0.7	-0.7	mA
DISCRETE INPUTS VDD = +5.0V						
V_{IHmin}	Min High level input voltage		3.0 to 5.5	4.7	4.8	V
V_{ILmax}	Max Low level input voltage		3.0 to 5.5	3.5	3.5	V
$V_{Ihst-min}$	Min input hysteresis voltage		3.0 to 5.5	0.36	0.36	V
I_{IHmax}	Max High level input current	Vin = 18V Vin = 40V	3.0 to 5.5	10 40	10 40	uA
I_{ILmax}	Max |I| Low level input current	Vin = 0V	3.0 to 5.5	-0.43	-0.43	mA
I_{ILmin}	Min |I| Low level input current	Vin = 0V	3.0 to 5.5	-0.21	-0.21	mA
SUPPLY VOLTAGES VDD = +14V						
ICCmax	Max quiescent logic supply current	Vin(logic) = Vcc or GND VIN[8:1] = open	5.5	400	400	uA
IDDmax	Max quiescent analog supply current	Vin(logic) = Vcc or GND DIN[8:1] = Open DIN[8:1] = GND	 5.5 5.5	 11 23	 11 24	mA

Table 6 AC Electrical Characteristics

Symbol	Parameter (VDD=+5.0V)	VCC (V)	Limits		Unit
			–55 to +85ºC	-55 to +125ºC	
t_{ZLmax}	Maximum propagation delay, /CS↓ and /OE↓ to DO low. (1) (3)	3.0 4.5 5.5	100 53 42	113 59 46	ns
t_{ZHmax}	Maximum propagation delay, /CS↓ and /OE↓ to DO high (1) (3)	3.0 4.5 5.5	100 53 42	113 59 46	ns
t_{HZmax}	Maximum propagation delay, /CS↑ or / OE↑ to DO HI-Z. from D0 Low or high. (1) (2) (3)	3.0 4.5 5.5	100 71 65	110 78 72	ns
t_{HLmin} t_{LHmin}	Minimum data propagation delay, Din to DO (4) (5)	5.0	3.5	3.5	us
t_{Hlmax} t_{LHmax}	Maximum data propagation delay, Din to DO (4) (5)	5.0	420	630	us
$C_{in\text{-}max}$	Maximum logic input Capacitance. (6)		10	10	pF
$C_{out\text{-}max}$	Maximum DO pin capacitance, output in HI-Z state. (6)		15	15	pF

Notes:
1. DO is loaded with 30pF to GND.
2. DO is loaded with 10K Ohms to GND for High output, 10K Ohms to VCC for Low output.
3. Timing measured from V_{IN}=1.5V to ΔV_{OUT}=200mV. See Figure
4. See Figure . The delay is due to both the on chip filter circuits and VDD.
5. Guaranteed by design.
6. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to GND.

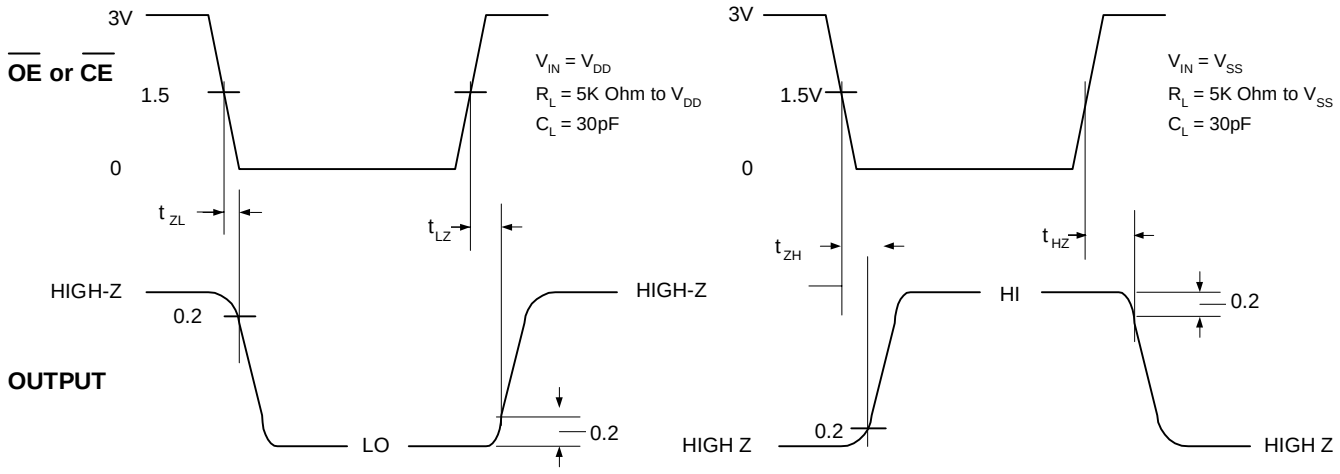

Figure 9 Chip Select or Output Enable to Output Delay

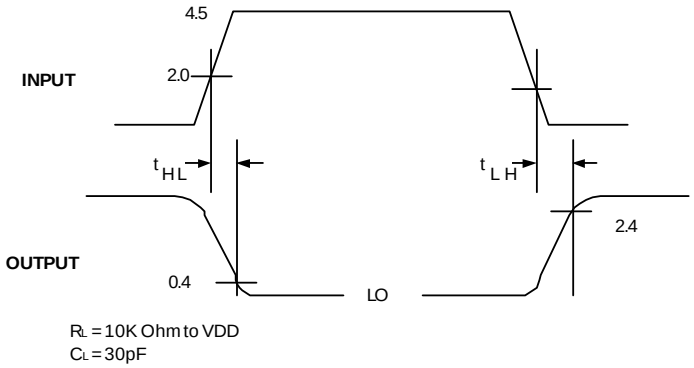

Figure 10 Input to Output Delay

ORDERING INFORMATION

Part Number	Marking	Package	Temperature
DEI1166-TES - G	DEI1166-TES E4	24 TSSOP	-55 / +85 ºC
DEI1166-TMS - G	DEI1166-TMS E4	24 TSSOP	-55 / +125 ºC

PACKAGE DESCRIPTION

24L TSSOP – G Package

Moisture Sensitivity: MSL1 / 260°C
Θja: ~83˚C/W (Mounted on 4 layer PCB)
Θjc: ~16˚C/W
Lead Finish: NiPdAu (e4)

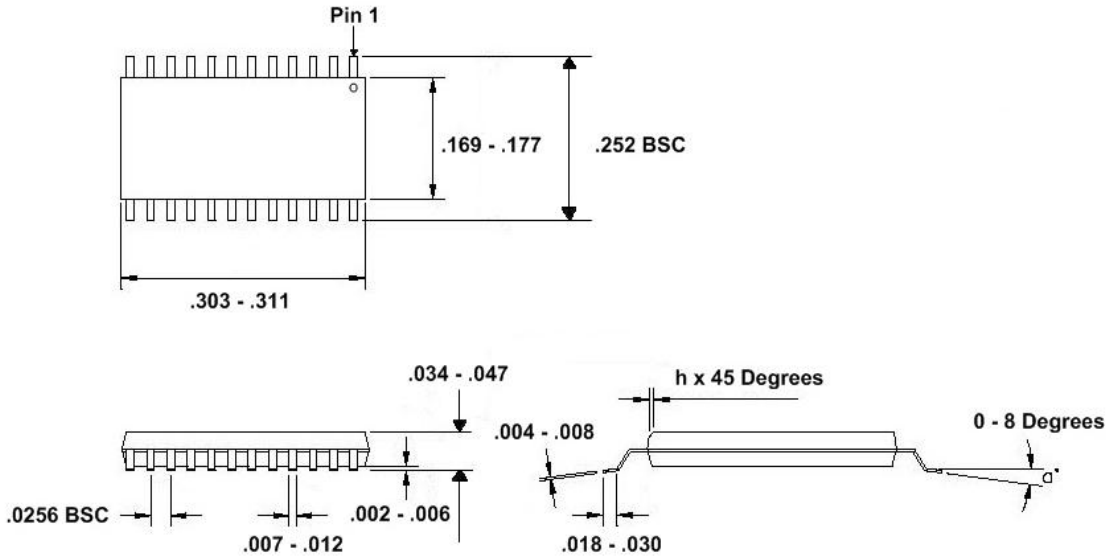

Figure 11 Outline Drawing