Device
Engineering
Incorporated

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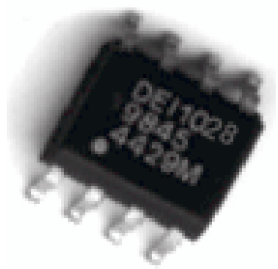
DEI 1028
Voltage Clamping Circuit

FEATURES

- Protection for power electronics on 28VDC avionics or industrial power bus to DO-160, Category Z, Abnormal Surge Voltage (DC) levels.
- Controls power P-FET to clamp transient at 34V.
- Small foot print (8L SOIC NB).
- Wide input voltage range.
- Programmable Undervoltage Lockout.
- Logic compatible On/Off input.
- Stable over temperature.
- Soft start delay.



GENERAL DESCRIPTION

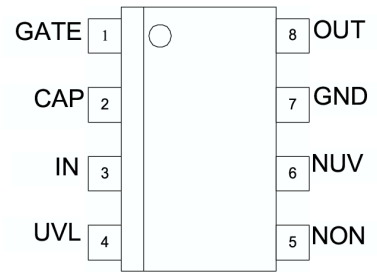
The DEI1028 is a control circuit for a 28VDC power bus voltage clamp. It is designed for use as the front end to a 28VDC input power supply to provide transient voltage protection. It controls the gate drive of a P-Channel power MOSFET to linearly clamp the output during over-voltage transients. The output voltage is maintained below the clamping threshold of 35V (max) which is adequate to protect most Commercial-Off-The-Shelf switching supplies, linear regulators, and op amps.

There is an Undervoltage Lockout feature that shuts the Power MOSFET off when the input voltage is below a user programmed threshold. An open collector logic output annunciates the under-voltage status. There is also a logic on/off input which may be used to control the power circuit. An external capacitor may be used to set a delay from when input power is applied to when the MOSFET is turned on.

Table 1 Pin Definitions

Pin #	Name	Description
1	**GATE**	**OUTPUT**. Controls the gate of the external P-channel power MOSFET.
2	**CAP**	**IN/OUT**. Controls the soft start delay of the device. Use 0.22uF for 200ms minimum soft start time.
3	**IN**	**INPUT**. Power input for the DEI1028 Voltage Clamp.
4	**UVL**	**INPUT**. Controls the under voltage lockout condition of the device.
5	**NON**	**INPUT**. Logic low enables device. Logic high disables device.
6	**NUV**	**OUTPUT**. Open collector output. Active low when IN is below UVL threshold.
7	**GND**	**POWER.** Ground
8	**OUT**	**INPUT**. Feedback to gate control from drain of Power MOSFET.

Pin Diagram



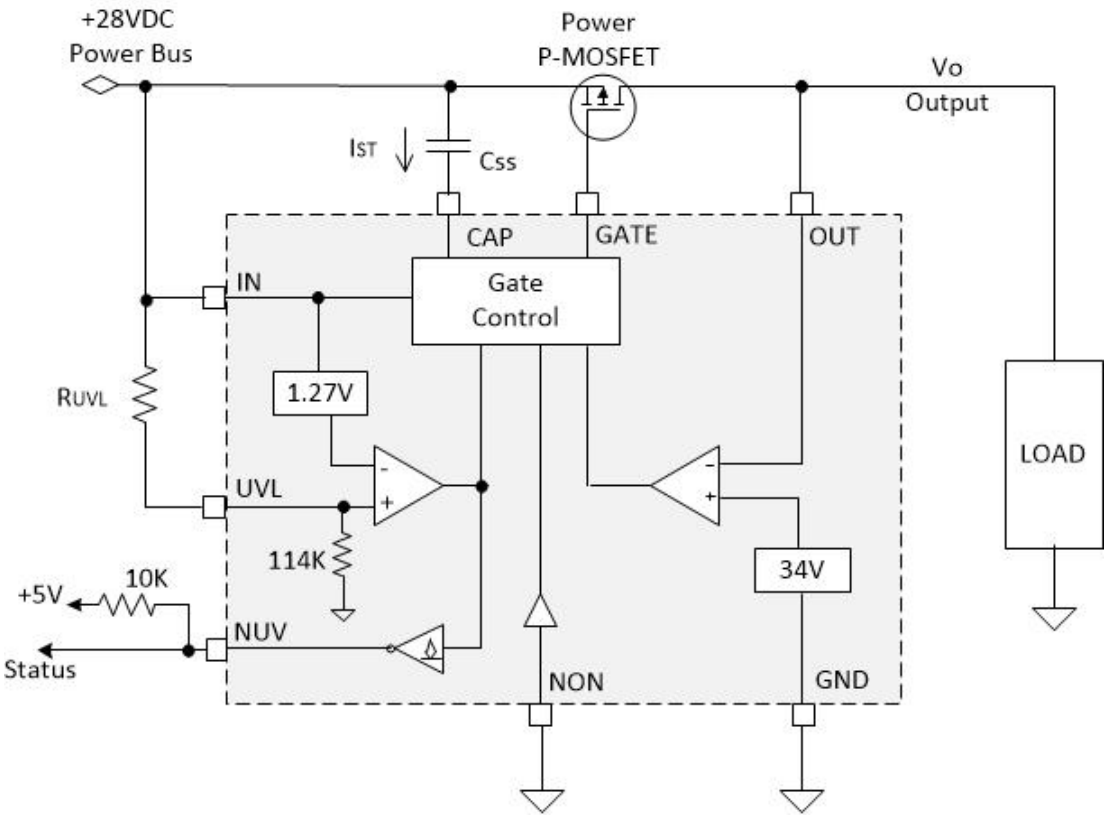


Figure 1 Function Diagram and Typical Application

ELECTRICAL DESCRIPTION

Table 2 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
IN Pin:	Continuous 1 ms Transient 100 ms Transient	V_{IN}	-0.5 -50 -	+40 - +100	V
UVL Pin:	Relative to V_{IN}	V_{UVL}	-6	-0.5	V
CAP Pin:	Relative to V_{IN}	V_{CAP}	-20	20	V
GATE Pin:	Relative to V_{IN}	V_{GATE}	-10	0.5	V
NON Pin:		V_{NON}	-0.5	6.0	V
NUV Pin:		V_{NUV}	-0.5	20	V
OUT Pin:		V_{OUT}	-0.5	40	V
Operating Temperature		T_A	-55	125	^oC
Storage Temperature		T_{STG}	-65	125	^oC

Notes:
(1) Voltages are relative to GND unless otherwise stated
(2) Stresses above absolute maximum ratings may cause permanent damage to the device.

Table 3 Operating Characteristics

Parameter	Symbol	Conditions [4]	Min	Max	Units
Clamp					
Clamp output voltage	$V_{O(CL1)}$	V_{IN} = 40 V, 60V	33	35	V
Clamp output voltage	$V_{O(CL2)}$	V_{IN} = 80 V	33	35	V
Source-Gate FET voltage (ON)	$V_{SG(1)}$	R_{UVL} = 13.6 KΩ, V_{IN} = 14V[5]	9	10	V
Source-Gate FET voltage (OFF)	$V_{SG(2)}$	R_{UVL} = 13.6 KΩ, V_{IN} = 10V[5]	0	0.7	V
Source-Gate FET voltage (ON)	$V_{SG(1)}$	R_{UVL} = 7 KΩ, V_{IN} = 25V[5]	9	10	V
Source-Gate FET voltage (OFF)	$V_{SG(2)}$	R_{UVL} = 7 KΩ, V_{IN} = 19.5V[5]	0	0.7	V
Source-Gate FET voltage (Linear control)	$V_{SG(3)}$	35V < V_{IN} ≤ 80V, V_{OUT}= Clamp Voltage (33-35V)	0.7	9	V
Turn-on time	t_{ON}	C_{SS} = 0.22uF [1] See Figure 3 & Figure 4	200	550	ms
Power-on delay factor	R_{ST}	V_{IN} > 10V R_{ST} = V_{ST}/I_{ST} = CAP switch voltage wrt V_{IN} / CAP Charge current	0.92	2.5	MΩ
Output overshoot voltage	V_{OMX}	See Figure 5[1]		35	V
Output settling time	t_S	See Figure 5[1]		2	ms
Supply Input					
Supply Current	I_{IN}	VIN = 30 V		5	mA
Logic IO					
NON input logic 1 level	V_{IH}	V_{IN} = 8 to 30 V	2.8		V
NON input logic 0 level	V_{IL}	V_{IN} = 8 to 30 V		0.8	V
NON input logic 0 current	I_{IL}	V_{NON} = 0 V V_{IN} = 8 to 30 V	-300	-30	µA
NUV output logic 1 level	V_{OH}	R_{UVL} = 13.6 KΩ, V_{IN} = 14 V, R_{PU} = 10 kΩ to 5V See Figure 6.	4.75		V
NUV output logic 0 level	V_{OL}	R_{UVL} = 13.6 KΩ, V_{IN} = 10 V I_{OL} = 420 µA See Figure 6.		0.8	V
Under Voltage Lockout (UVL)					
V_{IN} Undervoltage Lockout Threshold	V_{UVL} 13.6K	Minimum V_{IN} where GATE becomes active R_{UVL} = 13.6 KΩ	11.0	13.0	V
	V_{UVL}7K	Minimum V_{IN} where GATE becomes active R_{UVL} = 7 KΩ	21.0	23.0	V

Notes:

1. Guaranteed by design and not production tested.
2. Device must survive this test. Duration of negative voltage must be limited to less than 1ms due to heating effects.
3. MOSFET capacitance (Cgs) must be in the range 500 ~ 5000pF. If below 500pF, an external 470pF capacitor must be connected between the DEI1028 OUT and GATE pins.
4. T_A = -55 to 85 °C (-SES), -55 to 105 °C (-SKS)
5. Measured with 820KΩ load from GATE to Ground

Gate Drive

The DEI1028 device is designed to control the gate of a P-Channel power MOSFET such as the IRF9540. At normal operation the gate output turns the transistor ON to saturation. Below under voltage conditions the MOSFET is shut off. In clamp mode the MOSFET is driven to linear mode, keeping the output at approximately 34 V.

Undervoltage Lockout

An Undervoltage Lockout feature is provided to prevent large currents from flowing through the MOSFET if the input voltage is too low. The resistor is placed between the IN and UVL pins. The following formula is used to determine the resistor value to set the nominal (25 ºC) lockout threshold voltage:

$$R_{UVL}(Ohm) = 114K \times \frac{1.27}{(V_{UVL} - 1.27)}$$

See Figure 2 for temperature characteristics.

Power On Delay

An external capacitor between CAP and the input voltage may be used to set a turn on delay time. See Figure 3. The CAP pin may be left open if no delay capacitor is used.

At start up, the voltage across the capacitor is approximately zero, the voltage at the CAP pin is approximately the input voltage, and the MOSFET is turned off. The 1028 CAP pin provides a current sink (~1ua) to charge the capacitor. The 1028 turns the MOSFET on when the voltage across the capacitor reaches a threshold voltage (~1.5V). The ratio of that threshold voltage over the charge current determines the power on delay time according to:

$$t_{ON}(s) \approx C_{SS}(F) \times R_{ST}\ (Ohm)$$

Where R_{ST} is as specified in Table 3.

Safe Operating Area

The device protects against an 80V spike of ≤100ms duration, and provides overshoot protection. Pulses greater than 80V may cause the device to remove drive to the external FET, turning it off and causing the output to go below its clamped output voltage regulation level. This effect is worse at low temperature. The device provides conditioned power with Vin ≤80V, as described in DO160 Sect 16 Category Z "Typical Abnormal DC Surge Voltage Characteristics". See Figure 7.

Surge Operation

As shown in Figure 7, surges ≤ 80V will regulate and protect. For surges >80V, the device may lose drive to the external FET, but will continue to protect the output. The application designer must consider the safe operating area of the external FET separately.

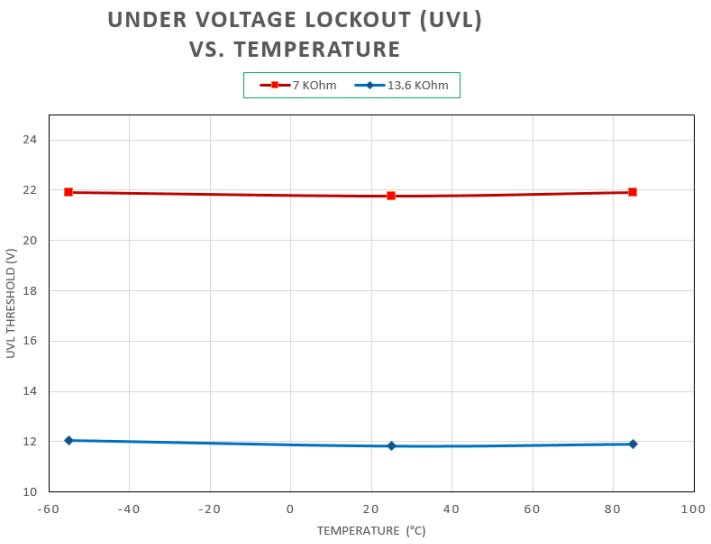


Figure 2 Typical UVL cutoff voltage by temperature for Ruvl = 7K and Ruvl = 13.6K

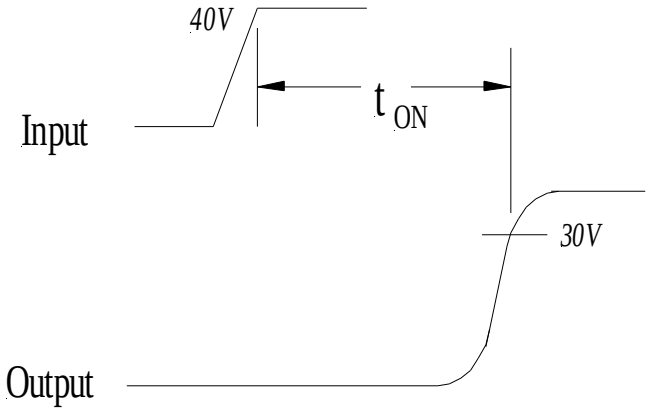


Figure 3 Turn on Time

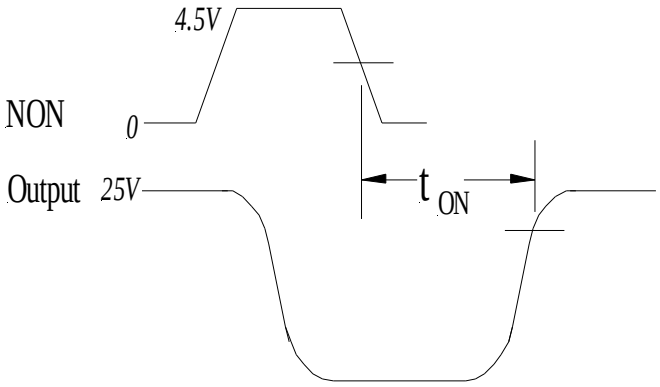


Figure 4 Logic Control ("NON" pin)

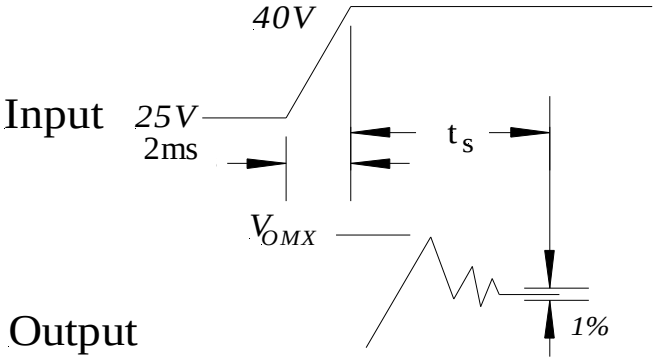


Figure 5 Overshoot and Settling

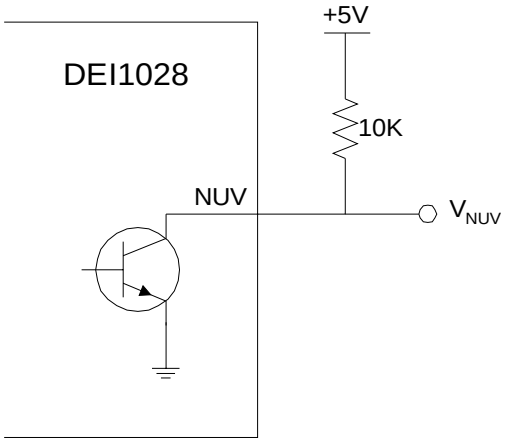


Figure 6 Under Voltage Logic Output

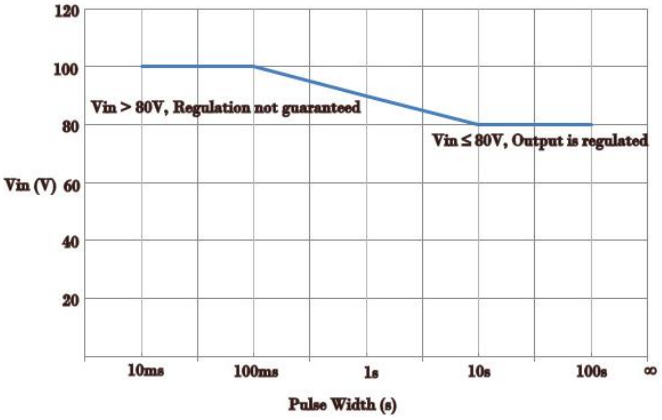


Figure 7 Safe Operating Area (Ta=25C)

PACKAGE DESCRIPTION

8 Lead SOICN

Table 4 Package Characteristics, 8L SOICN

PACKAGE TYPE	8 LEAD SOICN
REFERENCE	8L NB SOIC G
THERMAL RESISTANCE: θ_{JA} (4 layer PCB with Power Planes) θ_{JC}	 135 °C/W 40 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL	MSL 1 / 260°C
LEAD FINISH MATERIAL / Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MS-012-AC

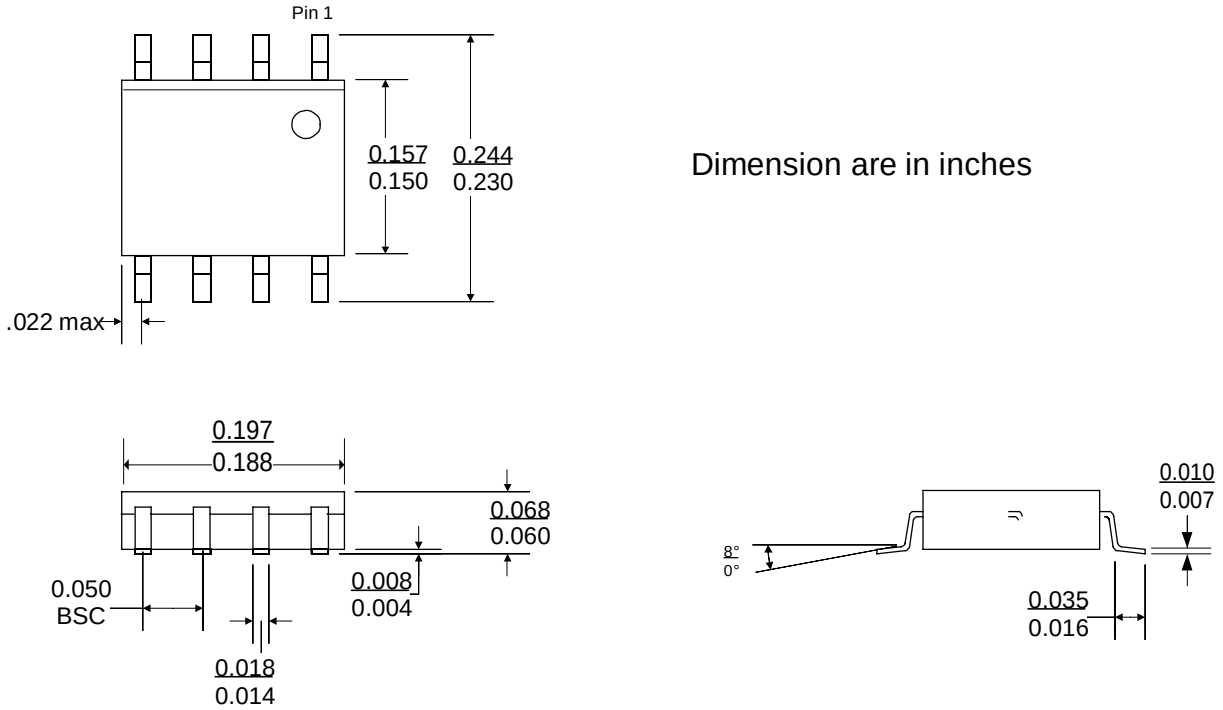


Figure 8 Mechanical Outline, 8L SOICN

ORDERING INFORMATION

Table 5 Ordering Information

PART NUMBER	MARKING	PACKAGE	TEMPERATURE RANGE
DEI1028–SES-G	DEI1028 E4	8L NB SOIC G	-55 / +85 ℃
DEI1028–SKS-G	DEI1028 E4 + Blue Dot	8L NB SOIC G	-55 / +105 ℃