Device
Engineering
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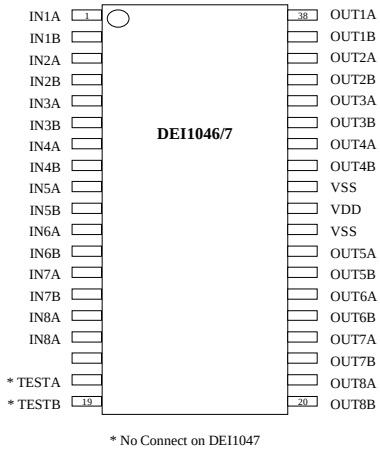
DEI1046, DEI1047, DEI1148
OCTAL ARINC 429 LINE RECEIVER

FEATURES

- Octal ARINC 429 to TTL/CMOS logic line receivers
- Operates from single +5V ± 10% or 3.3V + 10%, -5% power supply
- ARINC inputs internally protected to lightning requirements of DO-160 Level A3
- Operates in high noise environment
  - Input Common Voltage Range: ± 20V
  - 2V minimum Input hysteresis
- Optional logic level TEST inputs on DEI1046.
- Package Options
  - 38L TSSOP, 4.4mm body (DEI1046/1047)
  - 44L MQFP, 13.9mm footprint (DEI1148)

DEI1046/1047 PINOUT



* No Connect on DEI1047

Table 1a DEI1046/1047 Pin Description

PIN	NAME	DESCRIPTION
15,13,11, 9, 7,5,3,1	IN[8:1]A	429 INPUTS. ARINC 429 format serial digital data "A" inputs.
16,14,12, 10, 8,6,4,2	IN[8:1]B	429 INPUTS. ARINC 429 format serial digital data "B" inputs.
18	TESTA	LOGIC INPUT. Test input A on DEI1046. No Connect on DEI1047.
19	TESTB	LOGIC INPUT. Test input B on DEI1046. No Connect on DEI1047.
21,23,25,27, 32,34,36,38	OUT[8:1]A	LOGIC OUTPUTS. CMOS/TTL format serial digital data "A" outputs.
20,22,24,26, 31,33,35,37	OUT[8:1]B	LOGIC OUTPUTS. CMOS/TTL format serial digital data "B" outputs.
29	VDD	POWER INPUT. 5 VDC OR 3.3VDC.
28, 30	VSS	POWER INPUT. Ground.

DEI1148 PINOUT

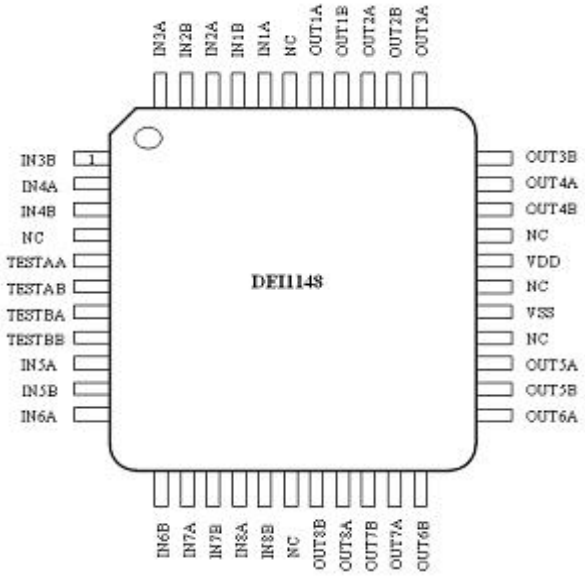


Table 1b DEI1148 Pin Description

PIN	NAME	DESCRIPTION
15, 13, 11, 9, 2, 44, 42, 40	IN[8:1]A	429 INPUTS. ARINC 429 format serial digital data "A" inputs.
16, 14, 12, 10, 3, 1, 43, 41	IN[8:1]B	429 INPUTS. ARINC 429 format serial digital data "B" inputs.
5	TESTAA	LOGIC INPUT. Test input A (+) for odd channels.
6	TESTAB	LOGIC INPUT. Test input A (-) for odd channels.
7	TESTBA	LOGIC INPUT. Test input B (+) for even channels.
8	TESTBB	LOGIC INPUT. Test input B (-) for even channels.
19, 21, 23, 25, 32, 34, 36, 38	OUT[8:1]A	LOGIC OUTPUTS. CMOS/TTL format serial digital data "A" outputs.
18, 20, 22, 24, 31, 33, 35, 37	OUT[8:1]B	LOGIC OUTPUTS. CMOS/TTL format serial digital data "B" outputs.
29	VDD	POWER INPUT. 5 VDC OR 3.3VDC.
27	VSS	POWER INPUT. Ground.

FUNCTIONAL DESCRIPTION

The DEI1046/7/1148 is a BiCMOS device which contains eight differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. Each channel operates independently and meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 "DEI1046/7/1148 Block Diagram and Truth Table".

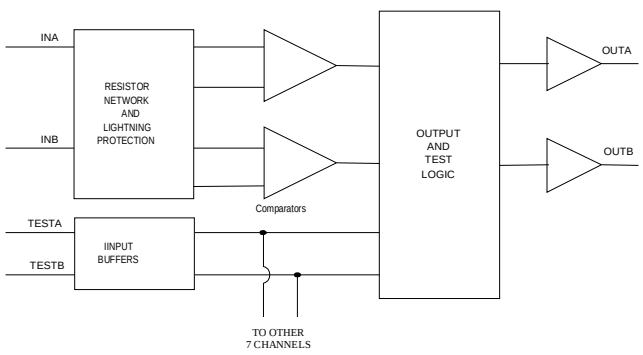
The device is designed to operate in a high noise environment. Inputs are accepted over a +/- 20V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160 Level A3.

The DEI1046 & 1148 devices provide logic level TEST inputs for built in system test. They force the outputs of all eight receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode. The DEI1046 has a single test port which controls all 8 channels. The DEI1148 has two test ports, each controlling 4 channels. Test inputs are not bonded out on the DEI1047; they are internally connected to logic 0.

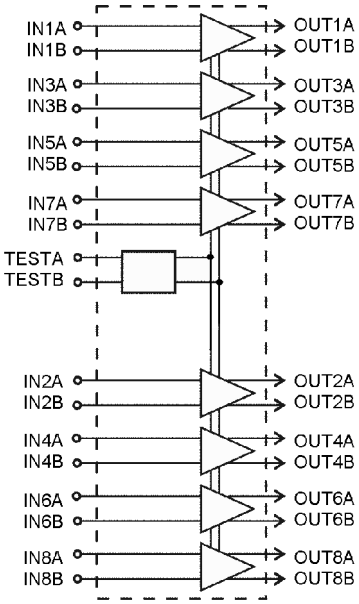
The ARINC inputs may optionally be connected to the ARINC bus through external 10K ohm series resistors. These resistors may be added in combination with transient voltage suppressors to achieve lighting protection beyond the level 3 limits.

Block Diagram Typical Channel

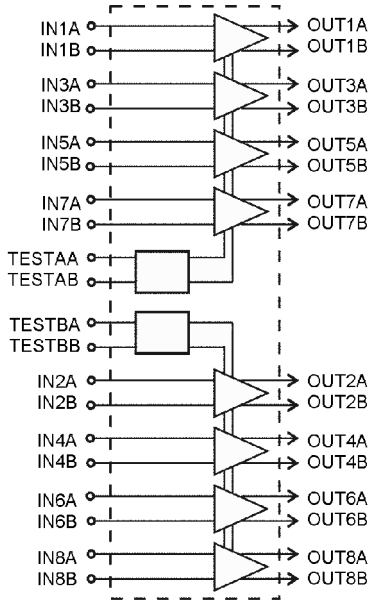


Truth Table

INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TEST A	TEST B	$A_{IN} - B_{IN}$ V	OUT A	OUT B	Logic
0	0	Logic +1	1	0	ONE
0	0	Logic -1	0	1	ZERO
0	0	NULL	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL



DEI1046 / 1047*



DEI1148

*Note: TEST inputs are not implemented on DEI1047. They are internally connected to logic 0.

Figure 1 DEI1046/1047/1148 Block Diagrams and Truth Table

ELECTRICAL DESCRIPTION

Table 2 Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to V_{SS})	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)	-40	+40	V
Input Voltage (TESTA/B Inputs)	V_{SS} – 0.3	V_{DD}+0.3	V
Power Dissipation @ 85 °C		800	mW
Junction Temperature, Tjmax (limited by molding compound Tg)		145	°C
Peak Body Temperature		260	°C
Lightning Protection (ARINC 429 Channel Inputs) Waveform 3 (2) Waveform 4, 5A, 5B* (2) (3)	 -600 -300	 +600 +300	 V V
ESD per JEDEC A114-A Human Body Model	-1000	1000	V

Notes:
1. Stresses above these limits can cause permanent damage.
2. Per DO160, Sect 22 Level 3A. See Figures 4-6.
3. Inputs can be protected to withstand higher stress by adding series resistors and shunt TVS on inputs. Inputs withstand 1500V Waveform 5A when clipped ≤ 600V.

Table 3 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	Vdd	+5V ± 10% +3.3V +10% -5%
Logic Input Levels	$V_{TESTA,B}$	0 to Vdd
Operating Temperature -xEx -xMx	Ta	 -55 to +85°C -55 to +125°C

Table 4 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C (-xEx); -55°C to +125°C (-xMx)
V_{DD} = +5V ± 10% or 3.3V +10% -5%

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
ARINC INPUTS						
$V_A – V_B$ = Logic +1	OUTA = 1	V_{+1}	6.5	10	13	V
$V_A – V_B$ = Logic -1	OUTB = 1	V_{-1}	-6.5	-10	-13	V
$V_A – V_B$ = Logic Null	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	0	2.5	V
Input Hysteresis		V_{HY}	2.0		4.0	V
$V_A – V_B$ = Null to +1 transition	OUTA = 0→1	V_{T+1+}	5.5		6.5	V
$V_A – V_B$ = +1 to Null transition	OUTA = 1→0	V_{T+1-}	2.5		3.5	V
$V_A – V_B$ = Null to -1 transition	OUTB = 0→1	V_{T-1+}	-6.5		-5.5	V
$V_A – V_B$ = -1 to Null transition	OUTB = 1→0	V_{T-1-}	-3.5		-2.5	V

Conditions: Temperature: -55°C to +85°C (-xEx); -55°C to +125°C (-xMx) V_{DD} = +5V ± 10% or 3.3V +10% -5%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20		+20	V
Input Resistance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	R_{IN}	280K	780K		Ω
Input Resistance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	R_S	140K	390K		Ω
Input Capacitance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_{IN}			10	pF
Input Capacitance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_S			10	pF
TEST INPUTS (not applicable to DEI1047)						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8	I_{IL}			25	µA
Logic 1 Current	V_{IH} = 2.0 DEI1046 DEI1148	I_{IH}			50 25	µA
LOGIC OUTPUTS						
OUT A or OUT B	I_{OH} = -5mA (Vdd=5.0V) I_{OH} = -1.5mA (Vdd=3.3V) TTL Compatible	V_{OH}	2.4			V
	I_{OL} = 5mA (Vdd=5.0V)	V_{OL}			0.5	V
OUT A or OUT B	I_{OL} = -1.5mA (Vdd=3.3V) TTL Compatible	V_{OL}			0.4	V
OUT A or OUT B	I_{OH} = 100µA CMOS Compatible	V_{OH}	V_{DD} – 50mV			V
OUT A or OUT B	I_{OL} = 100µA CMOS Compatible	V_{OL}			V_{SS} + 50mV	V
SUPPLY CURRENT						
V_{DD} Current	Data Rate = 0MHz, A/BIN =open, A/BOUT=open, Vdd = 5.5V or 3.63V	I_{DD}	1.5	3	8.5	mA

Notes:

1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to Ground unless otherwise noted.

Table 5 Switching Characteristics

PARAMETER	**TEST CONDITION**	**SYMBOL**	**MAX** Vdd 3.3V	**MAX** Vdd 5V	**UNITS**
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	t_{LH}	1000	900	ns
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	t_{HL}	1000	900	ns
OUT A/B rise time	10% to 90%, C_L = 50pF	t_r	50	25	ns
OUT A/B fall time	10% to 90%, C_L = 50pF	t_f	50	25	ns
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOH}	100	60	ns
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOL}	100	60	ns

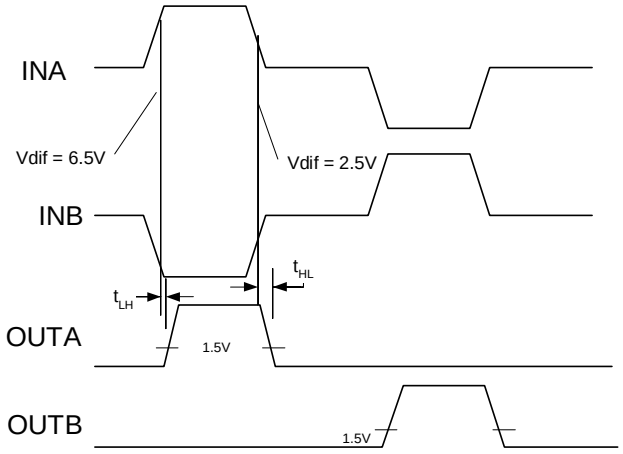


Figure 2 ARINC 429 Input to Logic Output Switching Waveform

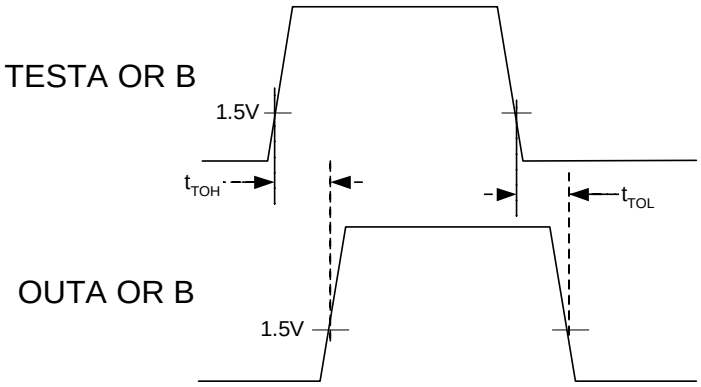


Figure 3 TEST Input to Logic Output Switching Waveform

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

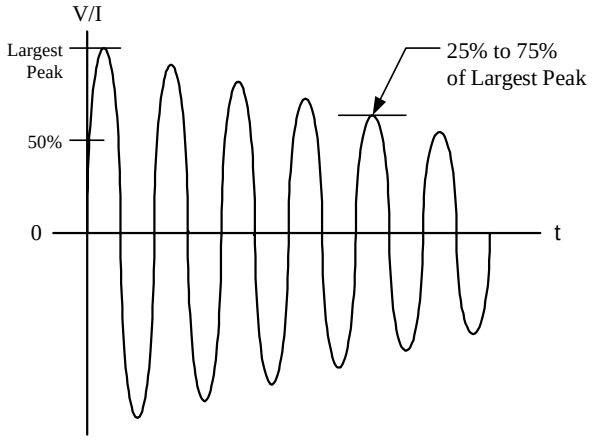


Figure 4 DO160 Lightning Induced Transient Voltage Waveform #3.
Voc = 600V, Isc = 24A, Frequency =1MHz +-20%

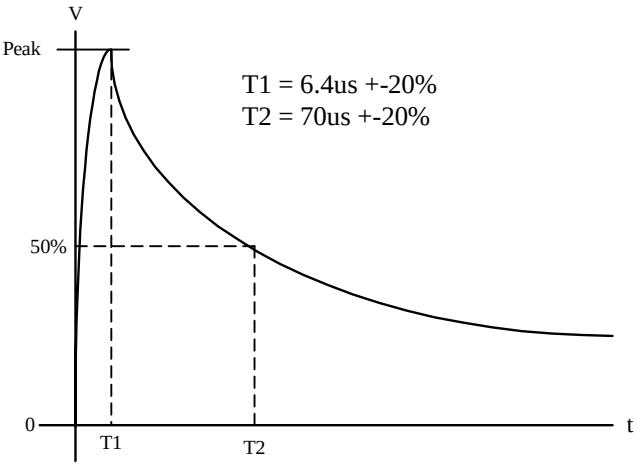


Figure 5 DO160 Lightning Induced Transient Voltage Waveform #4.
Voc = 300V, Isc = 60A

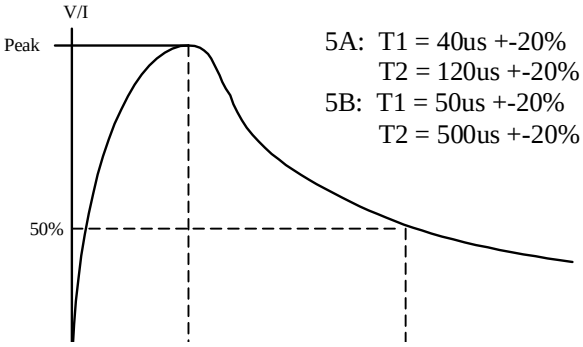


Figure 6 DO160 Lightning Induced Transient Voltage Waveform #5.
Voc = 300V, Isc = 300A

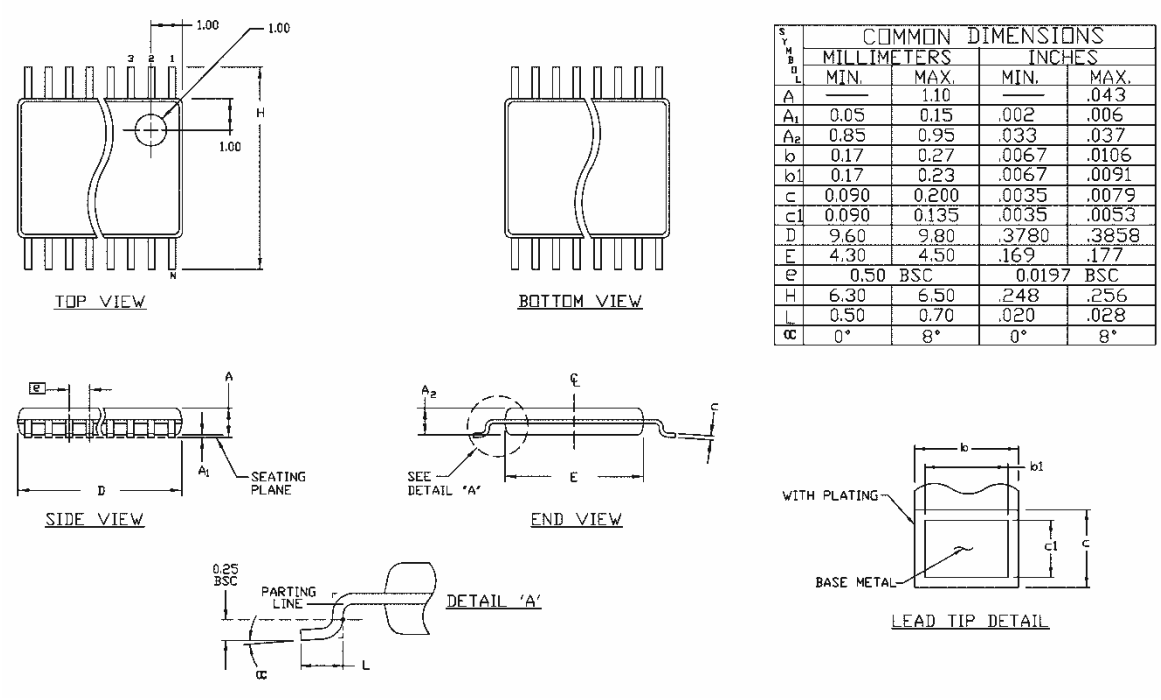
ORDERING INFORMATION

Table 6: Ordering Information					
DEI PN	**MARKING (1)**	**TEST INPUTS**	**TEMPERATURE RANGE**	**PACKAGE**	**SCREENING**
DEI1046-TES-G	DEI1046-TES E4	YES	-55/+85 ºC	38L TSSOP G	Standard
DEI1046-TMS-G	DEI1046-TMS E4	YES	-55/+125 ºC	38L TSSOP G	Standard
DEI1047-TES-G	DEI1047-TES E4	NO	-55/+85 ºC	38L TSSOP G	Standard
DEI1047-TMS-G	DEI1047-TES E4	NO	-55/+125 ºC	38L TSSOP G	Standard
DEI1148-QES-G	DEI1148-QES E3	YES	-55/+85 ºC	44L MQFP G	Standard
DEI1148-QMS-G	DEI1148-QMS E3	YES	-55/+125 ºC	44L MQFP G	Standard
Notes: 1. All packages marked with Lot Code and Date Code. "E4" after Date Code denotes Pb Free category.					

Table 7: Screening Process	
SCREENING	**STANDARD**
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ 85°C or 125°C
LOW TEMPERATURE	0.65% AQL@-55°C

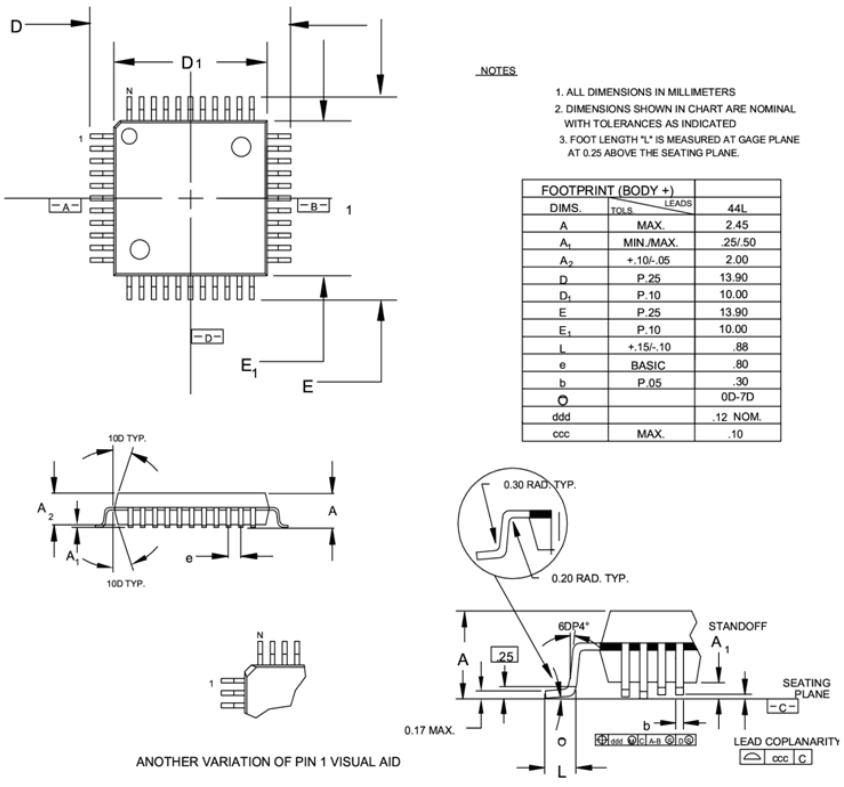
Table 8: Package Characteristics		
PACKAGE TYPE	**38L TSSOP, Green**	**44L MQFP, Green**
REFERENCE	38L TSSOP G	44L MQFP G
θ_{JA} (4 layer PCB with Power Planes)	75 °C/W	52 °C/W
θ_{JC}	15 °C/W	12 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 2 / 260°C	MSL 3 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4	Matte Sn e3
Pb-Free DESIGNATION	RoHS Compliant	RoHS Compliant
JEDEC REFERENCE	MO-153-BD-1	MO-112 VAR AA-1

PACKAGE DESCRIPTIONS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10	——	.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.17	0.27	.0067	.0106
b1	0.17	0.23	.0067	.0091
c	0.090	0.200	.0035	.0079
c1	0.090	0.135	.0035	.0053
D	9.60	9.80	.3780	.3858
E	4.30	4.50	.169	.177
e	0.50 BSC		0.0197 BSC	
H	6.30	6.50	.248	.256
L	0.50	0.70	.020	.028
α	0°	8°	0°	8°

Figure 7 38L TSSOP Mechanical Outline



FOOTPRINT (BODY +)		
DIMS.	TOLS / LEADS	44L
A	MAX.	2.45
A_1	MIN./MAX.	.25/.50
A_2	+.10/-.05	2.00
D	P.25	13.90
D_1	P.10	10.00
E	P.25	13.90
E_1	P.10	10.00
L	+.15/-.10	.88
e	BASIC	.80
b	P.05	.30
θ		0D-7D
ddd		.12 NOM.
ccc	MAX.	.10

Figure 8: 44L 13.90mm MQFP Mechanical Outline