DEVICE
ENGINEERING
INCORPORATED

385 East Alamo Drive
Chandler, AZ 85225
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1170, DEI1171
ARINC 429 LINE DRIVER WITH RATE SELECT and TRI-STATE

FEATURES

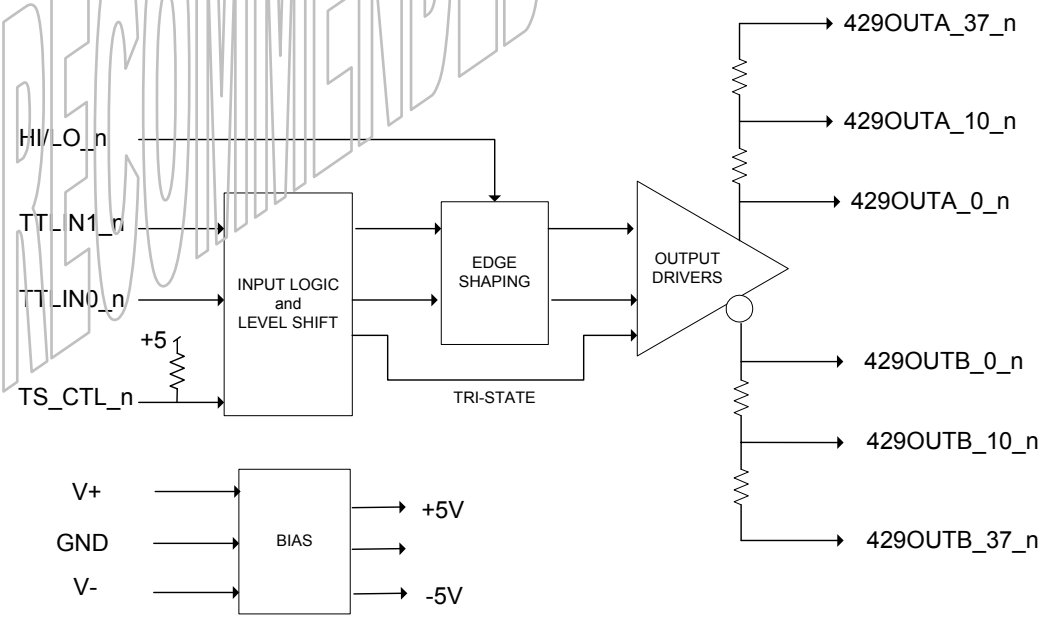
- TTL/CMOS TO ARINC 429 Line Driver.
- Rate control input set Hi (100KBS) or Lo (12.5KBS) speed slew rates.
- Operates from ±9.5V to ±16.5V power supply.
- Drives full ARINC load.
- Tri-State A429 output feature
- 0, 10 and 37.5 Ohm output resistor taps
- Thermally enhanced 5 x 5 mm MLP package
- Outputs Short Circuit Tolerant

GENERAL DESCRIPTION

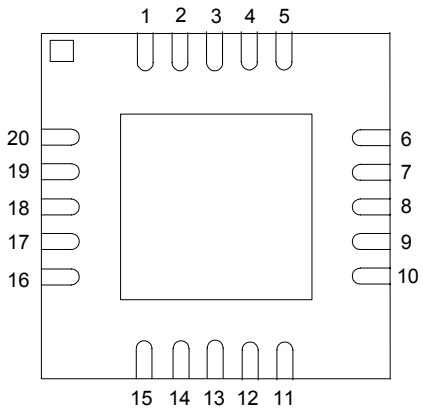
The DEI1170/1 BiCMOS integrated circuits are dual line drivers designed to directly drive the ARINC 429 avionics serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. A TTL/CMOS control input selects the output slew rate for HI (100KBS) and LOW (12.5KBS) speed operation. No external timing capacitors are required. A429 output tri-state capability is enabled by the TS_CTL input.

The exposed pad heatsink of the DEI1170 is connected to V- power supply. The DEI1171 exposed pad is electrically isolated.

FUNCTION DIAGRAM



TERMINAL DESCRIPTION



BOTTOM VIEW

Notes:

1. Package: 20 Lead 5.0 x 5.0mm MLP
2. Exposed Pad is connected V- Supply on DEI1170.
   Exposed Pad is electrically isolated on DEI1171.

Table 1 Pin Description

SIGNAL NAME	PIN	DESCRIPTION
HI/LO	**15**	**LOGIC INPUT.** Slew rate control. 1 = Hi speed. 0 = Low speed.
TTLIN0	**17**	**LOGIC INPUT.** Serial digital data input 0.
TTLIN1	**18**	**LOGIC INPUT.** Serial digital data input 1.
TS_CTL	**1**	**LOGIC INPUT.** Open or '1' disables output Tristate function. '0' Enables output Tristate function.
429OUTA_0	**7**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 0 Ohm
429OUTA_10	**6**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 10 Ohm
429OUTA_37	**5**	**429 OUTPUT.** ARINC 429 format serial digital data output A, 37 Ohm
429OUTB_0	**9**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 0 Ohm
429OUTB_10	**10**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 10 Ohm
429OUTB_37	**11**	**429 OUTPUT.** ARINC 429 format serial digital data output B, 37 Ohm
V+	**12**	**POWER INPUT.** +9.5 to +16.5 VDC.
GND	**19**	**POWER INPUT.** Ground.
V-	**4**	**POWER INPUT.** –9.5 to –16.5 VDC
NC	**2, 3, 8, 13, 14 ,16, 20**	**No Internal Connect**

Table 2 Speed Control Function Table

HI/LO_n	OUTPUT TRANSITION TIME
0	10uS (12.5 KBS data)
1	1.5uS (100KBS data)

Table 3 Transmit Data Function Table

TS_CTL_n	TTLIN1_n	TTLIN0_n	429OUTA	429OUTB	NOTES
X	0	0	0V	0V	Null output
X	0	1	-5V	5V	Zero output
X	1	0	5V	-5V	One output
1	1	1	0V	0V	Null output
0	1	1	Hi -Z	Hi-Z	Tri-state Output

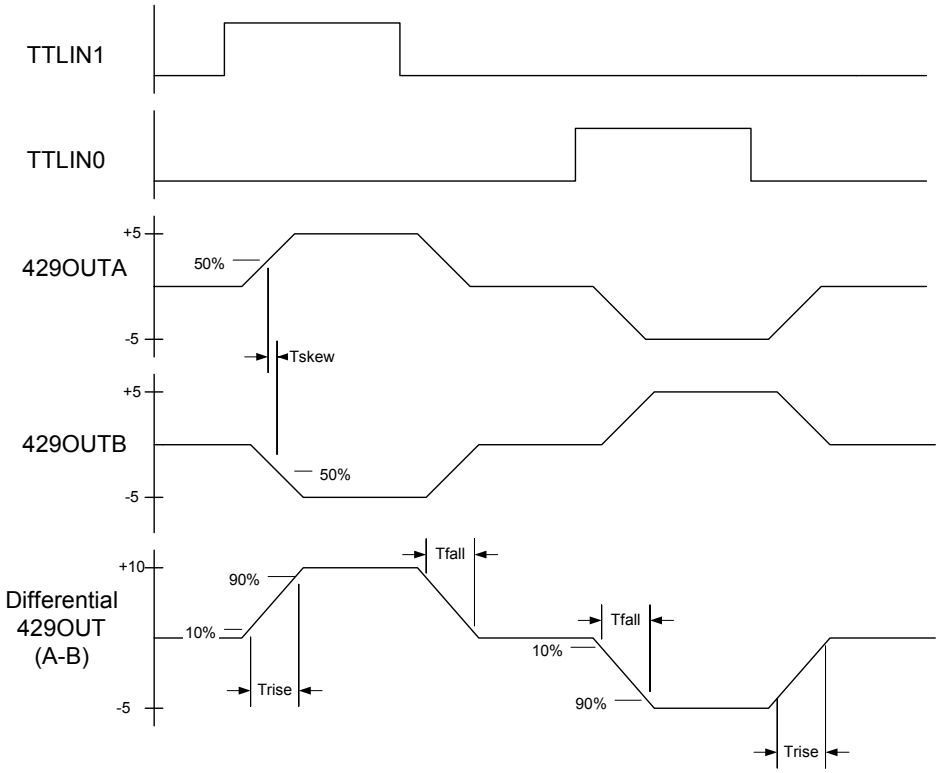


Figure 1 Timing Waveforms

ELECTRICAL DESCRIPTION

Table 4 Absolute Maximum Ratings

PARAMETER Voltages referenced to Ground	MIN	MAX	UNITS
V+ Supply Voltage	-0.3	+20	V
V- Supply Voltage	0.3	-20	V
V+, V- Supply Slew Rate		+/-100	V/uS
Storage Temperature	-65	+150	°C
Input Voltage TTLIN , HI/LO, and TS_CTL Inputs 429OUT Outputs	 Gnd – 0.3 'V-' – 0.3	 'V+' + 0.3 'V+' + 0.3	 V V
Power Dissipation @ 85 °C: (> 10 Sec) 20 Lead MLQ, thermal pad soldered to heat spreader land.		 TBD	 W
Junction Temperature: Tjmax, Plastic Packages (Limited by molding compound Tg)		 145	 °C
ESD per JEDEC A114-A Human Body Model		2000	V
Peak body Soldering Temperature (10 sec duration)		235	°C
Notes: 1. Stresses above absolute maximum ratings may cause permanent damage to the device. 2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.			

Table 5 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	9.5 to 16.5V -9.5 to –16.5V
Operating Temperature Plastic Package	 T_{OP}	 -55 to +85 °C

Table 6 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C. V+/- = +/-9.5 to +/-16.5V Unless otherwise noted.						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
LOGIC INPUTS						
Input Voltage, Logic 1		V_{IH}	2.0		V+	V
Input Voltage, Logic 0		V_{IL}	-0.3		0.8	V
Input Current, Logic 1	VIN = 5.0V	I_{IH}	0		100	uA
Input Current, Logic 0	VIN = 0.0V TS_CTL All Others	I_{IL}	0 0		-250 -100	uA uA
ARINC OUTPUTS						
ARINC Output Voltage (Differential) One Null Zero	Differential Output Voltage = 429OUTA – 429OUTB. No Load.	V_{DIF1} $V_{DIFnull}$ V_{DIF0}	9.0 -0.5 -9.0	10.0 0 -10.0	11.0 +0.5 -11.0	V V V
ARINC Output Voltage (Single Ended) Hi Null Lo	Referenced to Ground No Load.	Vo_{HI} $Vo_{null,}$ Vo_{LO}	4.5 -0.25 -5.5	5.0 0 -5.0	5.5 +0.25 -4.5	V V V
Output Tristate Current	-5V to +5V	Iz	-10		+10	uA
ARINC Output Short Circuit Current	Outputs shorted to Ground.	Isc_{LO} Isc_{H}		130 -130		mA mA
Output Resistance: 429OUT_37 429OUT_10 429OUT_0	Room Temperature	Rout		37.5 10 0		Ohms Ohms Ohms
Output Slew Rate Hi Speed	HI/LO = 1 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	1.0		2.0	uS
Output Slew Rate Lo Speed	HI/LO = 0 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	5		15	uS
Output skew time between A and B outputs.	HI/LO = 1 Measured at 50% voltage amplitude of both outputs.	Tskew			200	nS
SUPPLY CURRENT						
Quiescent Operating Supply Current, per channel. IV+ IV-	V+ =15V, V- = -15V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load	I_{V+} I_{V-}	- -14.0	6.0 -6.0	14.0 -	mA mA

DESIGN CONSIDERATIONS

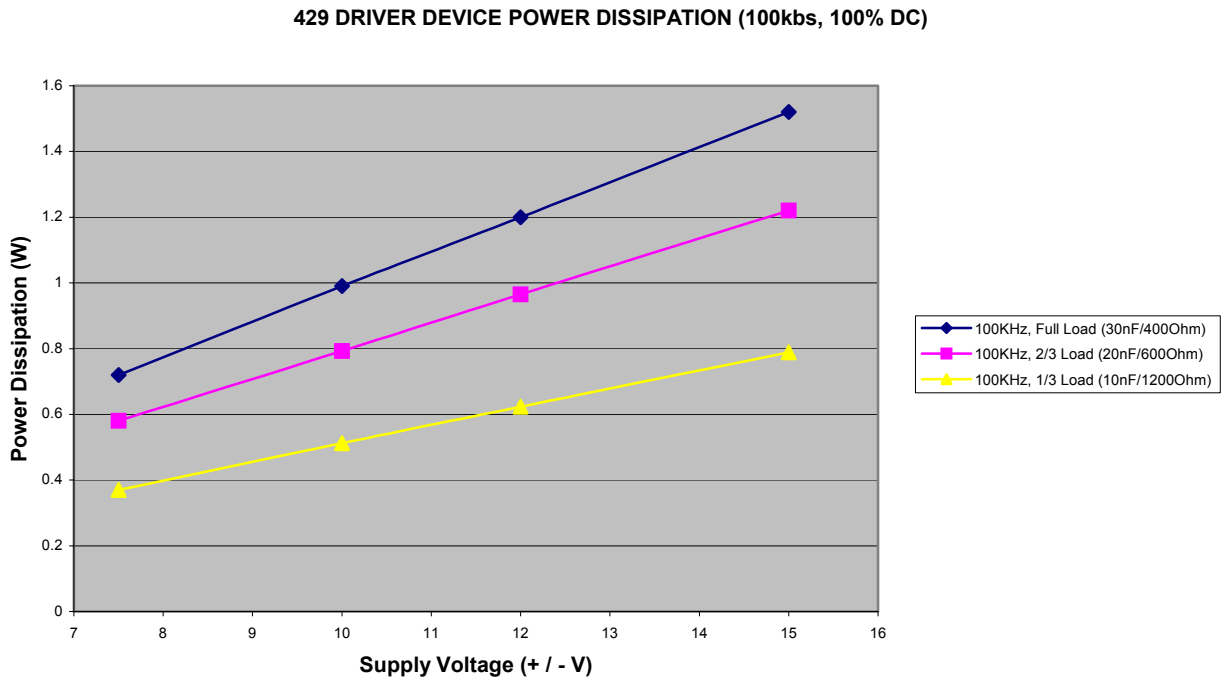
Transient Voltage Protection

External transient voltage suppressing devices are required to protect the device from stress such as that defined by DO160D Section 22, Lightning Induced Transient Susceptibility. The output stage of the driver includes intrinsic clamp diodes to the V+ and V- power rails. Consider using the 0 Ohm output option to allow use of an external 36 Ohm current limiting resistor and transient voltage suppressor. Transients at the device must be limited to less than one diode drop beyond the power rails to prevent excessive current to the device.

Thermal Management

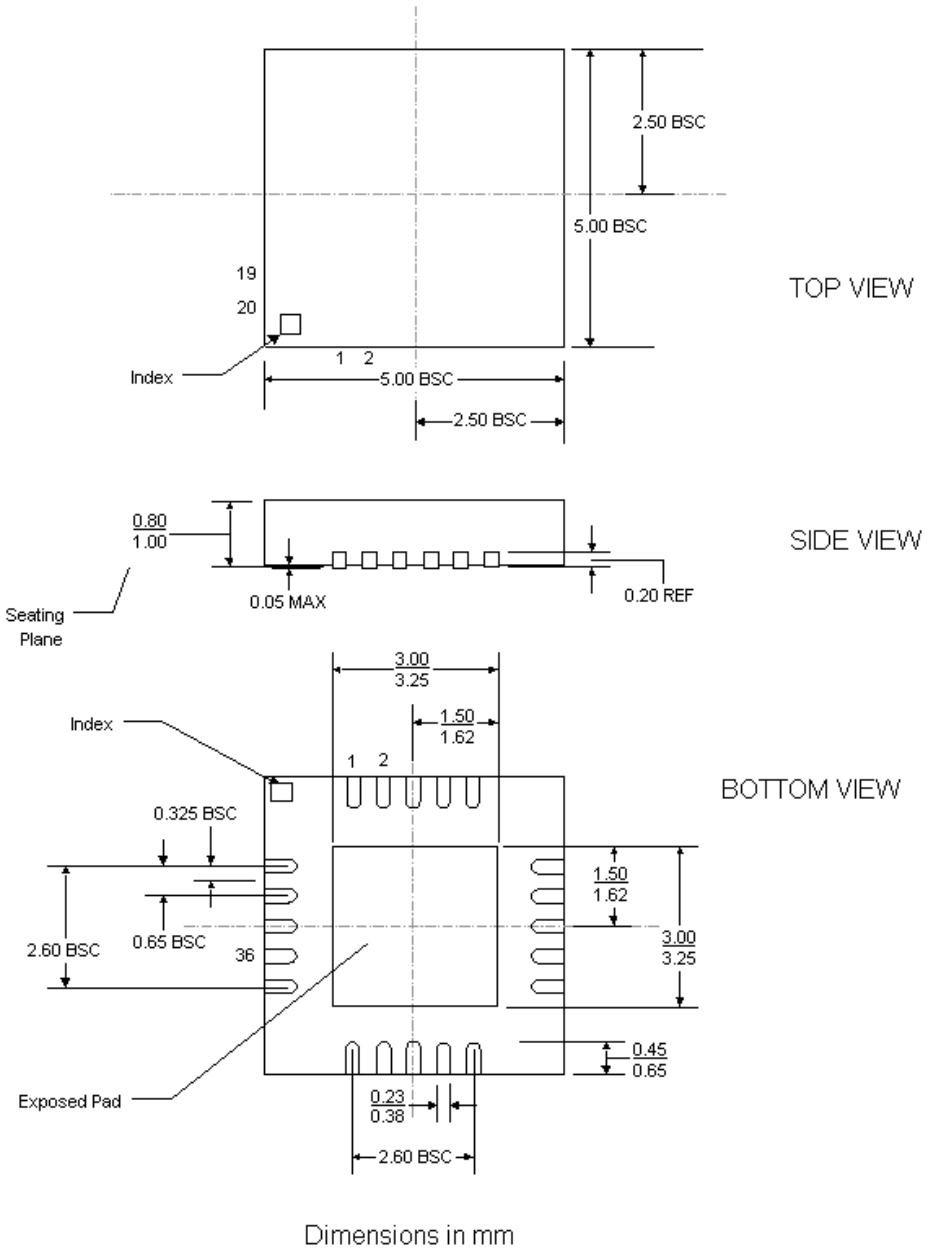
Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles. Dissipation may be estimated from the graph below which shows the approximate power dissipation for various loads and supply voltages. It is calculated for 100% data duty cycle at 100KBS with no word gap null times and must be reduced by the appropriate data duty cycle. Adjust for the application data duty cycle using a factor of (total bits transmitted in 10 sec period / 1,000,000) = (32 x total ARINC words transmitted in 10 sec period / 1,000,000).

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. The exposed heat sink pad of the MLP package should be soldered to a heat spreader land on the PCB. The DEI1171 pad is electrically isolated. The DEI1170 pad is internally connected to the V- supply voltage. Place vias on the signal/power traces close to the IC and on the heat spreader land to maximize heat flow to the internal power planes.



PACKAGE DESCRIPTIONS

20 Lead 5.0 x 5.0 MLP



Dimensions in mm

Table 7 20L MLP Characteristics

SYMBOL	DESCRIPTION	VALUE	UNITS
$Theta_{ja}$	Junction to Ambient. DEI1170 - Conductive pad DEI1171 - Isolated Pad 4 layer board with 2 internal power planes. Exposed pad soldered to .110" x .220" land with vias.	~34 ~40	°C/W
MSL	JEDEC Moisture Sensitivity Level Peak Body Temperature	2 235	- °C

ORDERING INFORMATION

Part Number	Marking	Package	Temperature
DEI1170-MES	DEI1170MES	20L MLP - conductive	-55 / +85 ºC
DEI1171-MES	DEI1171MES	20L MLP- isolated	-55 / +85 ºC