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DEI1038
ARINC 429 Line Driver Integrated Circuit

Features:

- ARINC 429 Line Driver for high speed (100KHz) and low speed (12.5KHz) data rates.
- Pin Compatible with HI-8383J including 13Ω output resistor.
- Low EMI RS-422 Line Driver mode for data rates up to 100 KHz.
- Adjustable Slew rates via external capacitors.
- Inputs TTL and CMOS Compatible.
- Low Quiescent Power of 125mW (typical)
- Programmable output differential range via V_{REF} pin.
- Outputs are not fused.
- Drives full ARINC load of 400Ω and 0.03µF.
- -55°C to +85°C operating temperature range.
- 100% Final testing.

Functional Description:

The ARINC 429 Line Driver Circuit is a bipolar monolithic IC designed to meet the requirements of several general aviation serial data bus standards. These include the differential bipolar RZ types such as ARINC 429, ARINC 571, and ARINC 575 as well as the differential NRZ types such as RS-422.

The DEI1038 operates in either a 429 mode or a 422 mode as controlled by the 429/422' pin. In 429 mode, the serial data is presented on DATA(A) and DATA(B) inputs in the dual rail format of the HS-3182. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5VDC along with V_1 to produce output levels of +5 volts, 0 volts, and –5 volts on each output for ±10 volts differential outputs.

In 422 mode, the serial data is presented on DATA(A) input. The driver is enabled by the SYNC and CLOCK inputs. The outputs swing between 0 volts and +5 volts if V_{REF} is at +5VDC.

The driver output resistance is 26 Ω ±20% at room temperature; 13 Ω on each output. The outputs are not fused. The output slew rate is controlled by external timing capacitors on CA and CB. Typical values are 75pF for 100KHz data and 500pF for 12.5KHz data.

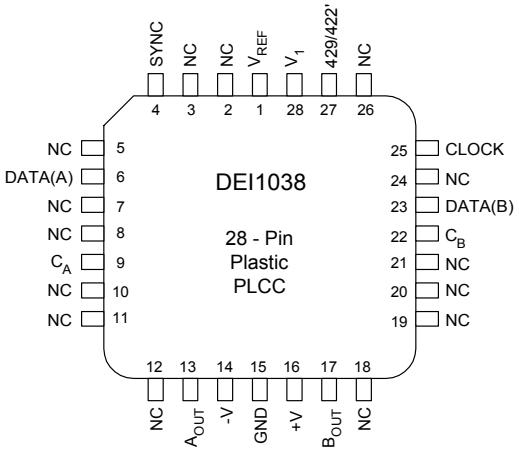


Figure 1: DEI1038 Pinout

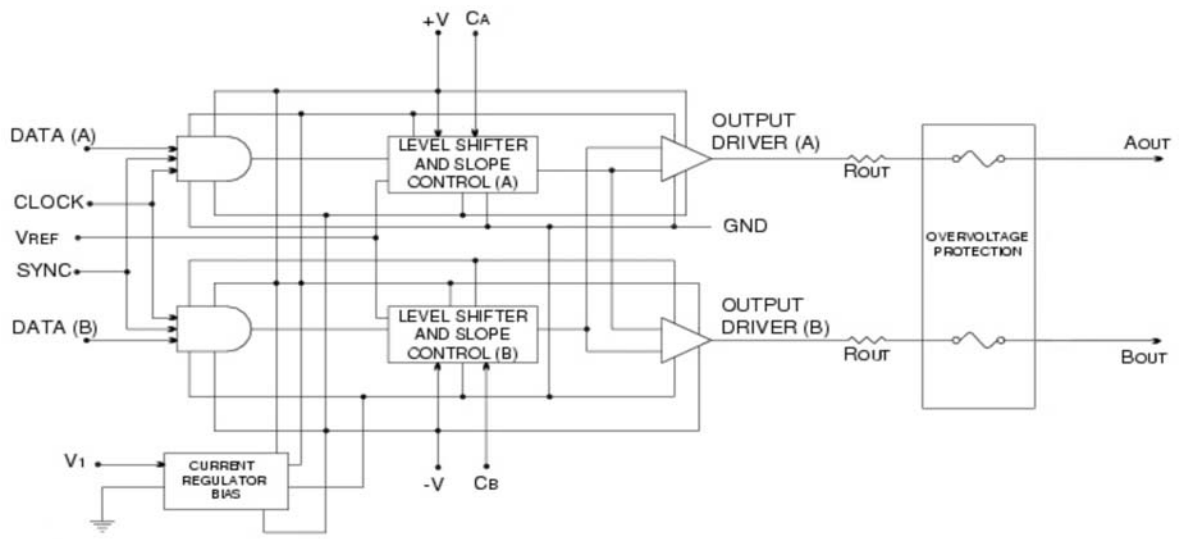


Figure 2: Block Diagram

Table 1: Pin Descriptions		
Pin #	**Pin Name**	**Description**
1	V_{REF}	Analog Input. The voltage on V_{REF} sets the output voltage levels on A_{OUT} and B_{OUT}. The output logic levels swing between $+V_{REF}$, 0 volts, and $-V_{REF}$ volts.
4	SYNC	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
25	CLOCK	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
6 23	DATA(A) DATA(B)	Logic inputs. These signals contain the Serial Data to be transmitted on the ARINC 429 data bus. Refer to Figure 3.
9 22	C_A C_B	Analog Nodes. External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typical $C_A = C_B = 75pF$ for 100 kHz data and $C_A = C_B = 500pF$ for 12.5 kHz data. *
13 17	A_{OUT} B_{OUT}	Outputs. These are the line driver outputs which are connected to the aircraft serial data bus.
14	-V	Negative Supply Input. –15VDC nominal.
15	GND	Ground.
16	+V	Positive Supply Input. +15VDC nominal.
27	429/422'	Logic Input. Mode control for ARINC 429 and RS-422 modes. An internal 10K W pull up resistor keeps the chip in ARINC 429 mode when there is no external connection. This creates a default logic 1, enabling the ARINC 429 mode. A forced logic 0 enables the RS-422 mode.
28	V_1	Logic Supply Input. +5VDC nominal.
2, 3, 5, 7, 8, 10	NC	No Connect
11, 12, 18,19	NC	No Connect
20, 21, 24,26	NC	No Connect

*C_A and C_B pin voltages swing between ±5 volts. Any electronic switching of the capacitor on the pins must not inhibit the full voltage swings.

Table 2: Logic Function								
	429/422' (1)	SYNC (2)	CLOCK (2)	DATA(A) (2)	DATA(B) (2)	A_{OUT}	B_{OUT}	COMMENTS
429 MODE	H	L	X	X	X	0	0	NULL
	H	X	L	X	X	0	0	NULL
	H	H	H	L	L	0	0	NULL
	H	H	H	H	H	0	0	NULL
	H	H	H	H	L	$+V_{REF}$	$-V_{REF}$	LOGIC 1
	H	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOGIC 0
422 MODE	L	L	X	X	X	$+V_{REF}$	0	NULL
	L	X	L	X	X	$+V_{REF}$	0	NULL
	L	H	H	L	X	0	$+V_{REF}$	LOGIC 0
	L	H	H	H	X	$+V_{REF}$	0	LOGIC 1

NOTES:

1. The 429/422' pin is internally pulled up to V_1 through a 10kΩ resistor. If no external connection is made to this pin, it will default to the 429 mode.
2. X = Don't care.

Table 3: Maximum Ratings			
PARAMETER	MIN	MAX	UNITS
VOLTAGE BETWEEN PINS:			
+V and GND	0	+40.0	V
–V and GND	0	-40.0	V
V_1 and GND	-0.3	+7.0	V
V_{REF} and GND	-0.3	+6.0	V
Logic Inputs	(GND-0.3)	(V_1+ 0.3)	V
Storage Temperature	-65	+150	°C
Peak Body Temperature, Non-G Package - G Package	-	 225 245	°C
Max Junction Temperature ($T_{J\ MAX1}$)Die Limit (short term operation)		+175	°C
Max Junction Temperature ($T_{J\ MAX2}$)Plastic Package Limit (prolonged operation)		+145	°C
Output Short Circuit Duration	See Note 1		
Output Over Voltage Protection	See Note 2		
Power Dissipation	See Table 5		

NOTES:

1. One output at a time can be shorted to ground indefinitely.
2. The outputs are not fused. External fusing must be provided to meet the Transmitter Fault Isolation of the ARINC 429 SPECIFICATION.

Table 4: Recommended Operating Range				
PARAMETER	MIN	TYP	MAX	UNITS
+V	+11.4		+16.5	VDC
-V	-11.4		-16.5	VDC
V_1	+4.5	+5.0	+5.5	VDC
V_{REF} (for ARINC 429)	+4.5	+5.0	+5.5	VDC
V_{REF} (for other applications)	+3.0		+6.0	V
Operating Temperature (T_A)	-55		+85	^oC

Table 5: Power Dissipation						
100% Duty Cycle Full Load = 400Ω/30,000pF Half Load = 4,000Ω/10,000pF						
DATA RATE	LOAD	+V = 15V	-V = -15V	V_1, V_{REF} = 5V	Pd POWER	LOAD POWER
0 to 100kbps	NONE	2.0mA	-5.0mA	4mA	125mW	0.0mW
12.5kbps	FULL	16.0mA	19.0mA	4mA	485mW	60.0mW
100kbps	FULL	48.0mA	51.0mA	4mA	1194mW	325.0mW
12.5kbps	HALF	6.0mA	8.0mW	4mA	196mW	30.0mW
100kbps	HALF	22.0mA	25.0mA	4mA	561mW	162.5mW

Thermal Management

Device power dissipation varies greatly as a function of data rate, load capacitance, data duty cycle, and supply voltage. Proper thermal management is important in designs operating at the HI speed data rate (100KBS) with high capacitive loads and high data duty cycles.

Power dissipation may be estimated from Table 5 "Power Dissipation Table". Device power dissipation (Pd) is indicated for 100% data duty cycle with no word gap null times and should be adjusted for the appropriate data duty cycle (DC). Pd(application) = DC * [Pd(table) - 145mW] + 145mW, where DC is the application data duty cycle, Pd(table) is the Pd from the table for the indicated data rate and bus load, and 145mW is the quiescent power. The application's data duty cycle (DC) for 100KBS operation is calculated as:

DC = (total bits transmitted in 10 sec period / 1,000,000) =
(32 x total ARINC words transmitted in 10 sec period / 1,000,000).

Heat transfer from the IC package should be maximized. Use maximum trace width on all power and signal connections at the IC. Place vias on the signal/power traces close to the IC to maximize heat flow to the internal power planes. If possible, design a solid heat spreader land under and beyond the IC to maximize heat flow from the device.

Table 6: DC Electrical Characteristics						
Conditions: Temperature: = -55°C to +85°C; +V = +11.4 to +16.5VDC, –V = -11.4 to –16.5VDC; V_1 = V_{REF} = +5VDC ±5%, 429/422' = Open Circuit (unless otherwise noted.)						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITIONS**
IQ+V	Quiescent +V supply current	-	2	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQ-V	Quiescent -V supply current	-	5	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_1	Quiescent V_1 supply current	-	4	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_{REF}	Quiescent V_{REF} supply current	-	10	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
V_{IH}	Logic 1 In. V	2.0	-	-	V	No Load.
V_{IL}	Logic 0 In. V	-	-	0.6	V	No Load.
I_{IH}	Logic 1 In. I	-	-	10	mA	No Load.
I_{IL}	Logic 0 In. I	-	-	-20	mA	No Load. (Pin 27 I_{IL} = -2mA max)
I_{OHSC}	Output Short Circuit Current (Output High)	-80	-	-	mA	Short to Ground
I_{OLSC}	Output Short Circuit Current (Output Low)	80	-	-	mA	Short to Ground
V_{OH}	Output Voltage HIGH. (+1)	V_{REF} - 250mV	V_{REF}	V_{REF} + 250mV	V	No Load. 429 Mode.
V_{NULL}	Output Voltage NULL. (0)	-250	-	+250	mV	No Load. 429 Mode.
V_{OL}	Output Voltage LOW. (-1)	$-V_{REF}$ – 250mV	$-V_{REF}$	$-V_{REF}$ + 250mV	V	No Load. 429 Mode.
I_{CT} + -	Timing Capacitor Charge Current C_A (+1) C_B (-1) C_A (-1) C_B (+1)	-	 +200 –200	-	 mA mA	No Load. 429 Mode. SYNC = CLOCK = HIGH C_A and C_B held at zero volts.
ISC (+V)	+V Short Circuit Supply Current	-	-	+150	mA	Output short to ground
ISC (-V)	-V Short Circuit Supply Current	-	-	-150	mA	Output short to ground
R_{OUT}	Resistance on each output	-	13	-	Ohms	Room Temp Only
C_{IN}	Input Capacitor	-	-	15	pF	-

AC ELECTRICAL CHARACTERISTICS

Figures 3 and 4 show the output waveforms for the ARINC 429 and RS-422 modes of operation.

The output slew rates are controlled by timing capacitors C_A and C_B. They are charged by ±200µA (nom.). Slew rate (SR) measured as V/µsec, is calculated by:

SR = 200/C
where C is in pF.

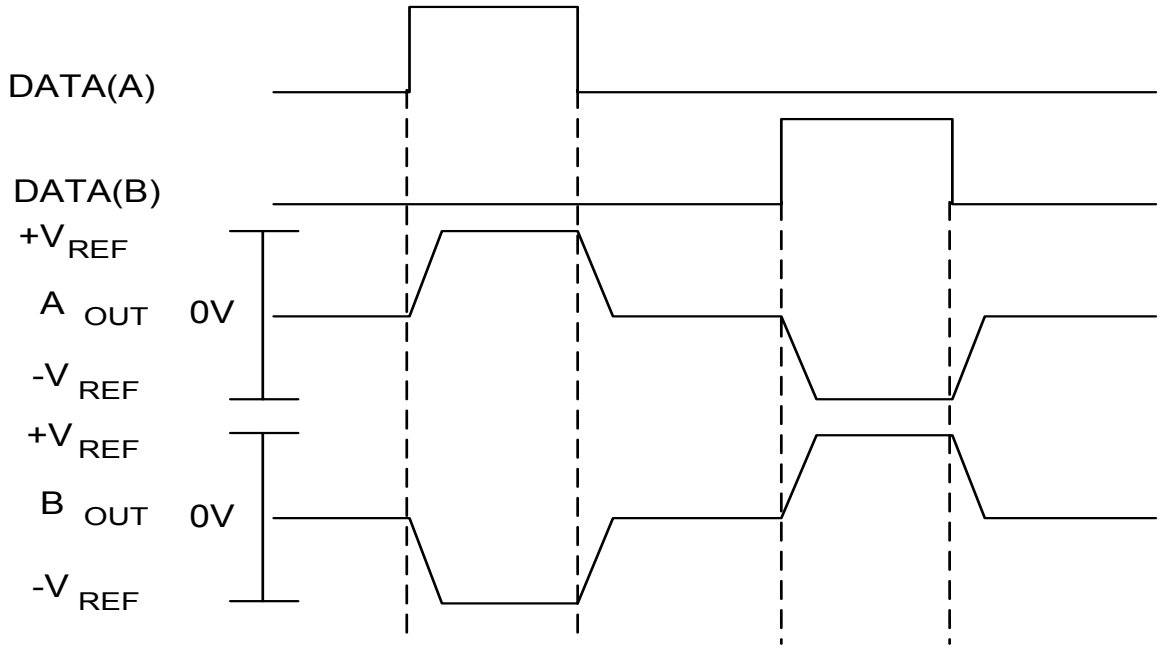


Figure 3: ARINC 429 Waveforms

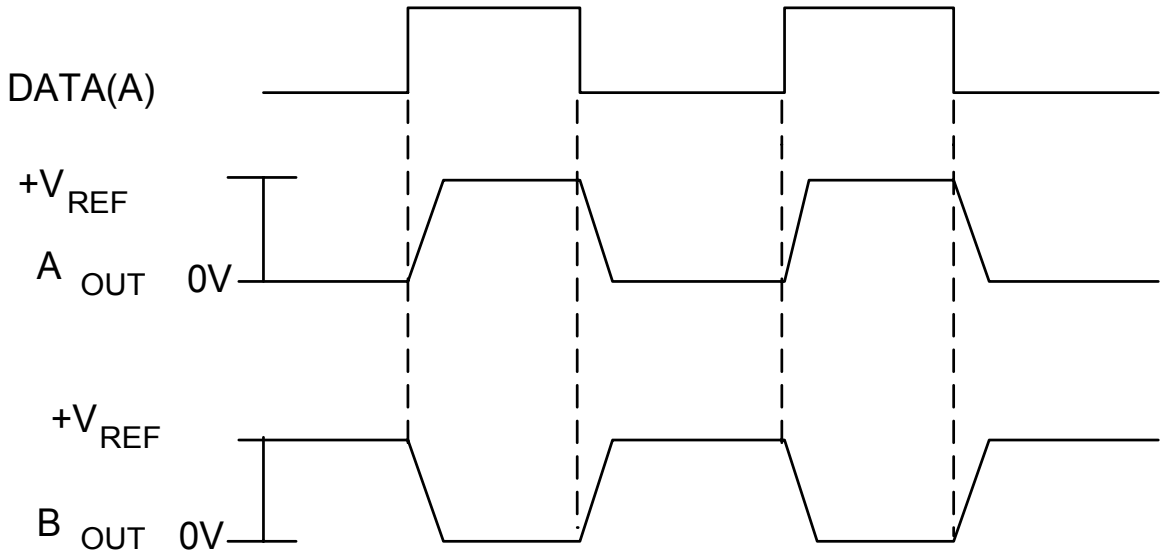
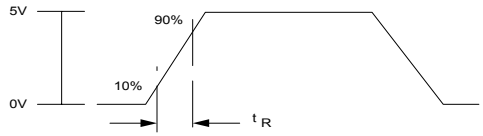
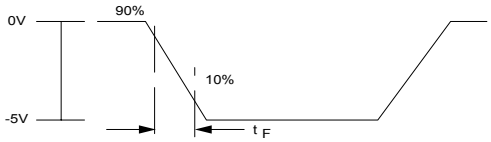


Figure 4: RS-422 Waveforms

Table 7: AC Electrical Characteristics					
Parameter	Symbol	MIN	MAX	UNITS	NOTES
Output Rise Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_R t_R	 1.0 5.0	 2.0 15.0	 µsec µsec	
Output Fall Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_F t_F	 1.0 5.0	 2.0 15.0	 µsec µsec	
Input to Output Propagation Delay	t_{PNH} t_{PNL}	-	3.0	µsec	See Figure 5
A_{OUT} / B_{OUT} Skew Spec.	-	-	500	nsec	

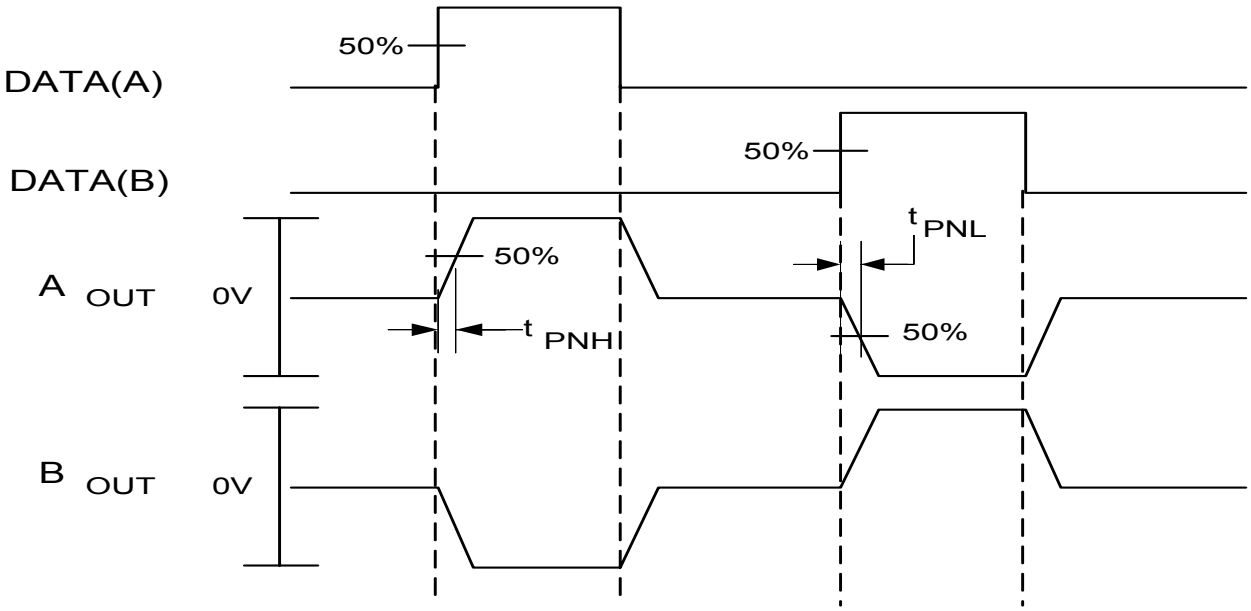


Figure 5: Propagation Delay

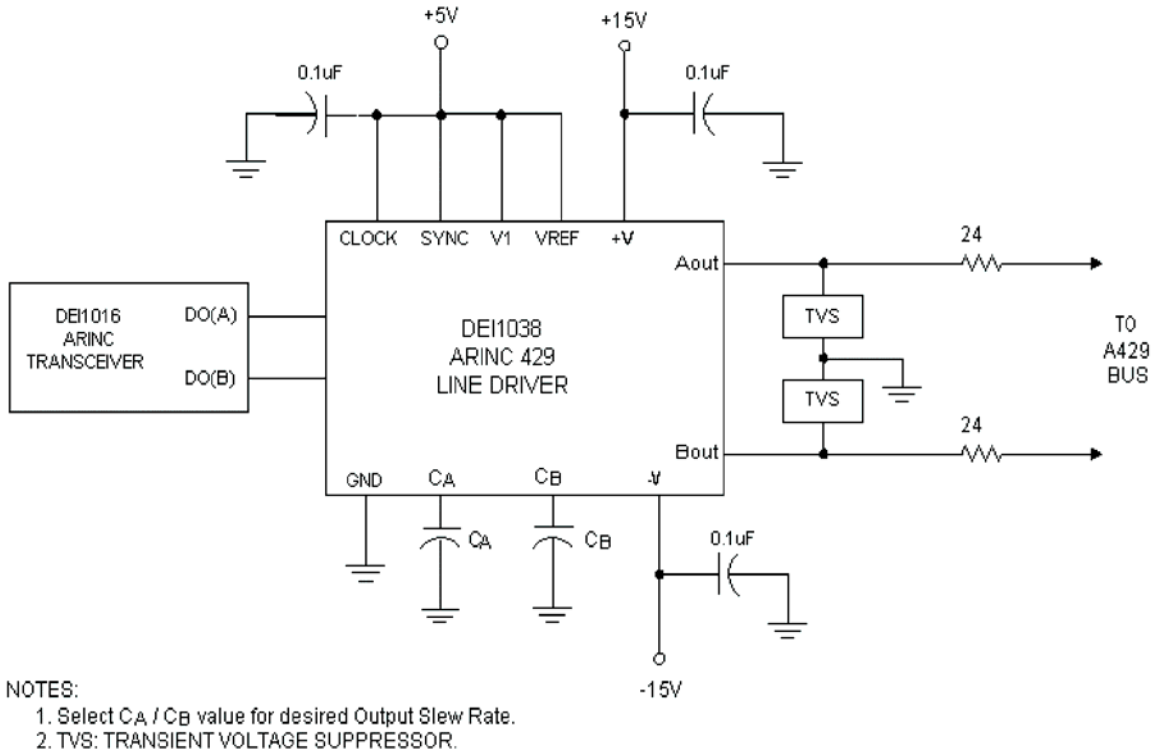


Figure 6: Typical Application

Component Screening:

Table 8: Screening Process	
SCREENING	**STANDARD PLASTIC**
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ +125 °C
LOW TEMPERATURE	0.65% AQL@-55°C

Ordering Information:

Table 9: Ordering Information				
DEI PART NUMBER	**MARKING (1)**	**PACKAGE**	**TEMPERATURE RANGE**	**SCREENING**
DEI1038	DEI1038	28 PLCC	-55 / +85 °C	STANDARD
DEI1038-G	DEI1038 E3	28 PLCC G	-55 / +85 °C	STANDARD

Notes:
1. All packages marked with Lot Code and Date Code. "E3" after Date Code denotes Pb Free category.

Package Description:

Table 10: Package Characteristics Table		
PACKAGE TYPE	**28L PLCC**	**28L PLCC, Green**
REFERENCE	28 PLCC	28 PLCC -G
THERMAL RESISTANCE: θ_{JA} (4 layer PCB with Power Planes) θ_{JC}	 55 °C/W 25 °C/W	 55 °C/W 25 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 3 / 225°C	MSL 3 / 245°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	SnPb	Matte Sn e3
Pb-Free DESIGNATION	Not Pb-free	RoHS Compliant
JEDEC REFERENCE	MS-018-AB	MS-018-AB

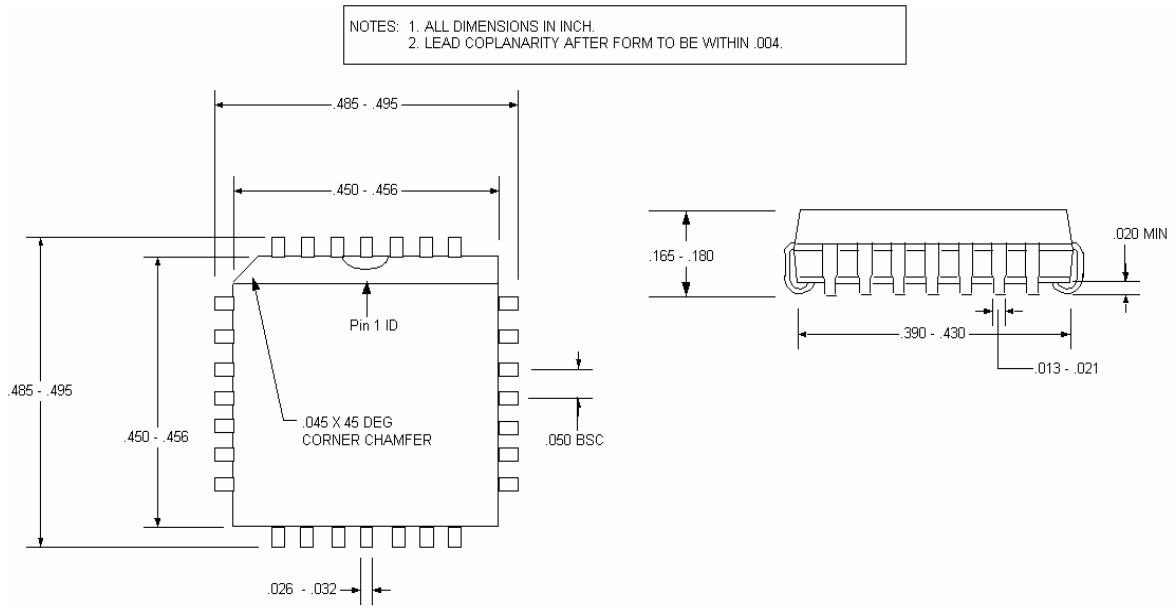


Figure 7: 28L PLCC Package Dimensions

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