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700 SERIES
20V BIPOLAR ARRAY FAMILY

FEATURES

- 20V bipolar analog array family of 9 base chips
- Metal mask customization to stock base wafers yields fast design turnaround
- Small chip size and enhanced complexity, due to advanced, small geometry process
- NPN current gain typically 200, f_T of 800MHz
- Large NPN with 200 mA of current handling capability
- PNP current gain between 40 and 90, f_T of 15MHz
- Wide selection of package options
- Design library for low cost tools: SIMetrix, PSPICE, and ICED
- "Kit parts" available for bread-boarding
- Design Manual with dozens of reference function circuits and tutorials
- Turn-key design and layout services available

DESCRIPTION

The 700 Series is a semi-custom 20V Bipolar analog and mixed-signal ASIC (Application Specific Integrated Circuit). Customers design their proprietary ASIC's using low-cost commercially available SPICE simulator, layout editor, and free design library. The design manual and library contain dozens of reference design function circuits including comparators, amplifiers, voltage references and regulators, logic gates, and timers.

DEI delivers fast turnaround by applying the customer designed metal interconnect pattern to a stock Series 700 wafer. Once the design is production ready, DEI provides production fabrication and test for timely deliveries of high-quality, fully-tested, proprietary Integrated Circuits.

Table 1: 700 Series Base Chip Summary

Chip Series	710	711	712	713	723	724	734	736	747
Pads	4	8	17	22	25	30	30	41	48
NPN/PNP Transistors	14	22	27	39	60	80	120	180	280
Schottky NPN Transistors	4	6	10	11	12	16	24	36	56
Large NPN Transistors	1	1	1	2	3	4	9	5	9
Large PNP Transistors	0	1	1	2	3	3	6	4	5
Total Transistors	33	52	66	93	143	183	279	405	630
750 Ohm Resistors	122	190	210	411	623	895	1268	1798	2487
Total Base Resistance (Ohms)	91k	142k	160k	310k	470k	675k	950k	1.35M	1.87M
Base Pinch Resistors	2	2	9	9	7	11	8	14	16
Epi Pinch Resistors	1	1	2	2	2	2	2	2	2
Junction Capacitors	1	2	2	4	7	7	9	12	10
Cross Unders	40	60	70	160	200	300	450	650	950

DS-MW-01700-01 Rev B
7/14/03

The 700 Series is based on a unique architecture and provides a uniform suite of components with which to implement your design. Each chip provides blocks of 12 transistors, 10 of which are convertible from NPN to PNP, and 2 Schottky NPN transistors positioned at the end of each block. These islands are surrounded by a field of resistors - the high quantity of resistors facilitating easy design.

Islands of transistors are arranged in columns and rows. The number of the chip defines the number of rows and columns; for example, the 712 contains a single column and 2 rows.

Between the bonding pads along the periphery are other devices: large (200mA) NPN transistors, large PNP transistors, pinch (high value) resistors, and junction capacitors. Cross under resistors are provided throughout the structure of the entire chip to ease routing.

There are nine chips in this series forming a smooth progression in size, each being approximately 30% larger in area. The specification of the chips in the 700 Series is shown below. Use this as a guide to determine which device is suitable for the application you have in mind. More information is available in the Design Manual at http://www.deiaz.com/700_series.htm.

Main Features of the 700 Series

- All devices use an advanced, small geometry (4 micron metal) process resulting in small chip size and enhanced complexity.
- Each of the small transistors can be either NPN or PNP. In the NPN mode the transistor has three separate emitters and two bases, allowing the simple creation of current ratios and multiple use of a single device. The same transistor can also be configured as a single or dual, lateral PNP transistor, ideal for current mirrors and pull up functions.
- The NPN device offers current gain of typically 200 and an f_T of 800MHz. Each of the three emitters can carry up to 8mA. The PNP lateral device has a gain between 40 and 90 and f_T of 15MHz. In the Periphery of the chip, the large NPN provides up to 200mA of drive current.
- Components such as resistors and small transistors have identical size and orientation providing optimum matching.
- The main resistor component on the chips is a single value, 750ohms base resistor. Connection in series and parallel of the many resistor sections on the array allows creation of almost any value between about 50ohms and 100kohms. Matching between any two resistors is 2%, with 1% matching when 10 or more are used for each value.

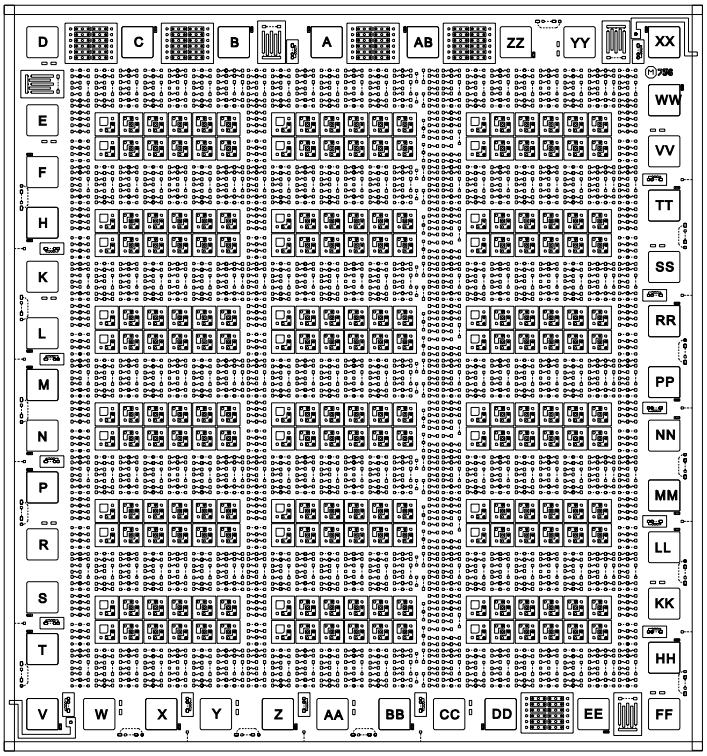


Figure 1: 736 Array

ELECTRICAL DESCRIPTION

Table 2: Absolute Maximum Ratings

PARAMETER Voltages referenced to Vee (Substrate)	MIN	MAX	UNITS
Vcc Supply Voltage	-0.3	+20	V
Operating Temperature Plastic Packages Ceramic Packages	 -55 -55	 +85 +125	°C
Storage Temperature Plastic Packages Ceramic Packages	 -65 -65	 +150 +150	°C
Junction Temperature: Tjmax		 +125	°C
ESD per JEDEC A114-A Human Body Model		2000	V
Lead Soldering Temperature (10 sec duration)		280	°C
Notes: Stresses above absolute maximum ratings may cause permanent damage to the device.			

Table 3: Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC $-V_{SUB}$	0.9 to 20V
Operating Temperature Plastic Ceramic	T_{OP}	 -55 to +85 ºC -55 to +125 ºC

Table 4: Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS 25ºC	MIN	MAX	UNIT
SMALL NPN TRANSISTORS					
BV_{CEO}	C-E breakdown voltage with base open	Ic = 10uA	20		V
h_{FE}	Common emitter current gain	Ib = 1uA Vce = 5V	100	350	-
V_{BE}	B-E diode voltage with collector connected to base	Ibe = 10uA		700	mV
I_{CEO}	C-E leakage current with base open	Vce = 20V		10	nA
BV_{EBO}	E-B breakdown voltage (Zener voltage)	Ieb = 10uA	5.6	6.1	V
RC	Resistance between the two collector contacts			200	Ω
SMALL PNP TRANSISTORS					
BV_{CEO}	C-E breakdown voltage with base open	Ic = 10uA	20		V
h_{FE}	Common emitter current gain	Ib = 1uA Vce = 5V	50	200	-
I_{CEO}	C-E leakage current with base open	Vce = 20V		10	nA
LARGE NPN TRANSISTORS					
BV_{CEO}	C-E breakdown voltage with base open	Ic = 10uA	20		V
h_{FE}	Common emitter current gain	Ib = 2mA Vce = 5V	40	150	-
I_{CEO}	C-E leakage current with base open	Vce = 20V		50	nA
LARGE PNP TRANSISTORS					
BV_{CEO}	C-E breakdown voltage with base open	Ic = 10uA	20		V
h_{FE}	Common emitter current gain	Ib = 100uA Vce = 5V	5		-
I_{CEO}	C-E leakage current with base open	Vce = 20V		20	nA
BASE RESISTORS					
R_{B1}	Base Resistor		600	900	Ω
$\Delta R_{B1} - R_{B2}$	Difference between two identical resistors, close together			tbd	%
SCHOTTKY DIODES					
V_F	Forward voltage drop	I = 10uA	300	400	mV
Ir	Reverse leakage current	Vr = 20V		50	nA
BASE PINCH RESISTORS					
I_{RBP}	Resistor current at forced 5V.	V_{Res} = 5V	10	150	uA
EPI PINCH RESISTORS					
I_{REP}	Resistor current at forced 20V.	V_{Res} = 20V	1	8	uA
METAL INTERCONNECT					
R_{MET}	Metal interconnect resistance	500 Squares		40	Ω
JUNCTION CAPACITORS					
BV_{JCAP}	Junction capacitor break down voltage	Icap = 10uA	9		V
Ir	Reverse leakage current	Vcap = 5V		50	nA

DESIGN TOOLS

Design Manual

The **700 Series Bipolar Array Design Manual** by Array Design Inc. is available for download at http://www.deiaz.com/. This presents a comprehensive survey of bipolar linear IC design and the specifics of designing with the 700 Series array. It is geared for the engineer contemplating his or her first IC design as well a thorough reference for the experienced Bipolar IC design engineer.

The manual covers the basics of the bipolar technology and the IC design process. It includes descriptions and analysis of dozens of circuit building blocks and reference function circuit designs. Finally, there are tutorials on how to load and use the design tools.

Circuit Design Tools

The 700 Series device model libraries, schematic symbol libraries, and dozens of function circuit blocks are available for download at http://www.deiaz.com/. These are available for two inexpensive, readily available CAE tools for schematic capture / SPICE circuit simulation. SIMetrix™ is the recommended tool and is available from Catena Software Ltd. at http://www.catena.uk.com/ or can be purchased through DEI directly. The industry standard P-SPICE™ is available from Cadence at http://www.pspice.com./.

Circuit Layout Tools

The 700 Series device layout patterns are available for download at http://www.deiaz.com/. These include the graphic templates for all array family members. These GDSII stream files can be used for design on any IC layout tool. Full support for LVS (Layout Vs Schematic) and DRC (Design Rule Check) is provided for the widely used and inexpensive ICED tool available from IC Editors, Inc. at http://www.ic-editors.com/ and can be purchased through DEI.

Bread Board Kit parts

Some designers prefer to breadboard their designs in addition to circuit simulation. This option is supported with a set of kit parts. These are the actual devices on the chips, wired up individually. All kit parts are in 18-pin dual in-line packages. Pin 9 is always the substrate and must be connected to the most negative potential in your circuit.

- 7KP1 contains six identical small NPN transistors with a single emitter connected.
- 7KP2 also contains six small NPN transistors. However, here the upper two transistors have three emitters, the middle ones two and the lower pair one emitter.
- 7KP3 has four small PNP transistors (with each collector brought out separately) and one epi-pinch resistor.
- 7KP4 provides two each of the large NPN and PNP transistors and one each of the small transistors. One of the large NPN transistors has its emitters available in two groups.
- 7KP7 contains six Schottky-clamped NPN transistors (with one of the emitters again permanently connected to the substrate).

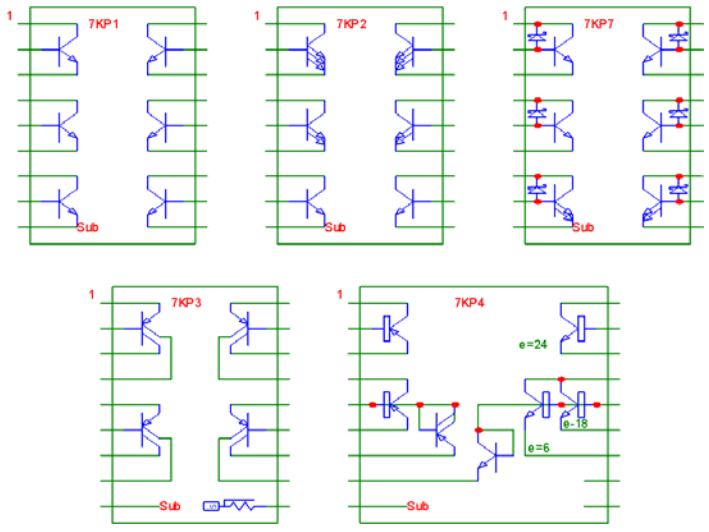
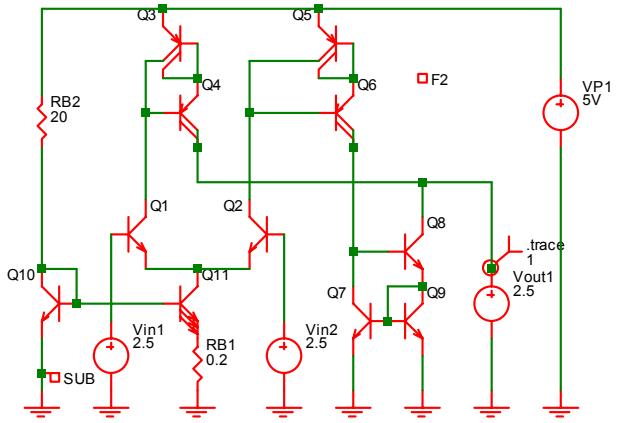


Figure 2: 700 Series Kit Parts

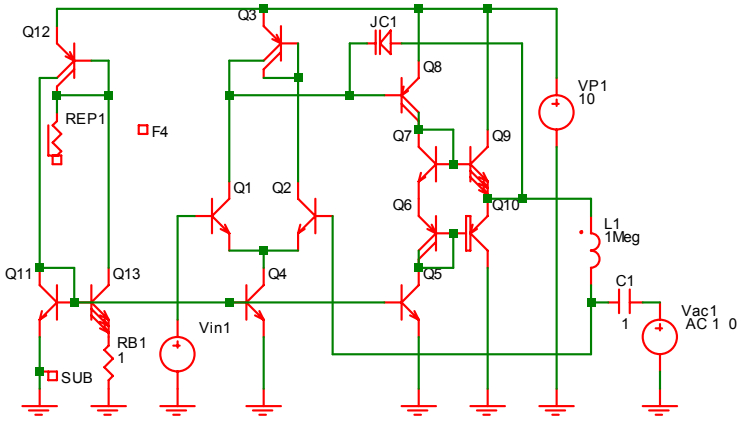
APPLICATION CIRCUITS

Here are just a few circuits which are thoroughly described in the 700 Series Design Manual and included in the CAE libraries. A listing of available circuits is also available at our website http://www.deiaz.com/700_series.htm under Circuit Examples and under Design Techniques.



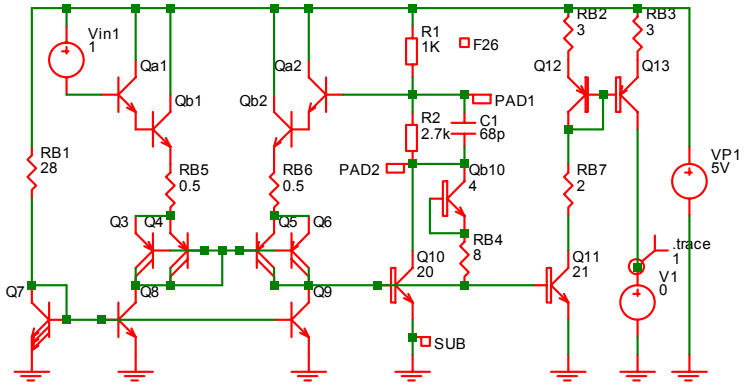
Frequency range is approx. 20MHz (there is some peaking at 9MHz). Change from -55C to 125C is -2dB and the three-sigma variation ±0.5dB. This is circuit F2 in the downloaded examples.

Figure 3: Transconductance Amplifier



Open loop gain is 88dB and ft 10MHz. This is circuit F4 in the downloaded examples.

Figure 4: Operational Amplifier

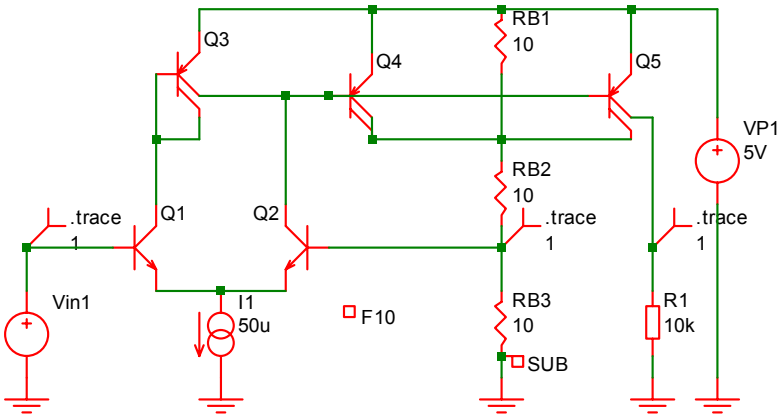


Emitter resistor values have been chosen for a maximum output current of 1mA (2.25 Volts nominal voltage drop). With a 5 Volt supply, the maximum input voltage is a little over 1 Volt. Response time is on the order of 150nsec.

(Circuit F26 was Contributed by Garry Brown, Rover Group, Coventry, UK)

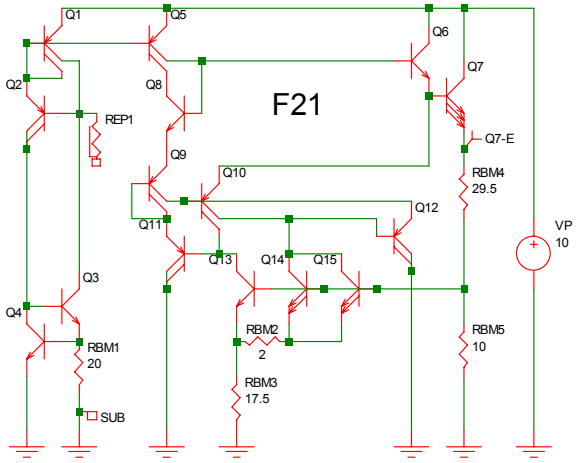
Figure 5: Voltage to Current Converter

APPLICATION CIRCUITS (CON'T)



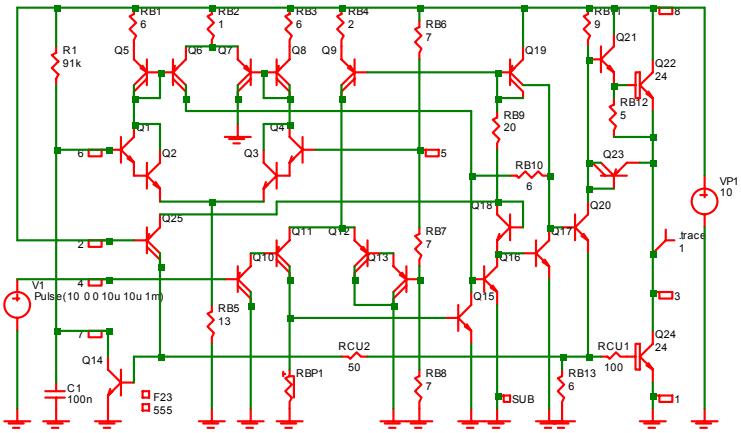
The switching points are:
Lower: VP x RB3 / (RB1 + RB2 + RB3)
Upper: VP x RB3 / (RB2 + RB3)

Figure 6: Schmitt Trigger



The divider string RB4/RB5 has been set here for 5 Volts, but you can set the ratio for any voltage from 3 to 18 Volts. Output impedance is 0.3 Ohms and the current limits at 90mA at -55C and 120mA at 125C. This is circuit F21 in the downloaded example files.

Figure 7: Voltage Regulator



The industry standard 555 timer is available to be implemented into an array. This timer consists of two comparators, a latch, and a discharge transistor. The first comparator is formed by Q1 through Q8 (note that Q1 and Q2, a darlington pair, can fit into the same island – the same can be done with Q3 and Q4). The second comparator is formed by Q10 through Q13. The discharge transistor is Q14, and the rest of the circuit makes up the flip flop and control logic. This is schematic F23 in the downloaded files.

Figure 8: 555 Timer

PACKAGE OPTIONS

Table 5: Standard Package Options (Contact factory for other options)

Pins	8	14	16	18	20	24	28	40	44	48
Plastic										
Dual In-Line (DIP), 300 mil	X	X	X	X	X	X				
Dual In-Line (DIP), 600 mil						X	X	X		X
Small Outline (SOIC), narrow body (150 mil)	X	X	X							
Small Outline (SOIC), wide body (300 mil)			X		X	X	X			
Plastic Leaded Chip Carrier (PLCC)							X		X	
Ceramic										
Dual In-Line, 300 mil	X		X							
Dual In-Line, 600 mil						X	X			

The 700 Series has been created and is maintained by Array Design Incorporated, San Francisco, CA 94110-5151.