DEVICE
ENGINEERING
INCORPORATED

385 East Alamo Drive
Chandler, AZ 85225
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1067
OCTAL GND/OPEN INPUT, SERIAL OUTPUT INTERFACE IC

FEATURES

- Eight GND/OPEN discrete inputs
  - Meet electrical requirements for ABD0100 and ARINC 735A GND/OPEN discrete inputs
  - Hysteresis provides noise immunity
  - Internal pull up resistor with 1mA source current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160D, Section 22, Cat A3 and B3.
- 3-wire serial interface (/CS, CLK, DO)
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10MHz Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3V or 5V
- Analog Supply Voltage (VDD): 15V +/-10%
- Pin compatible with DEI1066
- 16L NB SOIC package

PIN ASSIGNMENTS

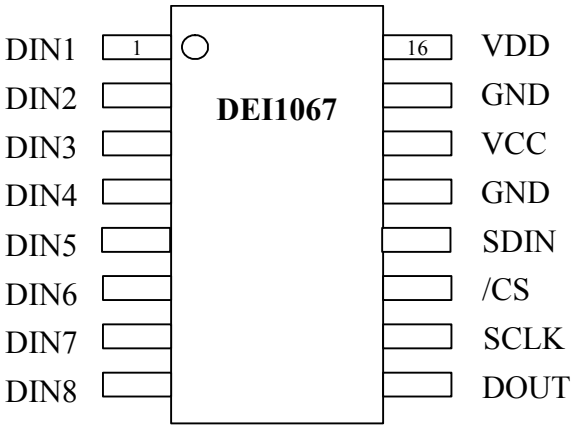

Figure 1 DEI1067 Pin Assignment (16 Lead NB SOIC)

DS-MW-01067-01 Rev. E
10/18/10

FUNCTIONAL DESCRIPTION

The DEI1067 is an eight-channel discrete-to digital interface BICMOS device. It senses eight Ground/Open discrete signals of the type commonly found in avionic systems. The data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

Table 1 Pin Descriptions

Pins	Name	Description
8-1	DIN[8:1]	Parallel data inputs. Eight Ground/Open format discrete signals. These have an internal pull-up to VDD. The logic threshold and hysteresis characteristics are determined by the applied VDD voltage.
9	DOUT	Serial data output. This pin is the output from the last stage of the shift register. This is a 3-state output.
10	SCLK	Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into the shift register and data in stage 8 is shifted out DOUT, being replaced by the data previously stored in stage 7.
11	/CS	Chip Select. A high-to-low transition on this input loads data from the parallel DIN[8:1] inputs into the shift register. A low level on this input enables the DOUT 3-state output and the shift register. A high level on this input forces DOUT to the high impedance state and disables the shift register so SCLK transitions have no effect.
12	SDIN	Serial Data Input. Data on this input is shifted into the shift register on the rising edge of the SCLK input if the /CS input is low. This input has an internal pull-down resistor to GND.
13	GND	Logic Ground.
14	VCC	Logic Supply Voltage.
15	GND	Analog Ground.
16	VDD	Analog Supply Voltage.

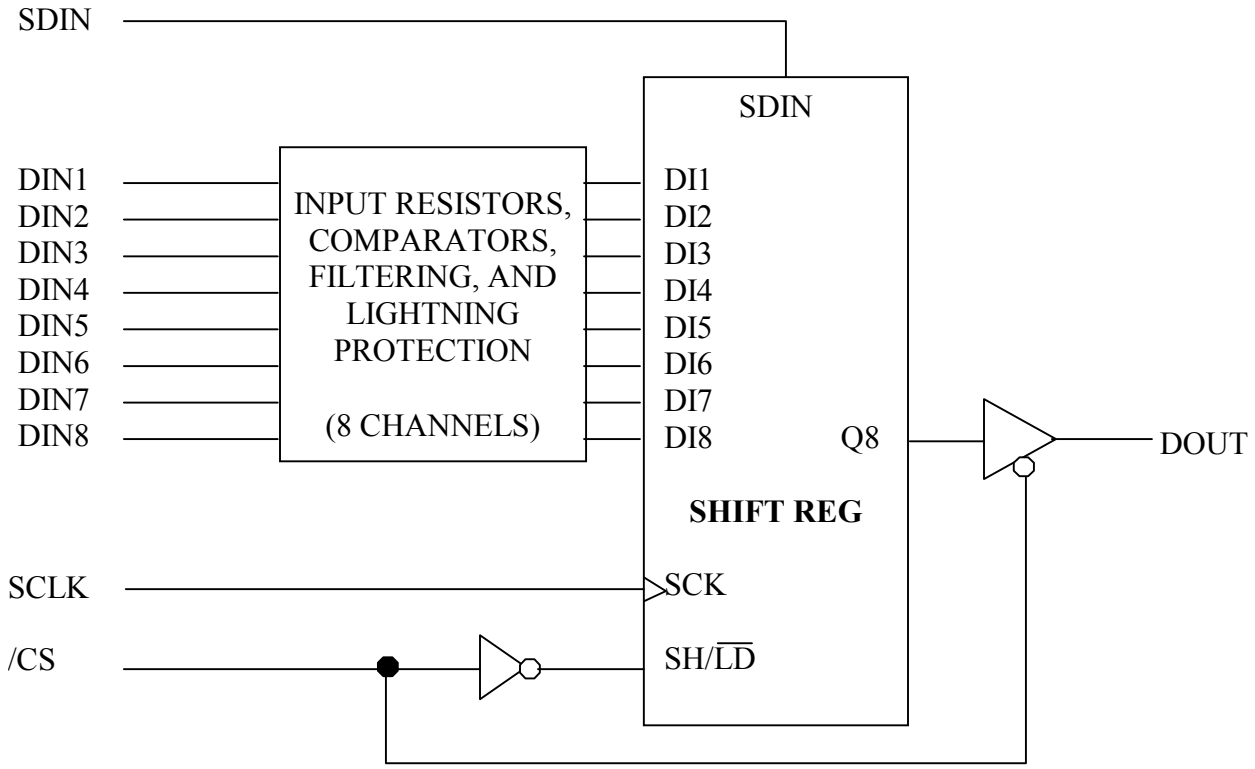

Figure 2 DEI1067 LOGIC DIAGRAM

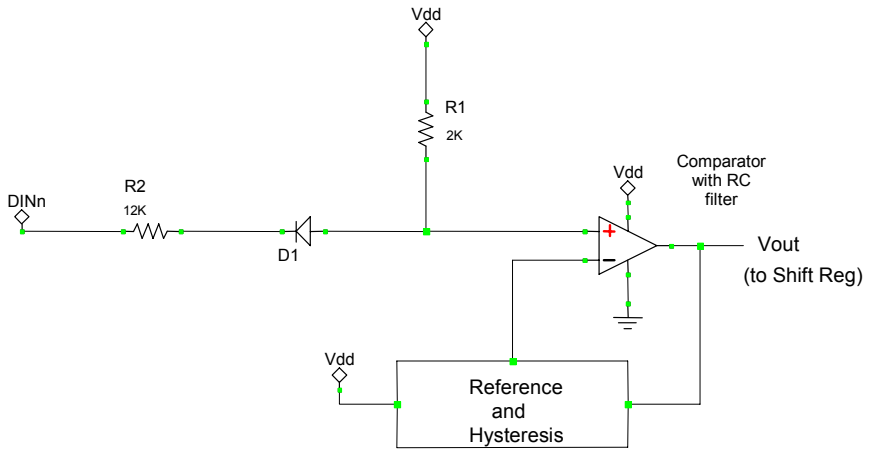

Figure 3 DINn Input Circuit

Table 2 Truth Table

/CS	SCLK	SDIN	DIN[8:1]	SREG Q1	DOUT
1	X	X	X	X	HI-Z
↓	X	X	Sampled into Shift Register	DIN1	Enabled DIN8
0	↑	0	X	0	SREG Q8
0	↑	1	X	1	SREG Q8
0	↓	X	X	No Change	No Change
↑	X	X	X	No Change	Disabled to HI-Z

DIN[8:1] Input Structure

Each of the eight discrete inputs consist of the circuit shown in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to the comparator IN+. The reference and hysteresis voltage is developed at the comparator IN-. Some notable features are:

- When Vdd is +15V, the circuit shall source ~1mA to a grounded input. This current will prevent a "dry" relay contact.
- The input threshold voltage and hysteresis with Vdd +/- 10%:
  - The falling Vth > 3.5V.
  - The rising Vth < 7.5V.
  - Hysteresis is maximum practical to meet the threshold requirements.
- The comparator includes an RC filter to provide noise rejection of transient pulses of up to several us. Thus there is a relatively large DINx setup time of several us (Refer to timing parameter tsu2).
- The inputs can withstand continuous input voltages of 40V minimum. The isolation diode breakdown voltage is greater than 50V. The 12K Ohm input resistor is designed to limit diode breakdown current to safe levels during transient events.

Serial Interface and Shift Register

The DEI1067 digital interface is an 8-Bit Serial or Parallel-Input / Serial-Output Shift Register with 3-State Output. The control inputs to the shift register are connected as shown in Figure 2 DEI1067 LOGIC DIAGRAM to implement an SPI compatible bus consisting of /CS, SCLK, DOUT, and SDIN. The Figure 5 waveform depicts a typical 8-Bit read cycle where the 8 DIN signals are read on to the serial bus. The Figure 6 waveform demonstrates a daisy-chain application where a 16-Bit read cycle includes the serial data passed through from the SDIN input.

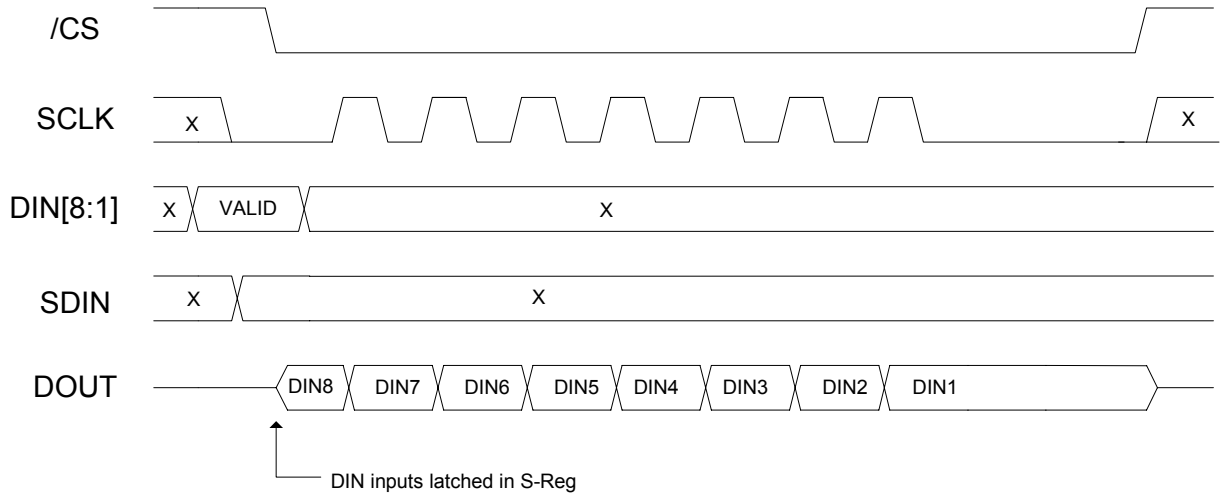

Figure 5 Serial Bus Read Cycle, 8 Bit

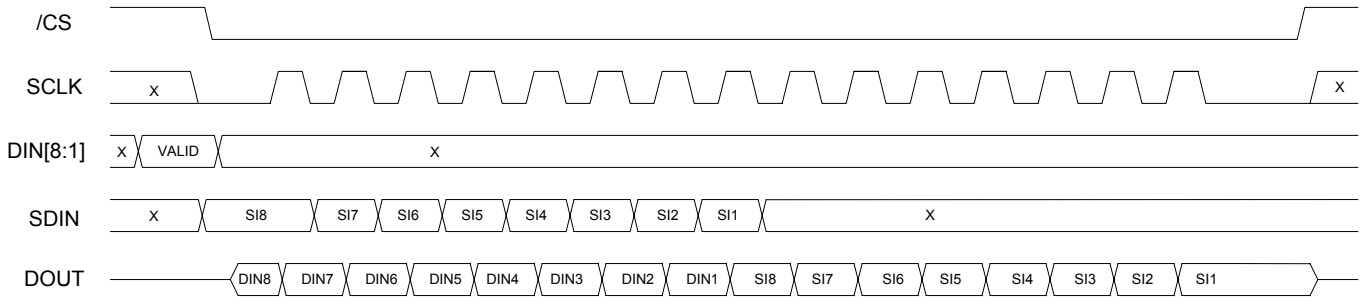

Figure 6 Serial Bus Read Cycle, 16 Bit Daisy Chain

Lightning Protection

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160D, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.

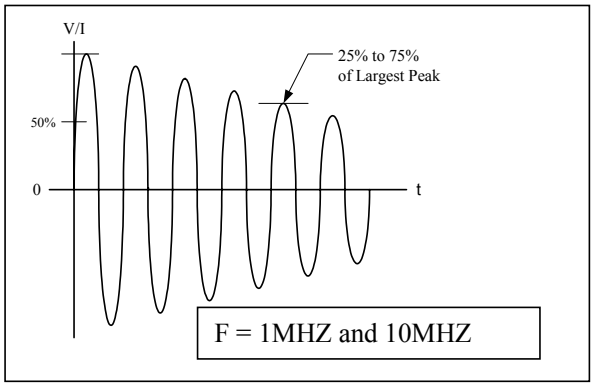

Figure 4 Voltage / Current Waveform 3

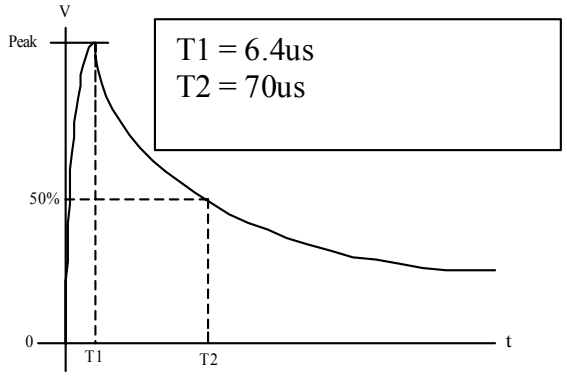

Figure 5 Voltage Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25 Ohms
- Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ohms
- Waveform 5A Voc / Isc = 300V / 300A => 1 Ohm

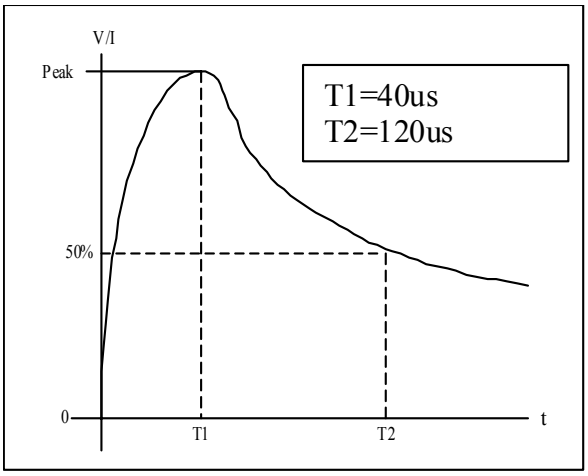

Figure 6 Current/Voltage Waveform 5A

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER Voltages referenced to Ground		MIN	MAX	UNITS
Vcc Supply Voltage		-0.3	+7.0	V
Vdd Supply Voltage		-0.3	20	V
Operating Temperature Plastic Package		-55	+85	°C
Storage Temperature Plastic Package		-65	+150	°C
Input Voltage DIN[8:1]	Continuous	-5	+40	V
	DO160D, Waveform 3, Level 3	-600	+600	V
	DO160D, Waveform 4 and 5, Level 3	-300	+300	V
Logic Inputs		-1.5	VCC + 1.5	V
DOUT		-0.5	VCC + 0.5	V
Power Dissipation @ 85 °C: (> 10 Sec) 16 Lead SOIC			0.8	W
Junction Temperature: Tjmax, Plastic Packages			145	°C
ESD per JEDEC A114-A Human Body Model Logic and Supply pins			2000	V
DIN pins			1000	
Peak Body Temperature (10 sec duration			260	°C

Notes:
Stresses above absolute maximum ratings may cause permanent damage to the device.

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	5.0V±10%, 3.3V±10% 15V±10%
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[8:1]	0 to 40V
Operating Temperature Plastic	Ta	-55 to +85 ºC

Table 5 DC Electrical Characteristics

Symbol	Parameter	Conditions (1)	LIMITS		Unit
			Min	Max	
LOGIC INPUTS AND OUTPUTS					
V_{IH}	HI level input voltage		2.0		V
V_{IL}	LO level input voltage			0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50		mV
V_{OH}	HI level output voltage	IOUT = -20uA	VCC – 0.1		V
		IOUT = -4.5mA, VCC = 4.5V to 5.5V	3.2		V
V_{OL}	LO level output voltage	IOUT = 20uA		0.1	V
		IOUT = 4.5mA, VCC = 4.5V to 5.5V		0.4	V
I_{IN}	Input leakage Logic inputs except SDIN. SDIN	Vin = Vcc or GND	 -1.0 -1.0	 1.0 750	uA
I_{OZ}	Max 3-state leakage current	Output in Hi Impedance state. VOUT = VIHmin, VILmax	-5.0	5.0	uA
DISCRETE INPUTS					
V_{IH}	HI level input voltage		7.5		V
R_{IH}	HI level Din-to-GND resistance	Resistor from Din to GND to guarantee HI input condition.	100K		Ohms
I_{IH}	HI level input current	Vin = 7.5V, VDD = 15V	-732	-212	uA
V_{IL}	LO level input voltage			3.5	V
R_{IL}	LO level Din-to-GND resistance	Resistor from Din to GND to guarantee LO input condition.		10	Ohms
I_{IL}	LO level input current	Vin = 0V, VDD = 15V	-1.55	-0.45	mA
V_{Ihst}	Min input hysteresis voltage		1.0		V
SUPPLY VOLTAGES					
ICC	Max quiescent logic supply current	Vin(logic) = Vcc or GND VIN[8:1] = open		200	uA
IDD	Max quiescent analog supply current	Vin(logic) = Vcc or GND VIN[8:1] = Open VIN[8:1] = GND		 11 24	mA

Notes:

1. Ta = -55 to +85 ºC. VDD = +15V±10%, VCC = 3.0 TO 5.5V unless otherwise noted.
2. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to Ground.
3. Guaranteed by design. Not production tested.

Table 6 AC Electrical Characteristics (4)

Symbol	Parameter	Conditions (6, 7)	Limits		Unit
			Min	Max	
f_{MAX}	SCLK frequency. (50% duty cycle) (5) Maximum usable SCLK frequency = 1/(tp2 + tsu3)	VCC = 3.0V VCC = 4.5V VCC = 3.0V VCC = 4.5V		4.8 24 2.8 10.7	MHz
t_W	SCLK pulse width. (50% duty cycle)	VCC = 3.0V VCC = 4.5V	100 20		ns
t_{su1}	Setup time, SCLK low to /CS↓.	VCC = 3.0V VCC = 4.5V	100 50		ns
t_{h1}	Hold time, /CS↓ to SCLK↑.	VCC = 3.0V VCC = 4.5V	20 20		ns
t_{su2}	Setup time, DIN valid to /CS↓.		1	35	us
t_{h2}	Hold time, /CS↓ to DIN not valid.		-1		us
t_{su3}	Setup time, SDIN valid to SCLK↑.	VCC = 3.0V VCC = 4.5V	75 20		ns
t_{h3}	Hold time, SCLK↑ to SDIN not valid.	VCC = 3.0V VCC = 4.5V	5 5		ns
t_{p1}	Propagation delay, /CS↓ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		250 70	ns
t_{p2}	Propagation delay, SCLK↑ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		250 100	ns
t_{p3}	Propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)	VCC = 3.0V VCC = 4.5V		200 80	ns
t_{p4}	Delay time between /CS active.	VCC = 3.0V VCC = 4.5V	25 25		ns
C_{in}	Maximum logic input pin Capacitance. (5)			10	pF
C_{out}	Maximum DOUT pin capacitance, output in HI-Z state. (5)			15	pF

Notes:

1. DOUT loaded with 50pF to GND.
2. DOUT loaded with 1K Ohms to GND for Hi output, 1K Ohms to VCC for Low output.
3. Timing measured at 25%VCC for “0” to Hi-Z, 75%VCC for “1” to Hi-Z.
4. Sample tested on lot basis.
5. Not tested
6. Ta = -55 to +85 ºC. VDD = +15V, VIL = 0V, VIH = VCC unless otherwise noted.
7. Measurements made at 50%VCC.

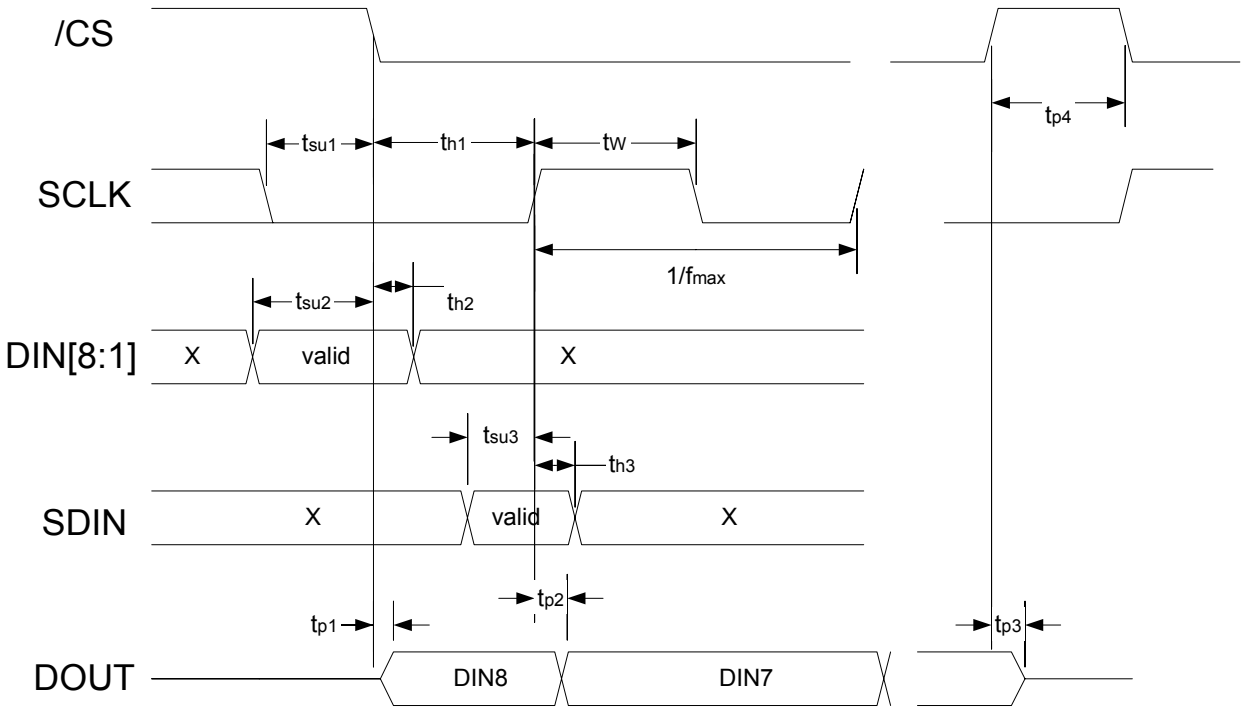

Figure 7 Switching Waveforms

PACKAGE DESCRIPTION

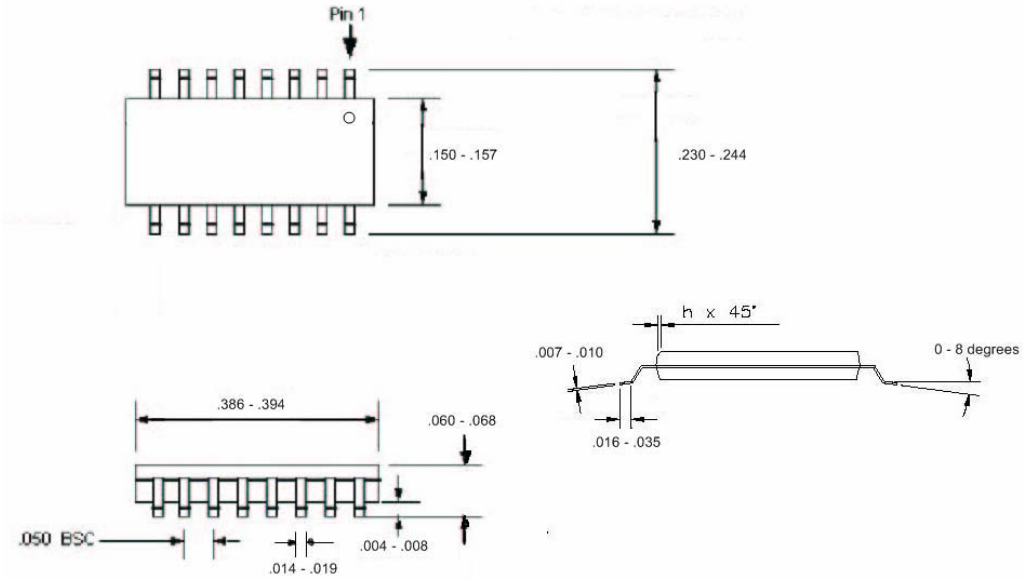

Figure 8: Mechanical Outline - 16L NB SOIC –G Package

Table 7 Package Information

	16 SOIC NB G
Moisture Sensitivity (per JEDEC J-STD-020C)	MSL 1 / 260˚C
Lead Finish	NiPdAu plate
RoHS Compliant Materials	Yes
Thermal Resistance: Θja: Θjc:	 74˚C/W (Mounted on 4 layer PCB) 30˚C/W

ORDERING INFORMATION

Table 8 - ORDERING INFORMATION

Part Number	Marking	Package	Burn In	Temperature
DEI1067-SES-G	DEI1067-SES E4	16 SOIC NB G	No	-55 / +85 ºC
Notes: 1. "E4" after date code denotes "Pb free" category				