Device
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DEI1044, DEI1045 QUAD ARINC 429 LINE RECEIVER

Features:

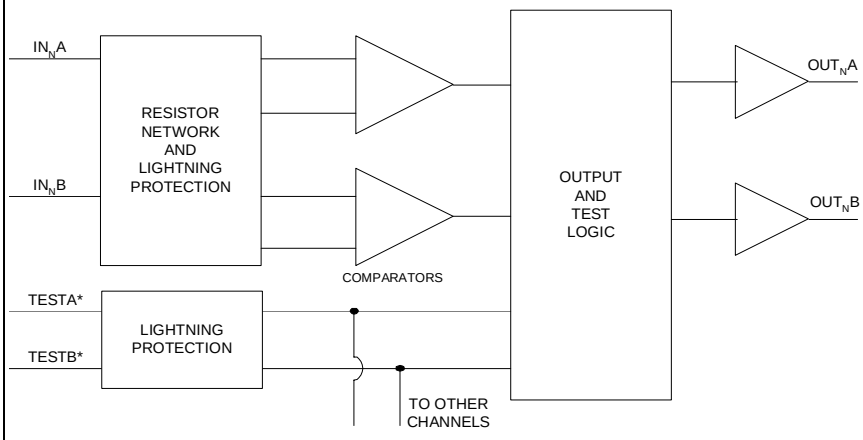
- Converts ARINC 429 levels to TTL/CMOS digital data.
- Meets requirements of ARINC 429 digital information transfer system standards.
- Inputs internally protected to Lightning requirements of DO-160D level A3.
- Operates at data rates beyond ARINC 429 specifications to 5MHz.
- 5 Volt or 3.3 Volt operation.
- 20L 4.4mm TSSOP Package.
- One-half volt receiver hysteresis.
- Operates within ±5 volts common mode input voltage range.
- BiCMOS process
- DEI1044 has TTL/CMOS test inputs

Functional Description:

The DEI1044 and DEI1045 are quad ARINC 429 Line Receiver ICs implemented in BICMOS technology. They contain four differential line receivers. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL/CMOS outputs. Each receiver operates independently, is lightning protected, and meets all requirements of the *ARINC 429 Digital Information Transfer Standard*.

The DEI1044 IC includes two TEST inputs for built in system test. They force the outputs of all receivers to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode. The DEI1045 does not have TEST inputs.

The DEI1044/1045 Quad Line Receiver can be used in conjunction with Device Engineering's family of avionics products in interfacing the ARINC 429 data bus.



Notes:
1) One of four identical channels shown (N = 1 to 4)
2) * TEST inputs are No Connect on DEI1045

Figure 1: Function Diagram

Table 1 Function Table

TEST A	TEST B	IN$_N$A - IN$_N$B	OUT$_N$ A	OUT$_N$ B
L	L	ONE +10V	H	L
L	L	ZERO -10V	L	H
L	L	NULL 0V	L	L
L	H	X	L	H
H	L	X	H	L
H	H	X	L	L

Test Inputs are internally set to L on DEI1045

DS-MW-01044-02 Rev. F
11/12/10

Pinout

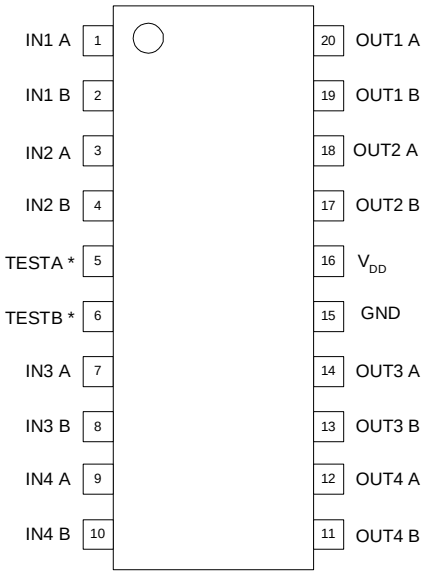


Figure 2: 20L TSSOP Pinout

Note: * Pins 5 and 6 are "No Connect" on DEI1045

Electrical Characteristics

Table 2: Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Supply Voltage (VDD)	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage (ARINC Inputs) DC conditions.	-30	+30	V
Input Voltage (Test Inputs)	V_{SS} – 0.3	V_{CC}+0.3	V
Power Dissipation @ 85 °C		350	mW
Peak Body Temperature, - G Package		260	°C
Lightning Protection (ARINC 429 Channel Inputs and TESTA/TESTB Inputs)			
Waveform 3 (2)	-600	+600	V
Waveform 4 and 5 (2)	-300	+300	V

NOTES:

1. Stresses above these limits can cause permanent damage.
2. Per DO160D, Sect 22 Level 3A. See Figures 7-9.
3. The DEI1044 contains circuitry to protect inputs against damage due to high voltage static discharge. It has been characterized per JEDEC A114-A Human Body Model to Level 1 (1KV io immunity). Observe precautions for handling and storing Electrostatic Sensitive Devices.

Table 3: Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VDD	+5V ± 10% +3.3V ± 10%
Logic Input Levels (DEI1044)	VTESTA,B	0 to Vcc
Operating Temperature -TMS	Top	-55 to +85°C -55 to +125°C

Table 4: Electrical Characteristics						
Conditions: Temperature: -55°C to +85°C (std versions), -55°C to +125°C (-TMS versions) V_{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
ARINC INPUTS						
$V_A - V_B$	OUT A = 1	V_{HI}	6.5	10	13	V
$V_A - V_B$	OUT B = 1	V_{LO}	-6.5	-10	-13	V
$V_A - V_B$	OUT A = 0 OUT B = 0	V_{NULL}	-2.5	0	2.5	V
Input Resistance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	R_{IN}	24k			Ω
Input Resistance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	R_S	12k			Ω
Input Hysteresis			0.5	1.0		V
Input Capacitance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_{IN}			50	pF
Input Capacitance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_S			50	pF
Input Common Mode Voltage	V_{HI}, V_{LO}, V_{NULL} at nominal values	V_{CM}	-5		+5	V
TEST INPUTS (DEI1044 only)						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8	I_{IL}			1	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}			20	µA
OUTPUTS						
OUT A or OUT B	I_{OH} = 5mA, V_{dd}= 5V I_{OH} = 1.5mA, V_{dd}= 3.3V	V_{OH}	2.4			V
OUT A or OUT B	I_{OL} = 5mA, V_{dd}= 5V I_{OL} = 1.5mA, V_{dd}= 3.3V	V_{OL}			0.4	V
OUT A or OUT B	I_{OH} = 100µA CMOS Compatible	V_{OH}	V_{DD} – 50mV			V
OUT A or OUT B	I_{OL} = 100µA CMOS Compatible	V_{OL}			V_{SS} + 50mV	V
SUPPLY CURRENT						
V_{DD} Current	A/B IN open, A/B OUT open	I_{DD}		5.5	11	mA
SWITCHING CHARACTERISTICS (1)						
			Max 3.3V		Max 5V	
Prop DelayIN A/B to OUT A/B	TESTA = TESTB = 0	t_{LH}	95		55	ns
Prop DelayIN A/B to OUT A/B	TESTA = TESTB = 0	t_{HL}	70		45	ns
OUT A/B rise time	10% to 90%	t_r	50		35	ns
OUT A/B fall time	10% to 90%	t_f	25		15	ns
TESTA/B to OUT A/B Prop delay		t_{TOH}	90		50	ns
TESTA/B to OUT A/B Prop delay		t_{TOL}	90		50	ns

Notes
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to Ground unless otherwise noted.

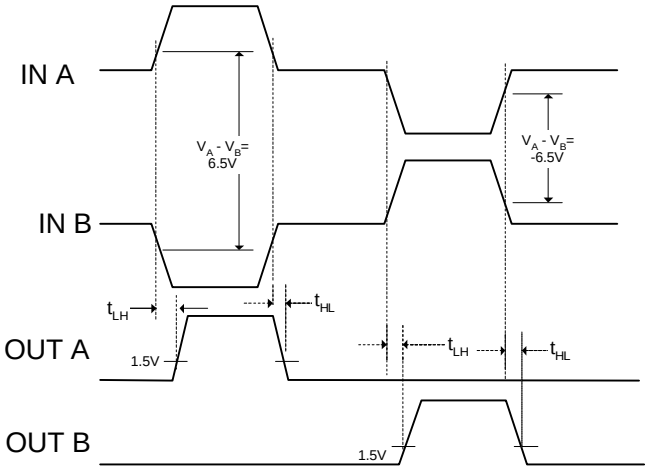


Figure 3: Input/Output Timing

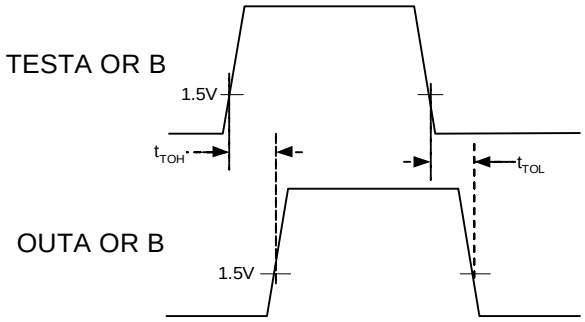


Figure 4: TEST Propagation Delay

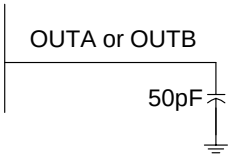


Figure 5: Output Load

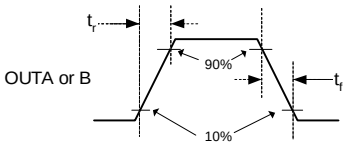


Figure 6: Rise/Fall Time

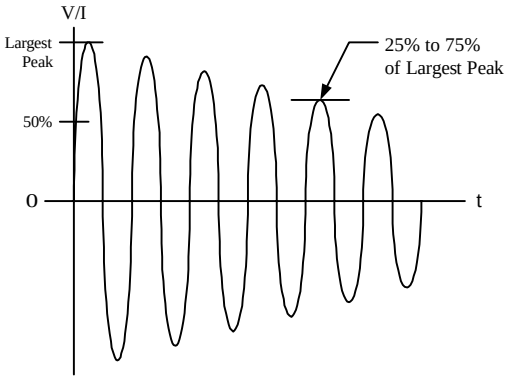


Figure 7: DO160C/D Voltage Waveform #3
V_{OC} = 600V, I_{SC} = 24A, Frequency = 1.0MHZ ±20%

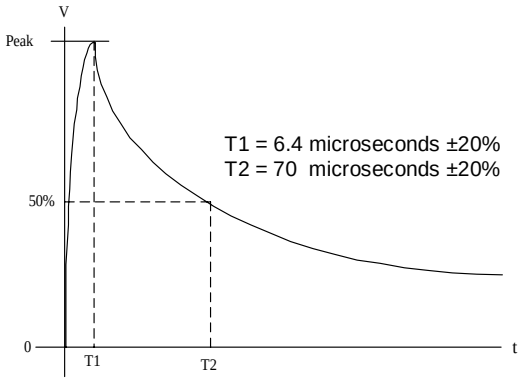


Figure 8: DO160C/D Voltage Waveform #4
V_{OC} = 300V, I_{SC} = 60A

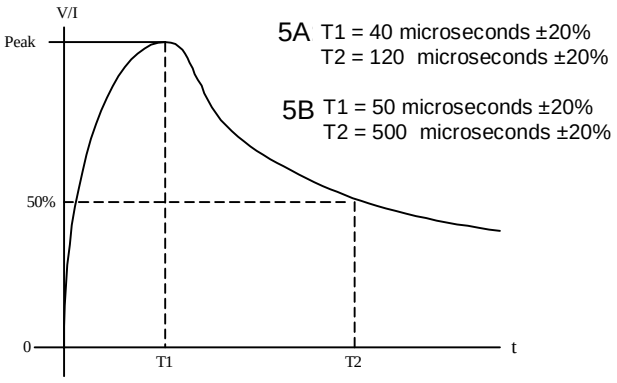


Figure 9: DO160C/D Voltage Waveform #5
V_{OC} = 300V, I_{SC} = 300A

Notes:

1. V_{OC} = Peak Open Circuit Voltage available at the calibration point.
2. I_{SC} = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of V_{OC} to I_{SC} is the generator source impedance to be used for generator calibration purposes.

Package Description:

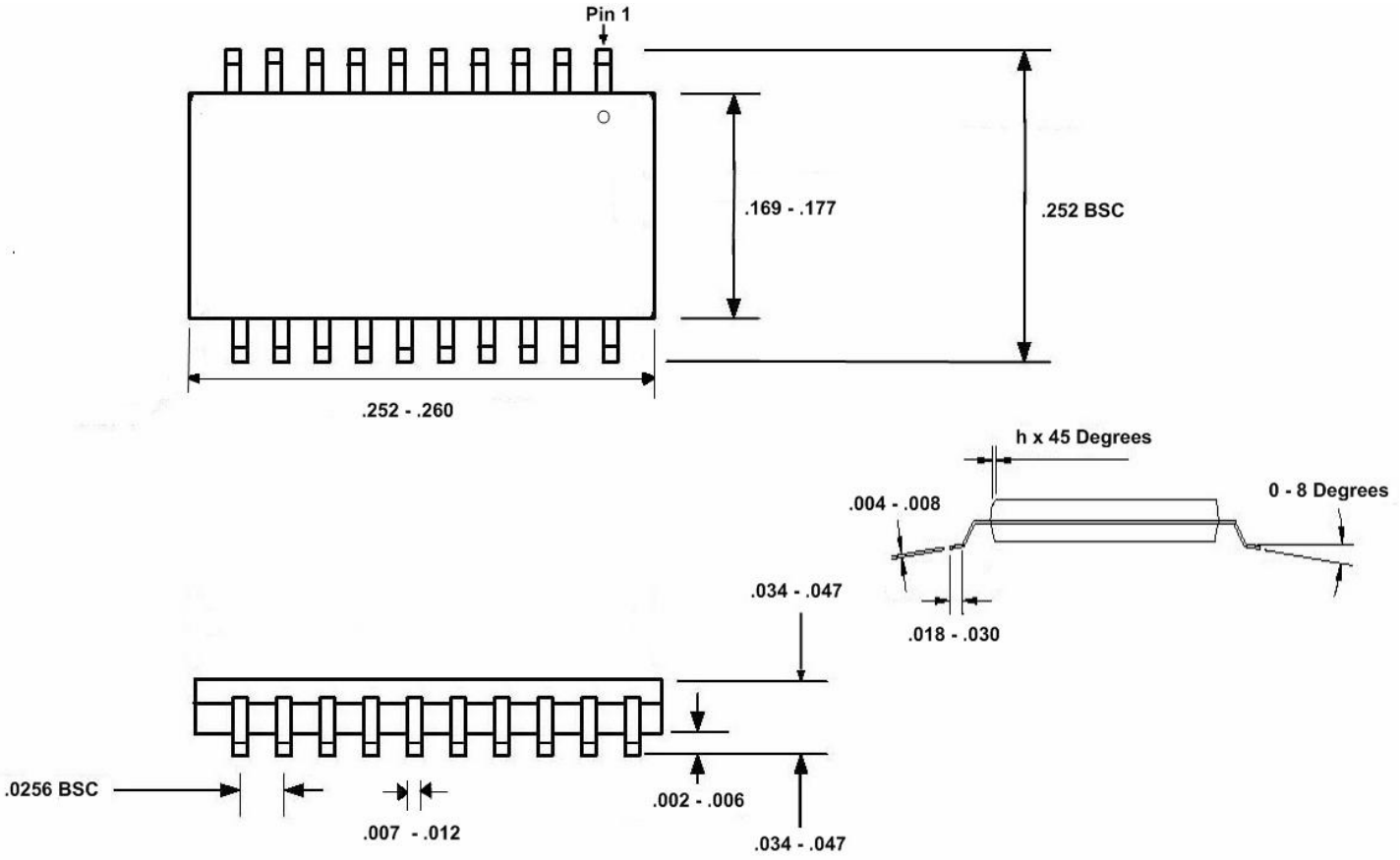


Figure 10: 20L TSSOP Package Dimensions

Table 5: Package Characteristics Table	
PACKAGE TYPE	**20L TSSOP, Green**
REFERENCE	20L TSSOP G
THERMAL RESISTANCE:	
θ_{JA} (4 layer PCB with Power Planes)	90 °C/W
θ_{JC}	17 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MO-153-AC

Table 6: Screening Process	
SCREENING	**METHODS**
ELECTRICAL TEST:	
ROOM TEMPERATURE	100%
HIGH TEMPERATURE	100% @ +85 or 125 °C
LOW TEMPERATURE	0.65% AQL@ -55°C

Table 7: Ordering Information

DEI PART NUMBER	MARKING (1)	PACKAGE	TEMPERATURE RANGE	TEST INPUTS
DEI1044-G	DEI1044 E4	20L TSSOP G	-55 / +85 °C	YES
DEI1044-TMS-G	DEI1044M E4	20L TSSOP G	-55 / +125 °C	YES
DEI1045-G	DEI1045 E4	20L TSSOP G	-55 / +85 °C	NO
DEI1045-TMS-G	DEI1045M E4	20L TSSOP G	-55 / +125 °C	NO

Notes:
1. All packages marked with Lot Code and Date Code. “E4” after Date Code denotes Pb Free category.