Device Engineering Incorporated

700 Series Bipolar Analog Arrays

- 20V Bipolar Analog Array
  - Can design to 40V or above with Cascoding
- Single Level Metal Customized
- 3-4 weeks to Ceramic Prototypes from Completion of Layout
- NRE Typically $20K to $60K.
- Standard OR Custom Packages.
- NPN Transistors:
  - Typical Beta = 200; f_T = 800MHz
- Large NPN Transistors (200 mA)

- PNP Transistors:
  - Beta = 40 to 90
  - f_T = 15MHz
- Turn-key Design and Layout Services Available
- See www.deiaz.com/700_series.htm

Chip Series	710	711	712	713	723	724	734	736	747
Pads	4	8	17	22	25	30	30	41	48
NPN/PNP	14	22	27	39	60	80	120	180	280
Schottky NPN	4	6	10	11	12	16	24	36	56
Large NPN	1	1	1	2	3	4	9	5	9
Large PNP	0	1	1	2	3	3	6	4	5
Total Transistors	33	52	66	93	143	183	279	405	630
750 Ohm Resistors	122	190	210	411	623	895	1268	1798	2487
Total Base Resistance (Ohms)	91k	142k	160k	310k	470k	675k	950k	1.35M	1.87M
Base Pinch Resistors	2	2	9	9	7	11	8	14	16
Epi Pinch Resistors	1	1	2	2	2	2	2	2	2
Junction Capacitors	1	2	2	4	7	7	9	12	10
Cross Unders	40	60	70	160	200	300	450	650	950

Design Tools:

- Free Design Libraries from website.
- SPICE libraries for SIMetrix™ (SIMetrix Technologies Ltd.) and PSPICE™ (Cadence).
- Layout Libraries for ICED™ from IC Editors Incorporated.
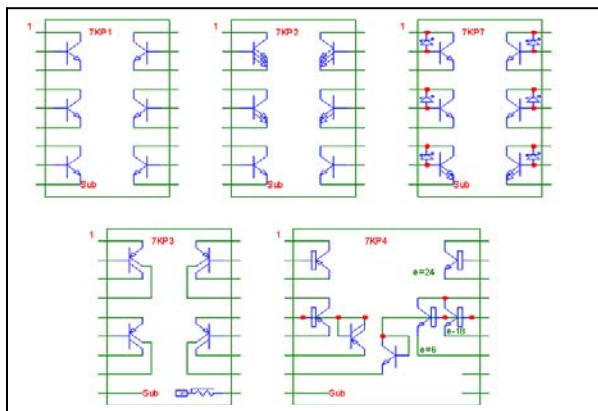
Bread Boarding:

- Breadboard your circuit using Kit Parts, available free from Device Engineering.
  - Array Devices in DIP Packages
  - Check breakdown voltages
  - 5 Kit Parts (shown at left):
    - 7KP1 => (6) NPN
    - 7KP2 => (6) Multi-emitter NPN
    - 7KP3 => (4) Dual Collector PNP
    - 7KP4 => Large NPN/PNP Mix
    - 7KP7 => (6) Schottky NPN

Device Engineering Incorporated, 385 East Alamo Drive, Chandler, AZ 85225
The 700 Series Arrays were Designed by Array Designs, Inc.   1of 2

BR-MW-10913-B
09/17/2010

Device Engineering Incorporated

700 Series Bipolar Analog Arrays

Quick Design:

- o Design Manual
  - o Example Circuits.
  - o Analog and Digital Gate Design Techniques.
  - o How Integrated Circuits are made.
- o Other Examples available – Contact Device Engineering.
- o Typical Design Cycle to Samples is 12 to 15 weeks (compared to 26 to 52 weeks for Full Custom).

555 Timer
(Circuit F23)

Transimpedance Amp
(Circuit F2)

Designers have the option to Breadboard a design using Kit parts, packaged NPN and PNP Array Transistors, to verify their design before it is committed to silicon in a 700 Series Array.

Incorporate your key intellectual property.

Device Engineering Incorporated, 385 East Alamo Drive, Chandler, AZ 85225
The 700 Series Arrays were Designed by Array Designs, Inc.   2of 2

BR-MW-10913-B
09/17/2010