Device
Engineering
Incorporated

385 East Alamo Drive
Chandler, AZ 85225
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1198
8CH GND/OPEN PARALLEL OUTPUT DISCRETE INTERFACE IC

FEATURES

- Eight discrete inputs
  - Senses GND/OPEN discrete signals.
  - Meets input threshold and hysteresis requirements specified per AirBus ABD0100H specification.
    - Thresholds: 4.5V/10.5V, Hysteresis: 3V
  - ~1mA DIN source/sink current to prevent dry relay contacts.
  - Internal isolation diode.
  - Uses an external 3KΩ resistor on the inputs to implement lightning transient immunity of 1600V and higher. i.e.: DO160E, Section 22, Levels 4 and 5.
  - Inputs protected from Lightning Induced Transients per DO160, Section 22, Cat A3 and B3 plus waveform 5A to 500V.
- Parallel I/O interface
  - TTL/CMOS compatible inputs and Tristate outputs
  - CLK & /OE control inputs and outputs
- Logic Supply Voltage (VCC): 3.3V +/-5%
- Analog Supply Voltage (VDD): 12.0V to 16.5V
- Package Options
  - 24 Lead TSSOP
  - 24 Lead TSSOP EP Thermally Enhanced
- Pin compatible with DEI1166/67

PIN ASSIGNMENTS

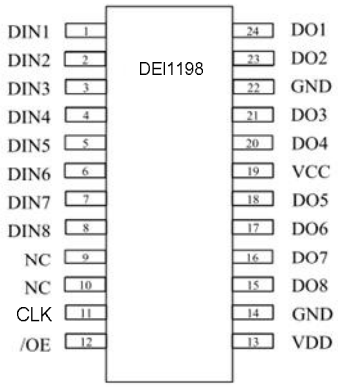


Figure 1 DEI1198 Pin Assignment (24 Lead TSSOP)

FUNCTIONAL DESCRIPTION

DEI1198 is an eight-channel parallel discrete-to-digital interface IC implemented in an HV DIMOS technology. It senses eight GND/OPEN discrete signals of the type commonly found in avionic systems and converts them to logic data. The discrete data is read from the device via a parallel tri-state bus.

The discrete input circuits are designed to achieve a high level of lightning transient immunity. The application design requires a series 3KΩ resistor on each discrete input to achieve DO160 Level 3 and WF5A 500V immunity. Higher immunity levels can be achieved (i.e. Level 5) with the addition of a TVS between the resistor and the input pin.

Table 1 Pin Description

PINS	NAME	DESCRIPTION
1-8	DIN[1:8]	Discrete Inputs. Eight GND/OPEN discrete input signals.
9-10	NC	Not Connected.
11	CLK	Latch Clock Logic Input A low level on this input enables transparent mode. A high level on this input enables latch mode.
12	/OE	Output Enable Logic Input. Low input when /CS is low will enable the tri-state outputs
13	VDD	Analog Supply Voltage. 12V to 16.5V
14	GND	Logic/Signal Ground
19	VCC	Logic Supply Voltage. 3.3V+/-5%
22	GND	Logic Ground
15-18,20-21,23-24	DO[1:8]	Logic Outputs. Eight tri-state data outputs

DIN[1:8] Discrete AFE

The Discrete Input Analog Front End circuit function is represented in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to a comparator with hysteresis. The external 3KΩ resistor is part of the front end circuitry for achieving threshold and hysteresis requirements while protecting the chip from Lightning Induced Transients.

Some notable features are:

- The DIN source/sink current is ~ 1mA. This current will prevent a “dry” relay contact.
- The input threshold voltage and hysteresis:
  - Low-to-high threshold voltage: 10.5V > Vth > 9V
  - High-to-low threshold voltage: 4.5V < Vth < 6V
  - Hysteresis: Vhys > 3V
- Input noise immunity is maximized with a combination of voltage hysteresis and use of a slow input voltage comparator
- The inputs can withstand continuous input voltages of 49V minimum. The isolation diode breakdown voltage is greater than 45V. The 10KΩ input resistance (consists of a 7KΩ On-Chip resistor and a 3KΩ Off-Chip resistor) is designed to limit diode breakdown current to safe levels during transient events.

Table 2 Truth Table

CLK	/OE	DIN[1:8]	LATCH[1:8]	DO[1:8]	Description
1	1	X	Hold	HiZ	Output = HiZ, Latch = Hold mode
1	X	Open	0	X	Latch[1:8] <= DIN [1:8]
		Ground	1		
1	0	X	Hold	Latch[1:8]	Output = Latched data
0	X	X	DIN[1:8]	X	Latch = Transparent mode
0	0	Ground	0	0	Output = Live data
		Open	1	1	
Legend: X = don’t care input or undefined output HiZ = Hi Impedance					

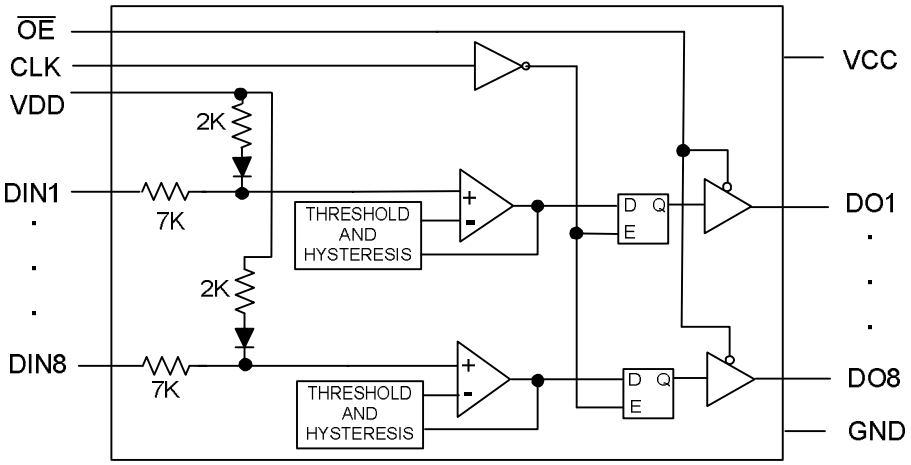


Figure 2 Function Block Diagram (two channels shown)

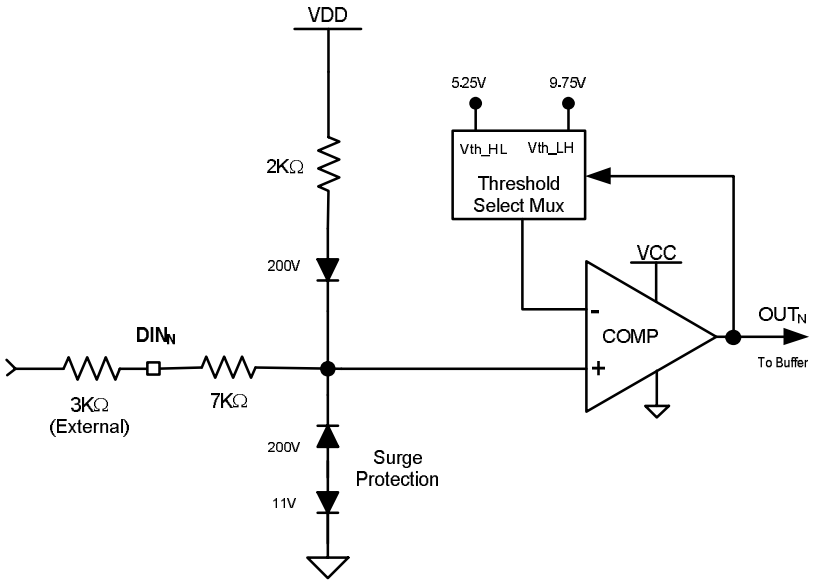


Figure 3 Analog Front End Detail

LIGHTNING PROTECTION

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A. They can withstand Level 3 stress (and WF5A up to 500V) with the external 3 KΩ series resistor for current limiting.

Protection for higher stress levels can be achieved (for example: the 3200V of WF3 Level 5) with the addition of transient voltage suppressor (TVS) devices at the DINn pins. First select the TVS clamp voltage < 450V (the intrinsic 1198 device capability). A convenient value would be 48V, which reduces the TVS capacitance to the lowest practicable level. The 3KΩ series resistor limits the TVS surge current, thus allowing small low power TVS devices.

For additional technical information on TVS selection, please refer to DEI's 'Transient Voltage Suppressor' Application Note on www.deiaz.com.

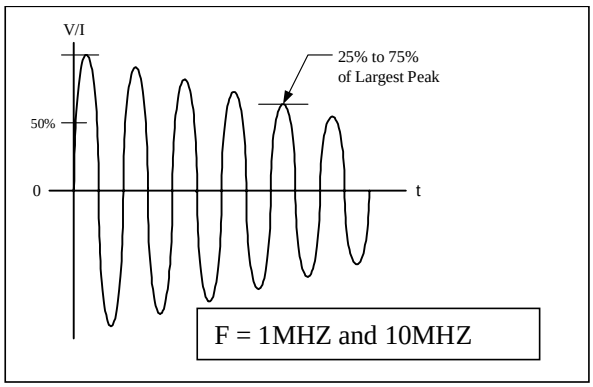


Figure 4 Voltage/Current Waveform 3

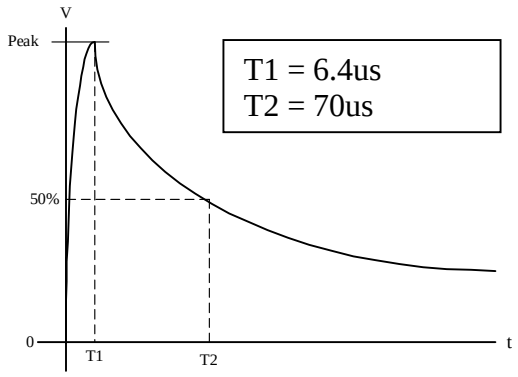


Figure 5: Voltage/Current Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25Ω
- Waveform 4 Voc/Isc = 300 V / 60 A => 5Ω
- Waveform 5A Voc / Isc = 300V / 300A => 1Ω
- Waveform 5A Voc / Isc = 500V / 500A => 1 Ω

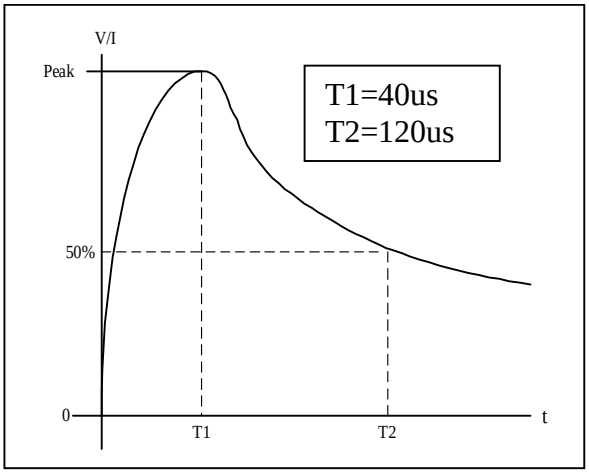


Figure 6 Voltage/Current Waveform 5A

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNITS
VCC Supply Voltage		-0.3	+5.0	V
VDD Supply Voltage		-0.3	18	V
Operating Temperature				
1198-TES-G		-55	+85	°C
1198-TMS-G		-55	+125	°C
Storage Temperature				
Plastic Package		-55	+150	°C
Input Voltage (3)(4)				
DIN[1:8]	Continuous	-10	+49	V
	DO160, Waveform 3, Level 3	-600	+600	V
	DO160, Waveform 4 and 5, Level 3	-300	+300	V
	DO160, Waveform 4 and 5	-500	+500	V
	DO160, Abnormal Surge Voltage, 100ms		80	V
Logic Inputs		-1.5	VCC + 1.5	V
DOUT		-0.5	VCC + 0.5	V
Power Dissipation @ 85 °C steady state 1198-TES-G			0.8	W
Power Dissipation @ 125 °C steady state 1198-TMS-G			0.8	W
Junction Temperature:				
Tjmax, Plastic Packages			145	°C
ESD per JEDEC A114 Human Body Model				
Logic and Supply pins			2000	V
DIN pins			1000	
Peak Body Temperature (10 sec duration)			260	°C

Notes:

1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. Voltages referenced to Ground
3. Stress applied to external 3 KΩ series resistor in series with DINn pin.
4. Discrete input voltage amplitude tolerance for WF3, 4 and 5 are +20%/-0%

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	3.3V±5% 12.0V to 16.5V
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[1:8]	0 to 49V
Operating Temperature 1198-TES-G 1198-TMS-G	Ta	 -55 to +85 ºC -55 to +125 ºC

Table 5 DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1)(2)	LIMITS			UNIT
			MIN	NOM	MAX	
Logic Inputs/Outputs						
$V1_{IH}$	HI level input voltage	VCC = 3.3V	2.0			V
$V1_{IL}$	LO level input voltage				0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50			mV
V_{OH}	HI level output voltage	I_DOUT = -20uA	VCC – 0.1			V
		I_DOUT = -4mA, VCC = 3V	2.4			V
V_{OL}	LO level output voltage	I_DOUT = 20uA			0.1	V
		I_DOUT = 4mA, VCC = 3V			0.4	V
I_{IN}	Input leakage	VIN = VCC or GND	-10		10	uA
I_{OZ}	3-state leakage current	Output in Hi Impedance state. DOUT = V_{IH}min, V_{IL}max	-10		10	uA
Discrete Inputs (4)						
$V2_{IH}$	HI level input voltage		10.5		49	V
VT_{LH}	Input Threshold Voltage, Low to High		9.0		10.5	V
R_{IH}	HI level DIN-to-GND resistance	Resistor from DIN to GND to guarantee HI input condition.	50K			Ω
I_{IH}	HI level input current	DIN = 28V, VDD = 15V DIN = 49V, VDD = 15V		1 1	240 2	uA mA
$V2_{IL}$	LO level input voltage		-4.0		4.5	V
VT_{HL}	Input Threshold Voltage, High to Low		4.5		6.0	V
R_{IL}	LO level DIN-to-GND resistance	Resistor from DIN to GND to guarantee LO input condition.			500	Ω
I_{IL}	LO level input current	DIN = 0V, VDD = 15V	-0.8	-1.3	-1.8	mA
V_{Ihst}	Input hysteresis voltage		3			V
Power Supply						
ICC	Max quiescent logic supply current	VIN(logic) = VCC or GND DIN[1:8]= open		1.8	3	mA
IDD	Max quiescent analog supply current	VIN(logic) = VCC or GND DIN[1:8]= Open DIN[1:8]= GND, All configured as Ground/Open		15 22	24 33	mA

Notes:

1. Ta = -55 to +85 ºC. VDD = 12.0 to 16.5V, VCC = 3.3V+/-5% unless otherwise noted
2. Current flowing into device is '+'. Current flowing out of device is '-'. Voltages are referenced to Ground
3. Guaranteed by design. Not production tested
4. With 3KΩ, 2% resistor in series with DIN input pin

Table 6 AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1,2)	LIMITS		UNIT
			Min	Max	
t_{HL} t_{LH}	Propagation delay, DIN to to DO. (3)	CLK = /OE=0		550	ns
t_{HZ} t_{LZ}	Output disable delay, /OE↑ to DO HI-Z from DO Low or High (4)(5)			50	ns
t_{ZH} t_{ZL}	Output Enable delay, /OE↑ to DO HI-Z from DO Low or High (4)(5)			50	ns
t_{SU}	DIN setup time, DIN to CLK↑ (6)		550		ns
t_H	DIN hold time, DIN to CLK↑ (6)			10	ns
C_{in}	Logic input pin Capacitance. (7)			10	pf
C_{out}	DOUT pin capacitance, output in HI-Z state. (7)			15	pf

Notes:
1. DOUT loaded with 50pF to GND.
2. Ta = -55 to +85ºC. VDD = 12V, VCC = 3V. VIL = 0V, VIH = VCC unless otherwise noted.
3. Timing measured from DO = 1.5V to V_{DIN} = 9V(Rising Edge)/4.5V (Falling Edge). See Figure 7.
4. DOUT loaded with 1KΩ to GND for Hi output, 1K Ohms to VCC for Low output.
5. Timing measured from /OE=1.5V to DO=200mV. See Figure 7.
6. Timing measured from CLK = 1.5V to V_{DIN} = 9V(Rising Edge)/4.5V (Falling Edge). See Figure 7.
7. Not production tested. Guaranteed by design.
8. AC characteristics are sample tested on lot basis.

TIMING DIAGRAMS

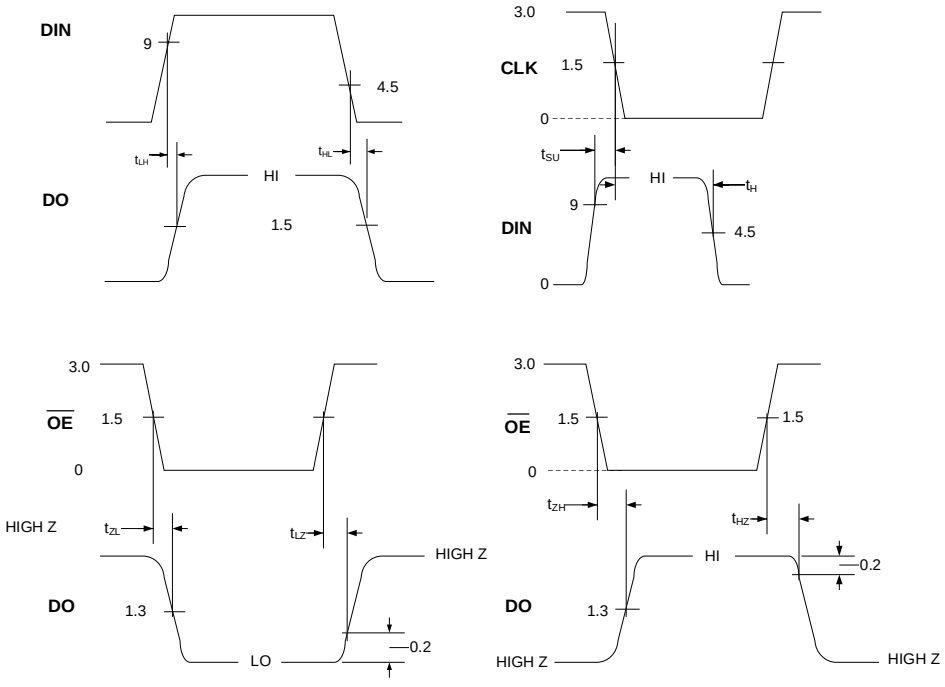


Figure 7 Switching Waveforms

APPLICATION INFORMATION

Discrete Input Filtering

The DEI1198 Analog Front End provides a moderate level of noise immunity via a combination of hysteresis and limited bandwidth. The Hysteresis is 3V minimum and the comparator bandwidth is approximately 10MHz.

Many applications provide additional noise immunity by means of debounce/filtering in software or in digital circuitry (i.e. FPGA). Common input debounce techniques are readily found with a web search of the term “software debounce” and range from simple detectors of two or more sequential stable readings to FIR filters emulating RC time constants.

Input Current Characteristics

The DIN Input Current vs. Voltage characteristics are shown in Figure 8**.**

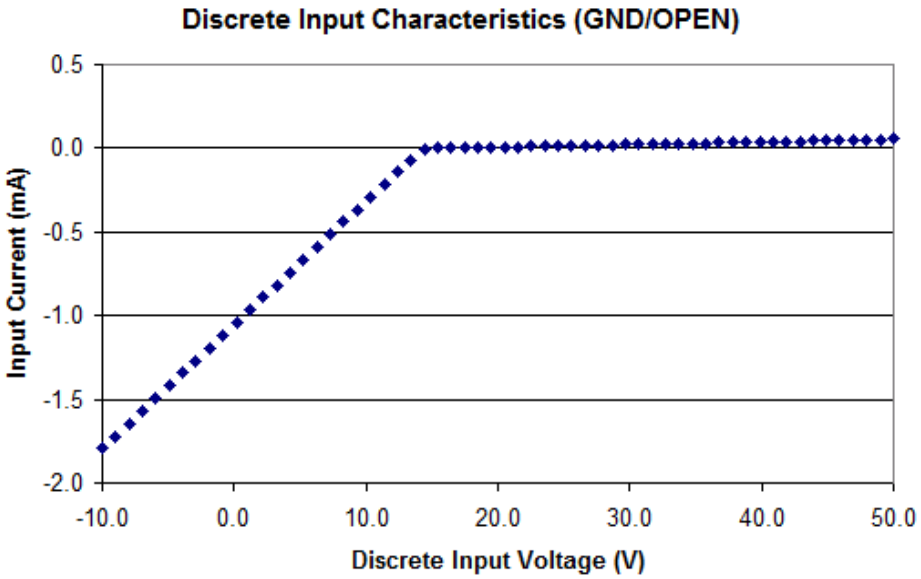


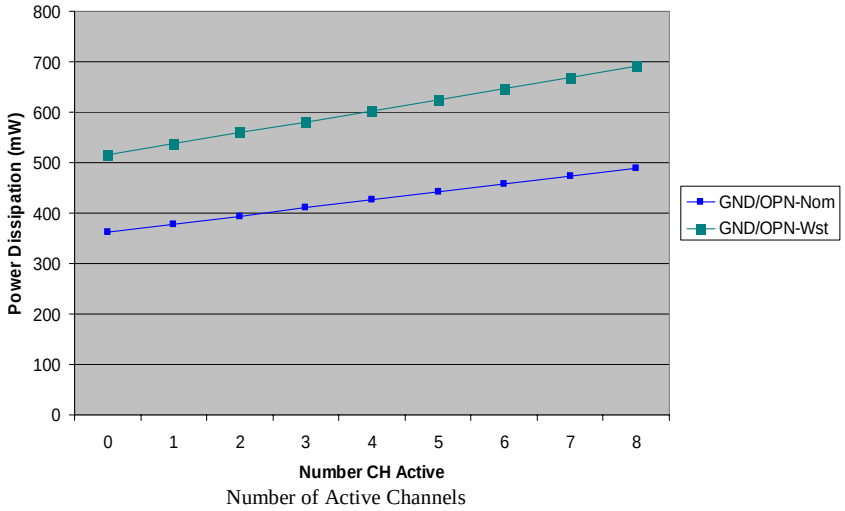
Figure 8 Input IV Characteristics (VDD=15V)

Package Power Dissipation

The DEI1198 power dissipation varies with operating conditions. **Figure 9** shows the device package power dissipation for various operating conditions. This includes the contributions from Supply currents and DIN Input currents. The curves are as follows:

Table 7 Legend for Power Dissipation Curves

CURVE ID	SUPPLY VOLTAGE, TEMPERATURE, IC VARIATION
GND/OPEN-Nom	3.3V, 12V / 27ºC / typical IC parameters
GND/OPEN-Wst	3.3V, 16.5V / 85ºC / Worst case IC parameters



Number of Active Channels

Figure 9 DEI1198 Power Dissipation vs Active Channels

ORDERING INFORMATION

Table 8 Ordering Information

Part Number	Marking	Package	Temperature
DEI1198-TES-G	DEI1198-TES	24 TSSOP G	-55 / +85 ºC
DEI1198-TMS-G	DEI1198-TMS	24 TSSOP EP G	-55 / +125 ºC

PACKAGE DESCRIPTIONS

Table 9 Package Information

PACKAGE TYPE	24TSSOP G	24TSSOP EP G
□□□ JA (4-layer PCB)	~ 84 °C/W	~ 29 °C/W
□□□ JC	~ 16 °C/W	~ 7 °C/W
MOISTURE SENSITIVITY	MSL 1 / 260°C	MSL 3 / 260°C
LEAD FINISH	NiPdAu	100% Matte Sn
MATERIALS	RoHS Compliant	RoHS Compliant
JEDEC REFERENCE	MO-153-AD	MO-153-AD

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the IC package**.** Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC leads**.**

The exposed thermal pad of the 24TSSOP EP G package must be soldered to a heat spreader land pattern on the PCB to achieve required thermal performance.

- Connect the exposed thermal pad to electrical Ground.
- Use large and multi-layer PCB boards, at least 4 layers 3" x 3", with internal solid GND and Power planes.
- Maximize the thermal pad land size by extending it beyond the IC to form a dog-bone pattern on the top layer and a similar sized heat spreader copper patter on the bottom layer.
- Use thermal VIAs to connect the thermal pad land pattern on the top layer, inter GND(s) and bottom GND layer. Place as many thermal VIA's in the land pattern as space allows to conduct heat from the thermal pad to the internal ground plane and bottom heat spreader.

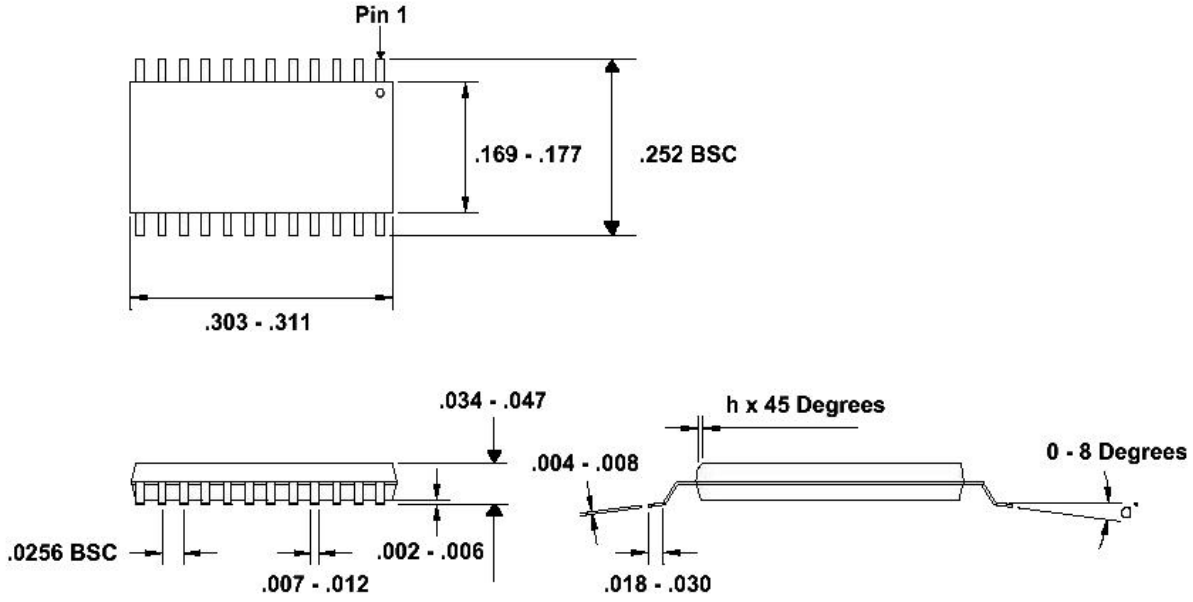
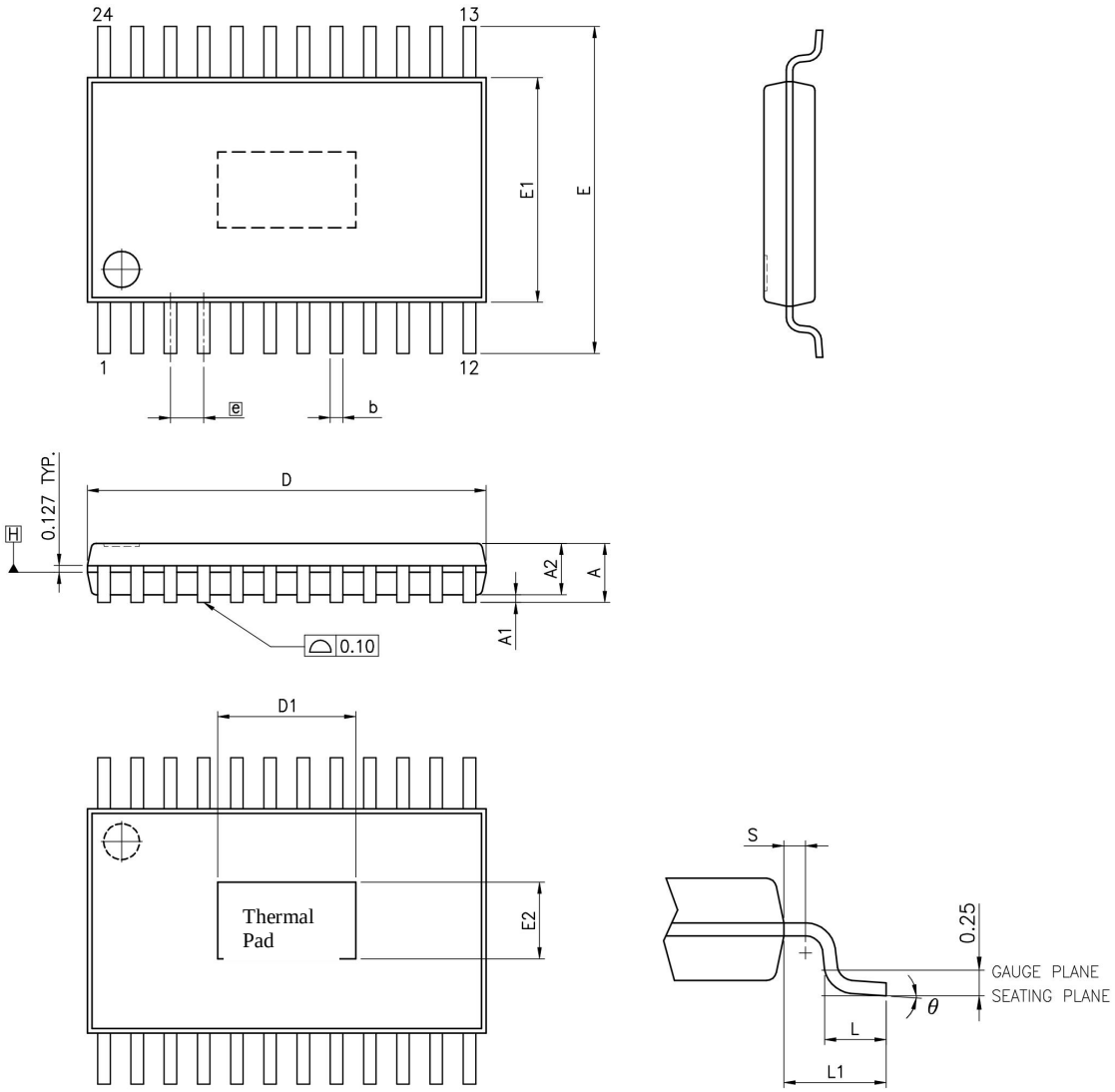


Figure 10 24 TSSOP G Outline



SYMBOLS	MIN	NOM	MAX
	--	--	1.20
A1	0.00	--	0.15
A2	0.80	1.00	1.05
b	0.19	--	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	--	--
□	0 °	--	8 °
E2	2.28	--	3.00
D1	3.70	--	4.75

Figure 11 24 TSSOP EP G Outline