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# DEI1058
# Six Channel Discrete-to-Digital Interface Sensing 28 Volt/Ground



## Features:

- Senses six 28V / Ground inputs
- Small footprint (16L SOIC NB)
- Inputs are lightning protected per DO-160D Level 3
- TTL/CMOS-Compatible Tri-state outputs
- Low Cost
- -55ºC to +85ºC operating temperature range.
- 100% Final testing

## Functional Description:

The DEI1058 is a six channel discrete-to-digital interface BiCMOS device. It senses six 28V/Ground discrete signals of the type commonly found in avionic systems. The inverted outputs are TTL/CMOS compatible and are enabled by the OE and CE pins. The inputs of this small 16 lead narrow body SOIC device are lightning protected to meet the requirements of DO160D waveforms 3, 4, and 5 Level 3. See figures 5-7.

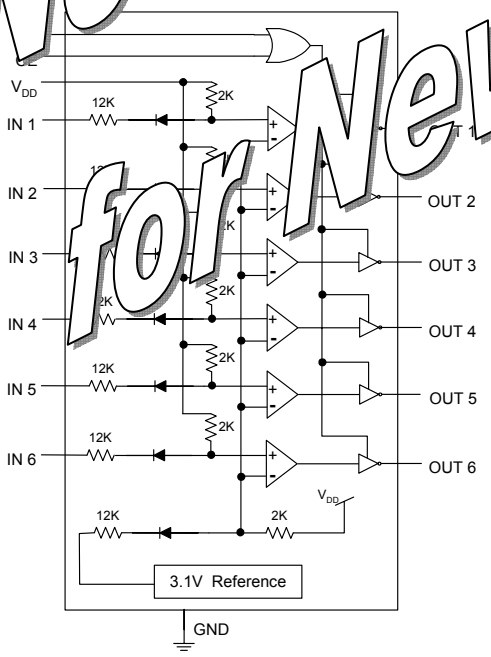


Figure 1: Concept Drawing

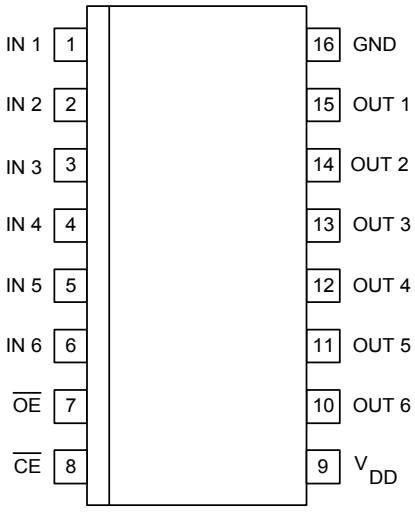


Figure 2: Pinout Diagram

| Table 1: Absolute Maximum Ratings | | | |
|---|---|---|---|
| **PARAMETER** | **MIN** | **MAX** | **UNITS** |
| Supply Voltage $V_{DD}$ | -0.3 | 7.0 | V |
| Discrete Input Voltage (Pins 1-6) | -5 | +35 * | V |
| Digital Input Voltage ($\overline{CE}$ and $\overline{OE}$) | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | V |
| Lightning Protection (Pins 1-6)<br>DO160D, Waveform 3; Level 3<br>DO160D, Waveforms 4, and 5; Level 3 | <br>-600<br>-300 | <br>+600<br>+300 | V |
| Storage Temperature | -55 | 125 | °C |
| Operating Free Air Temperature | -55 | 85 | °C |
| Lead Soldering Temperature (10 Seconds Max) | - | 280 | °C |
| Body Soldering Temperature (10 Seconds Max) | - | 210 | °C |
| The DEI1058 contains circuitry to protect inputs from damage due to electrostatic discharge. It has been characterized per JEDEC A114-A Human Body Model to Class 1. Observe precautions for handling and storing Electrostatic Sensitive Devices. | | | |
| * The DEI1058 will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A. | | | |

| Table 2: DEI1058 Device Operating Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| Supply Voltage | $V_{DD}$ | | 4.5 | 5.0 | 5.5 | V |
| Free Air Operating Temp. | $T_A$ | $V_{DD}$ = 4.5 – 5.5 V | -55 | | 85 | °C |
| Logic Output Sink Current | $I_{OL}$ | $V_{DD}$ = 4.5 – 5.5 V | | | 5.0 | mA |
| Logic Output Source Current | $I_{OH}$ | $V_{DD}$ = 4.5 – 5.5 V | -5.0 | | | mA |

| Table 3: DEI1058 Logic Truth Table | | | |
|---|---|---|---|
| **$\overline{CE}$ (Chip Enable)** | **$\overline{OE}$ (Output Enable)** | **Discrete Input** | **Output** |
| 0 | 0 | 28V | 0 |
| 0 | 0 | Ground | 1 |
| 1 | X | X | High Z |
| X | 1 | X | High Z |

| Table 4: DEI1058 Electrical Characteristics ($T_A$ = -55ºC TO +85ºC, $V_{DD}$ = 4.5 TO 5.5 V, Unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **Power Supply and Thermal Data** | | | | | | |
| Supply Current | $I_{DD}$ | $V_{IN}$ = $V_{DD}$ (all inputs)<br>$V_{DD}$ = 5.5 V | | 5 | 10 | mA |
| Thermal Resistance | $\theta_{JA}$<br>$\theta_{JC}$ | Junction to Ambient<br>Junction to Case | | 110<br>60 | | °C/W |
| Max. Junction Temperature | $T_{Jmax}$ | Max. Junction Temperature | | | 125 | °C |
| **Discrete Input Characteristics** | | | | | | |
| 28 Volt input voltage High Output | $V_{SG}$ | Voltage source from input terminal to ground for Logic High Output. | | | 3.0 | V |
| 28 Volt input voltage Low Output | $V_{SO}$ | Voltage source from input terminal to ground for Logic Low Output. | 3.5 | | | V |
| Ground State Input Resistor | $R_{IG}$ | Resistor from input to Ground to guarantee Logic High Output. | | | 100 | Ω |
| Input source current | $I_{IO}$ | Current sourced into 100 Ohm resistor to ground. | -100 | -330 | | µA |
| Reverse Leakage Current | $I_{IR}$ | $V_{IN}$ = 35 V, $V_{DD}$ = 0 V | | | 100 | µA |
| **Logic Input Characteristics** | | | | | | |
| $\overline{CE}$, $\overline{OE}$ input logic 1 level | $V_{IH}$ | | 2.0 | | | V |
| $\overline{CE}$, $\overline{OE}$ input logic 0 level | $V_{IL}$ | | | | 0.8 | V |
| **DC Output Characteristics** | | | | | | |
| Output logic 1 level (TTL) | $V_{OH}$ | $I_{OH}$ = -5 mA. | 2.4 | | | V |
| Output logic 0 level (TTL) | $V_{OL}$ | $I_{OL}$ = 5 mA. | | | 0.4 | V |
| Output logic 1 level (CMOS) | $V_{OH}$ | $I_{OH}$ = -100 µA | $V_{DD}$ – 50mV | | | V |
| Output logic 0 level (CMOS) | $V_{OL}$ | $I_{OL}$ = 100 µA | | | $V_{SS}$ + 50mV | V |
| Off-state Output Current | $I_{OZ}$ | $\overline{OE}$ = $V_{DD}$<br>$V_{DD}$ = 5.5 V<br>$V_{OUT}$ = 0 or $V_{DD}$ | | | +/-10 | µA |
| **Switching Characteristics** | | | | | | |
| I/O propagation delay | $t_{HL}$, $t_{LH}$ | Refer to Figure 4. | | | 150 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z | $t_{LZ}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low | $t_{ZL}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z | $t_{HZ}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high | $t_{ZH}$ | Refer to Figure 3. | | | 25 | ns |

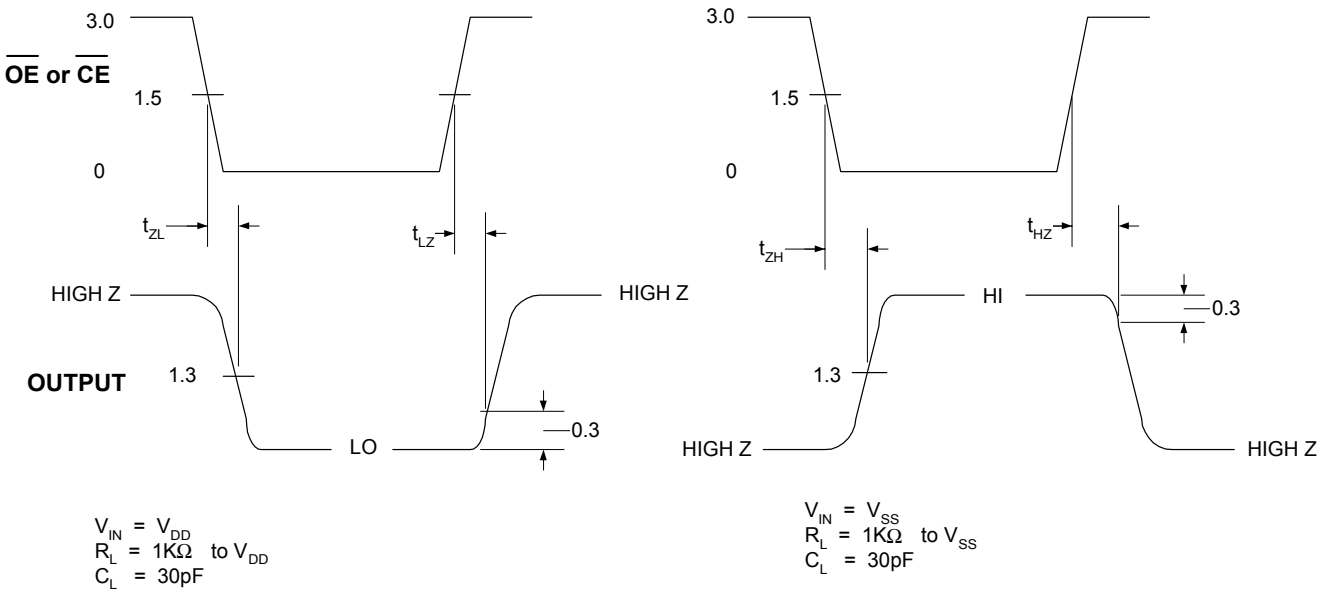


**Figure 3: Enable to Output Propagation Delay**

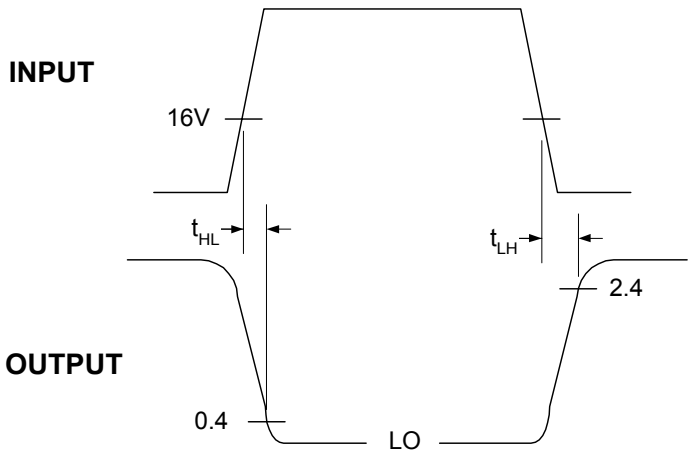


**Figure 4: Input to Output Propagation Delay**

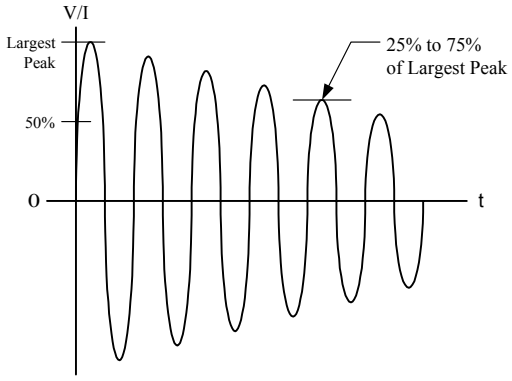


Figure 5: DO160D Voltage Waveform #3
$V_{OC}$ = 600V, $I_{SC}$ = 24A, Frequency = 1.0MHZ ±20%

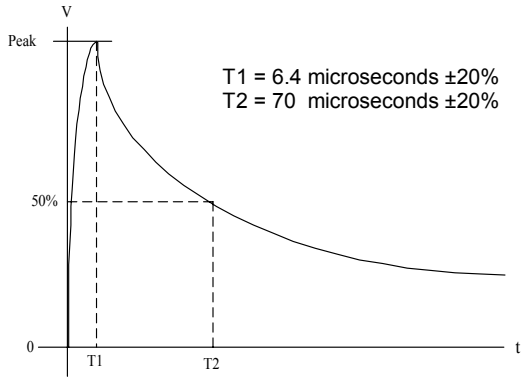


Figure 6: DO160D Voltage Waveform #4
$V_{OC}$ = 300V, $I_{SC}$ = 60A

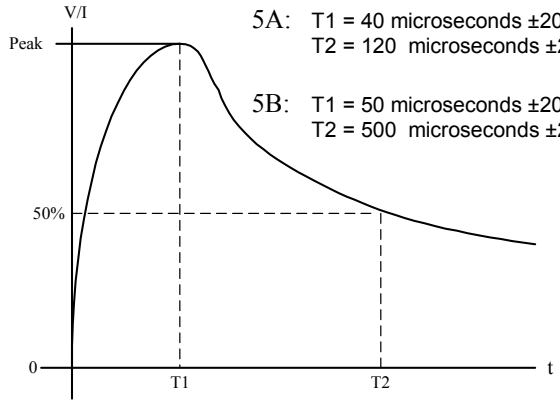


Figure 7: DO160D Voltage Waveform #5
$V_{OC}$ = 300V, $I_{SC}$ = 300A

Notes:

1. $V_{OC}$ = Peak Open Circuit Voltage available at the calibration point.
2. $I_{SC}$ = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%
4. The ratio of $V_{OC}$ to $I_{SC}$ is the generator source impedance to be used for generator calibration purposes.

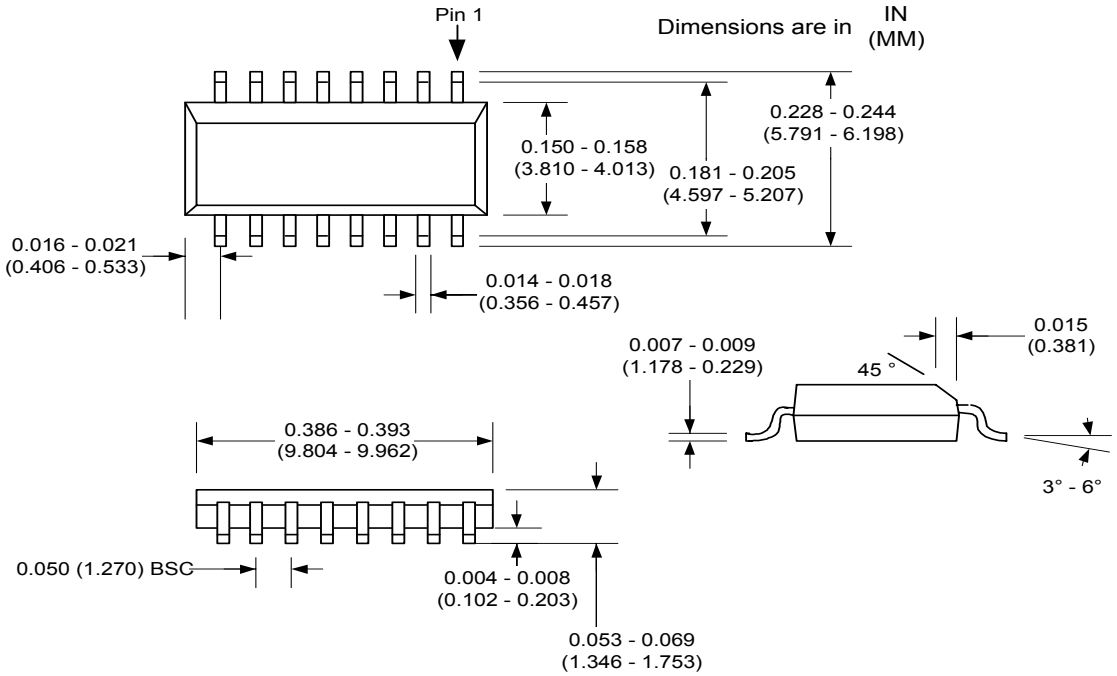


Figure 8: DEI1058 Mechanical Outline
JEDEC MS-012-16