TEL: 886-3-666-2866
FAX: 886-3-563-1498

R2880

RDC®

R2880

9. Peripheral Control Block Registers

12	NMIFLAG	R/W	NMI Flag. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequen- e written to this register.
11-8	Rsvd	RO	Reserved

Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.

a. The duration equation: **Duration =(** 2^{Exponent} **) / (Frequency/2)**
b. The Exponent of the COUNT setting:
(Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)
(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)
(x , x , x , x, x , x , x , 1) = (10)

R 2819.0 012 w 10 M

R2880