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9. Peripheral Control Block Registers

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12	NMIFLAG	R/W	NMI Flag. After WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.
11-8	Rsvd	RO	Reserved

Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.

- a. The duration equation: **Duration = (2^{Exponent}) / (Frequency/2)**
- b. The Exponent of the COUNT setting:
 (Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2, Bit 1, Bit 0) = (Exponent)
 (0 , 0 , 0 , 0 , 0 , 0 , 0 , 0) = (N/A)
 (x , x , x , x , x , x , x , 1) = (10)

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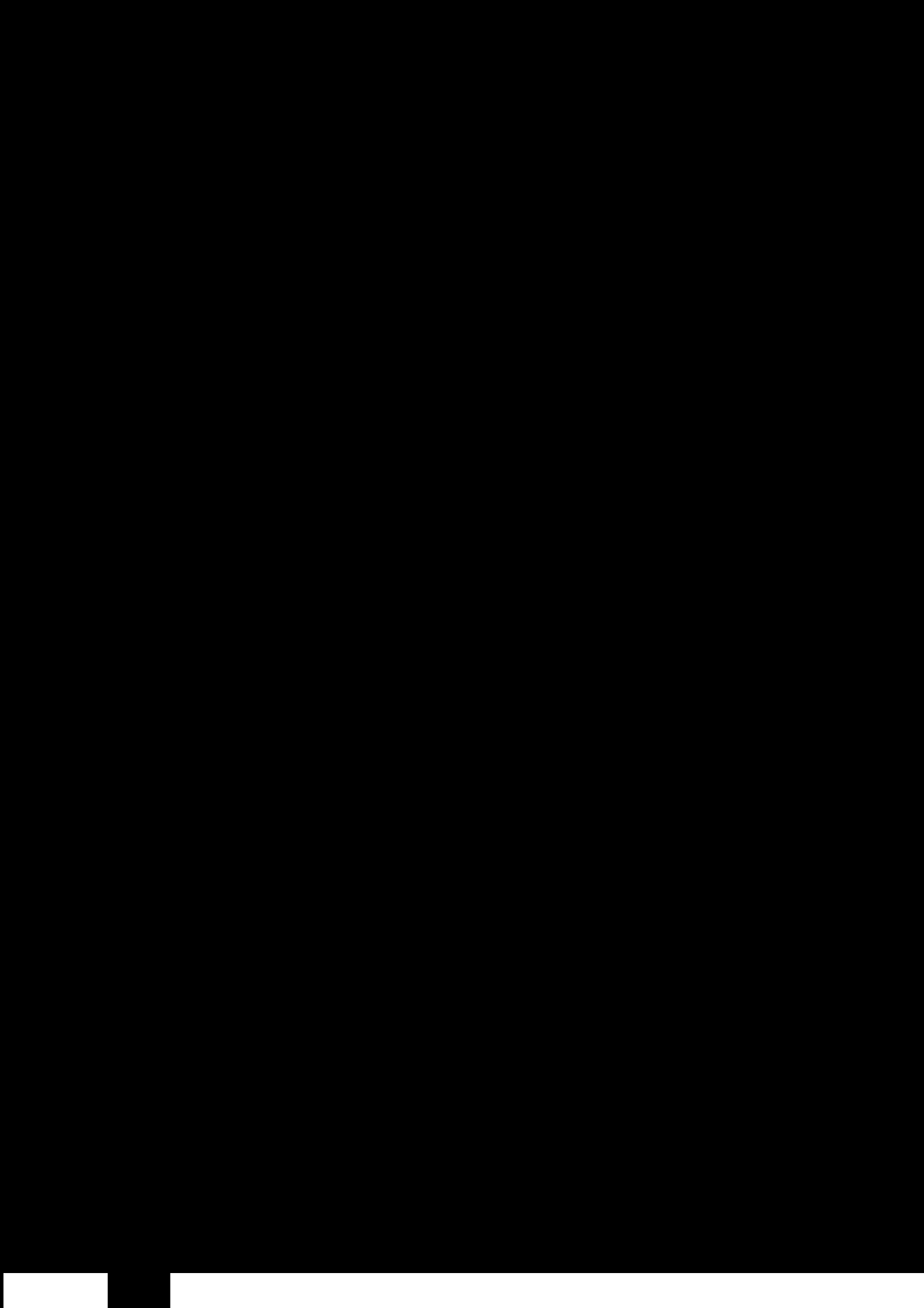
RISC DSP Communication

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